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Effect of Se Composition in CdSe*1-X*Te*X*/CdTe Solar Cells

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Effect of Se Composition in $CdSe_{1-X}Te_X$/CdTe Solar Cells

by

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DEDICATION

To my beloved parents

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

ABSTRACT

Cadmium Telluride solar cell is a leading thin film photovoltaic in the market today. Constant enhancement of efficiency in the last decade has made its position firmer in research interest as well. The record cell efficiency for CdTe solar cells is 22.1%. The theoretical limit suggests that there is still room for efficiency improvements. Reducing the band gap of CdTe solar cells can improve the short circuit current and overall cell performance.

This work focuses on bandgap engineering of the CdTe layer by incorporating Selenium (Se) in to form the compound $CdSe_xTe_{1-x}$ (CST) which can have a lower bandgap than CdTe, and it will therefore enhance the short circuit current density (J_{SC}) and cell efficiency. In this study three compositions of Se 7%, 15%, and 19% have been studied to understand the effects of Se on cell performance. The cell structure was glass/ITO/CdS/CST/CdTe/Back contact. The total thickness of CdTe and CST were maintained at 4 µm. All samples were exposed to the $CdCl_2$ heat treatment at temperatures of 390, 410, 420 and 430^0C. The thickness of the CST layer was also varied; three thicknesses 0.5,1, 1.5 and 2µm were investigated. Cells with CST layers with 19% Se composition and thickness of µm exhibited the best performance among three compositions. Among the four $CdCl_2$ annealing temperature 420^0C proved to produce the best overall cell performance. As the composition and thickness of the CST alloy increased a shift in the absorption edge from ~ 860 to 900 nm was observed in the QE indicating that the inclusion of CST resulted in improved JSC due to the smaller bandgap.

CHAPTER 1: INTRODUCTION

In the last decade the average energy consumption grew 1.7% each year, however, in 2017 there was a sharp rise in average energy consumption to 2.2% [1]. Fossil fuels is no match to mitigate this huge demand of energy as the cost of production and depletion of fossil fuel reserves will may lead us to run out of sources by 2088 [2]. Currently, natural gas has been the largest source of energy followed by renewable and oil sources. As fossil fuel is the greatest contributor for electricity generation and fossil fuel reserve is depleting day by day, we need to look for alternative sources for electricity generation. Renewable energy, to be very specific for our research Photovoltaic technology is the best alternative one can get, as this is not only environment friendly but also a long-term solution to this acute problem.

There are many types of renewable energy sources available currently, like solar, wind, water, and geothermal. But among all these sources solar stands out to be the brightest one with future prospect, and it's projected that by 2050 it will be the leading source of electricity generation [3]. If only the earth's surface can be covered by 0.1% with photovoltaic or solar cells with only 10% efficiency, then it is possible to fulfill the whole demand for electricity [5]. So, with this huge amount of source of energy, only efficient technique is required to develop photovoltaic cells to convert this energy with greater efficiency and store it in.

1.1   Photovoltaics

Certain electronic materials mainly semiconductors absorb sunlight and convert this light energy into electric energy called photovoltaics . The word photovoltaics comes from the Greek

word *phos* meaning light and -volt comes from the name Alessandro Volta (1745-1827) referring to electricity, revering the point that battery was invented by him [4].]. Generally, a solar cell is combination of two types of semiconductors, p-type and n-type semiconductors. In p-type semiconductors holes are the dominant charge carriers and in n-type electrons are the dominant charge carriers. Semiconductors have conductivity in between an insulator and most of the metals. Solar energy (photons) creates electron-hole pairs in PV devices, and through the subsequent collection of these electron-hole pairs the absorbed energy is converted to electrical energy. Depending on the wavelength, incident photons have different range of energies. PV cells must absorb energy more than its materials band gap energy in order to excite electron from the valence band to the conduction band. Through the collection of these high energy electrons which is current, an external load can be added to the device where it can perform the electrical work
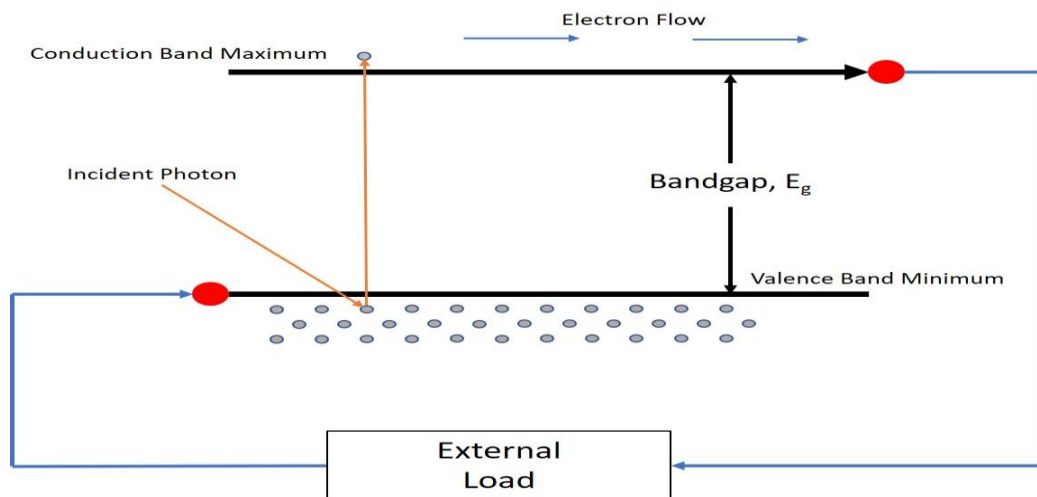
Figure 1.1 Basic mechanism of solar cell

1.2   Current Photovoltaic Technologies

Exploring solar cell technologies is an on-going topic of research. Photovoltaic technologies or solar cells can be categorized in many types depending on different factors. In general, they can be grouped in three categories.

1.2.1   First Generation Solar Cells

First generation solar cells also known as Crystalline Silicon Solar Cells was first developed by Bell Laboratories in 1954 with only 6% efficiency. This Silicon solar cell is dominating the market as it has more than 80% installations for residential use of the PV market [6]. As Silicon is the most abundant element on earth after Oxygen and has a band gap of 1.1 eV, very suitable material for PV applications [6]. Based on the structure of Silicon, Crystalline Silicon Solar cells are classified into two categories: Monocrystalline Silicon Cells and Multi-crystalline Silicon Cells. In 2014 among all the solar cells installed single or monocrystalline was 35% and multi-crystalline was 55%, making them the most available PV technologies [7].

a)   Monocrystalline Silicon Cells

These cells are made of single crystals of silicon. Using the Czocharlski method Cylindrical single crystals are developed. [8,9]. The wafers or big crystals are processed under controlled temperature and time in order to develop a uniform junction and suitable depth. Single crystalline Silicon production cost is very high due to the complexity and energy intensive fabrication, making the single crystalline silicon solar cells expensive as well. The latest record cell efficiencies for Monocrystalline Silicon Cells has reached 26.7% for small area cells and 24.4% for module with large areas [11].

b)   Multi-crystalline Silicon Cells

Substantial progress has been made for Si PV technology, when multi-crystal Si wafers were fabricated. A sharp diminution of fabrication cost is one of the advantageous facts about these cells as instead of making single crystal, molten silicon is decanted in mold, hence it doesn't require strict control of temperature and time [12]. Present record efficiency for small area cells is 22.3% and 19.9% been achieved for large area modules [11].

Till the late 80's Si had been the most prevalent solar cell material in the market, however, Si is also an indirect bandgap material, due to that factor it has a lower absorption coefficient than direct band gap semiconductors, making it not the most suitable material for light to electricity conversion. To counterbalance these effects a thick Si layer on the order of hundred micrometers is required to be fabricated, so that it can absorb most of the incident light. A Si wafer ranging from 100-300 µm leads to high processing costs, which is also the cause for higher module production costs. Si bears almost 40% of the final module cost [13]. Si solar cell efficiencies have approached the theoretical efficiency of single junction Si solar cells of nearly 33% [13]. As this Si PV technology is at its pinnacle, it is unlikely there would be any impactful advancement with this technology.

Another interesting first-generation solar cell technology is GaAs PV cell, a III-V semiconductor. As it is a direct band gap material it has high absorption coefficient and has a band gap of 1.42 eV which is better suited to match the solar spectrum than Si. Efficiencies of 28.8% for Small area cells and 25.1% for modules have been achieved to-date using this technology [11]. Despite its high efficiency, high manufacturing cost has confined this technology's usage only to space application and concentrated solar power systems [7]. The major cost for this PV technology is due to the GaAs parent wafer, and the processing technique that is used: epitaxy.

Another type of III-V PV cells which increases the efficiency of the cell is multijunction solar cells. Multijunction or Tandem solar cells are comprised of several layers of cells stacked on top of each other. Each layer is called a sub cell, and absorbs a certain range of wavelengths of light depending on the bandgap of the absorbers.

1.2.2 Second Generation Solar Cells

Thin Film Solar Cells (TFSC) are referred to as second-generation solar cells. In TFSC layers of semiconductor materials with only few micrometers of thickness are used due to their high optical absorption coefficients. As this technology requires less materials to fabricate compared a solar cell copmared to Si solar cells the production costs of this cell is also cheaper. The most common commercially used second generation cells are Amorphous Si (α-Si), Copper Indium Gallium Diselenide (CIGS) and Cadmium Telluride (CdTe). The common feature that has made this technology very lucrative is the direct band which are 1.75 ev, 1.0~1.7 ev, 1.45 for.

PECVD or Plasma-Enhanced Chemical Vapor Deposition technique is employed to deposit Amorphous Si from hydride gases like SiH_4. The uniformity of the coatings can be assured over a large area with exceptional control using this method. However, this is not a very efficient method to fabricate the cells as only 10%-30% gas is used there is much wastage of source material. Among all the TFSC materials Amorphous Si has the lowest fabrication temperature (150^0-300^0 C) making it the low cost and temperature supple technology. It has achieved efficiencies up to 10.2% for small area cells and 12.3% for tandem modules [11]. For low cost and low power electronics like toys and calculators α-Si devices have a very specific market. However, this technology has the tendency of degrading as the light is induced and with lower efficiencies it makes the technology unsuitable for commercial scale production. Moreover, other solar cell technologies are becoming cheaper making it difficult for this technology to survive.

A compound semiconductor material Copper Indium Gallium Diselenide (CuIn$_X$Ga$_{1-X}$Se$_2$ or CIGS) is a much better PV technology than α-Si, which is also a direct bandgap material with a band gap of 1.0-1.7 ev [14]. It has almost captured the 1.3% of the global solar cell market and 27% for thin film photovoltaics [15]. Efficiencies for small area cells have been achieved 22.6% and 19.2% for modules [16]. However, for complex stoichiometry control it has become hard to fabricate this technology.

Now CdTe has become the stellar TFSC technology with global 3.1% market and with 63% TFSC market [15]. As CdTe, a direct bandgap material with a bandgap of 1.45-1.5 ev and high absorption coefficient has become a well-tailored semiconductor material for PV application. With the lowest module cost CdTe has become the most thriving PV technology currently. It costs the lowest among any PV technology today and First solar Inc. is the leading CdTe PV cell producer in the market today. Small cell area efficiency at laboratory scale is 22.1% with the equivalency of multi-crystalline Si solar cells [16]. Record efficiency for modules is 18.6% [17]. The only concern for CdTe PV technology is the toxicity of Cd and scarcity of Te, which are the raw materials for this technology to fabricate. As the purpose of this study is to discuss CdTe PV technology, elaborate discussion is available in the upcoming chapters.

1.2.3 Third Generation or Emerging Solar Cell Technologies

Third generation or emerging solar cells are fabricated using nano-structured materials or polymers so that optimum electrical and optical properties can be achieved [14]. Among many third generations solar cells Dye Sensitized Solar Cells (DSSC) and Perovskites solar cells are the most prominent technologies for low cost of production.

Dye Sensitized Solar Cells (DSSC) which was invented by Michael Graetzel also referred as Graetzel cells [5]. To generate electricity an organic dye is used when it comes under the effects

of illumination it produces collectible electron. A high band gap and porous paste like TiO_2 is used to collect the molecules or for charge separation. Electrolyte is employed for charge collection. This technology has shown efficiencies for small area cells up to 11.9% and for modules 8.8%. [11]. In terms of efficiency DSSC doesn't match with the first- and second-generation solar cells, but it has other advantages over the two previous technologies. For a wide range of temperature typically 25^0C to 65^0C it is almost temperature independent. Whereas Si on the other hand shows declined efficiency by 20% for the same range of temperature [18]. DSSC shows better performance in terms of efficiency in soft light or cloudy conditions than typical polycrystalline Si solar cells. In addition to that DSSC can be made in different colors, so from an aesthetic point of view it is appropriate for different or certain application.

Through DSSC a new kind of solar cell technology has germinated, that is Perovskites solar cells. Within only 5 years of its development it has achieved efficiency up to 20.9% [11]. ABX_3 Crystal structure also referred as perovskites structured compound is the main absorber layer for the cells, the most common material for this technology is inorganic-organic lead halide $CH_3NH_3Pb(l,Cl,Br)_3$. Its band gap is engineered to match the solar spectrum, and low manufacturing costs, simple fabrication process has drawn interest of research for this technology. However, stability for long term and lead toxicity have some reasons for vexations, but extensive research is ongoing for this PV technology.

CHAPTER 2: SEMICONDUCTORS AND SOLAR CELL MATERIALS

2.1 Semiconductors

Semiconductor materials have electrical properties in between of a conductor and an insulator. In room temperature they are neither conductors nor insulators hence, the name semiconductor is given. As the atoms in semiconductors are closely attached together in a crystalline orientation, the number of free electrons is few, however with certain conditions electrons can move freely inside the material. To improve the ability of conduction of semiconductors external atoms can be added or replaced as acceptor or donor atoms into the crystalline structure, so that more electrons than holes or vice versa situation is present. This process of adding or replacing atoms is called doping and the external materials or impurities are called dopants. Doped semiconductors are called extrinsic semiconductors and pure ones are called intrinsic semiconductors. Based on the type of impurity added semiconductors can be categorized in P-type or N-type semiconductors. The most widely used semiconductor material is Si, it belongs to the group IV of the periodic table and has four valence electrons in its outer most shell. Si can be doped with Boron a group III element from the periodic table to make a P-type semiconductor or it can be doped with Phosphorus a group V element to make N-type semiconductor. In semiconductor materials N type doping increases the number of electrons and P type doping increases the number of holes. Two or more materials can be composed to make semiconductors, such kind of semiconductors are called Compound semiconductors. It can be comprised with two different elements from the like GaAs, GaN, they are named after the groups

they belong from like GaAs or GaN are III-V semiconductors, as Ga belongs to group III and As or N belongs to go group V. There are group II-VI materials as well like CdTe, Cds etc.

In the energy band diagram, there is a gap between Conduction Band minima (E_C) and Valence band minima (E_V) that gap is known as bandgap of the material. Electrons by absorbing photons or acquiring thermal energy can go from valence band to the conduction band and can move freely inside the material. In intrinsic semiconductor materials the fermi level (E_i), which narrates the probability of finding an electron across the bandgap, lies in the center of the band gap, for non-intrinsic semiconductor the fermi level (E_f) can lie anywhere in the bandgap depending on the type of doping the semiconductor has.

2.2   P-N Junction

2.2.1   Homojunction Semiconductors Under Equilibrium condition

When two types of semiconductors of same material, p-type and n-type namely are connected then homojunction is formed. P-type semiconductor part has holes as the majority carrier and in case of n-type electron is the majority carrier. For P-type semiconductor the fermi energy level is near to the Valence Band (VB) and the for N-type the fermi energy level is near to the Conduction band (CB). The built-in potential is given by:

$$V_{bi} = \frac{kT}{q} \times \ln\left(\frac{N_A \times N_D}{n_i^2}\right) \qquad 2.1$$
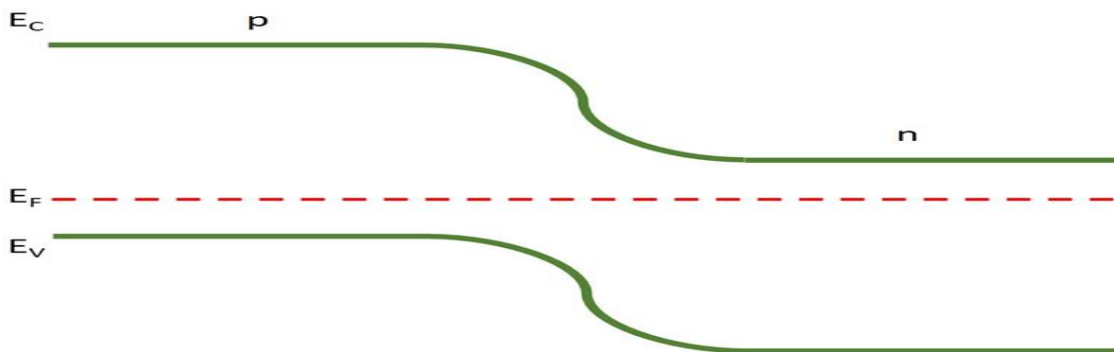
Figure 2.1 Homojunction (P-N junction) under equilibrium

2.2.2 Homojunction Semiconductors Under Reverse and Forward Bias Condition

Under forward bias condition majority of the voltage drop of the applied voltage happens across the depletion region. Hence the depletion width decreases and the majority carriers of the n side which is electron can overcome the barrier reaching the P side. But in case of reverse bias condition the applied voltage increases the built-in potential and as a result the barrier gets higher, the electrons on n-side face a higher barrier to cross over and reach the p-side. The barrier equation is given by:

$$V = (q \times [V_{bi} + V_a])$$ 2.2

Under reverse bias condition the current is governed by the given equation:

$$I = I_0 \times \left(e^{\frac{qV}{AkT}} - 1 \right)$$ 2.3

2.2.3 Heterojunction Semiconductors

When two different semiconductor materials are connected then heterojunction is formed. Depending on the band alignment they are called type I, II and III. The discontinuities of the band for conduction band and valence band can be expressed as:

$$\Delta E_C = X_p - X_n$$ 2.4

$$\Delta E_V = E_{gp} - E_{gn} - E_g$$ 2.5

2.3 Basics of Solar Cells

2.3.1 Solar Spectrum, Quantum Efficiency, and Air Mass

Efficiency of solar cells depends on many factors like incident light spectrum, incident light intensity, operating temperature of the solar cell as well. The earth's solar radiation intensity which is expressed as W/m^2, remains constant outside the earth's atmosphere. Some light gets absorbed before reaching the earth's surface and gets scattered by the water vapor and other elements in the atmosphere.
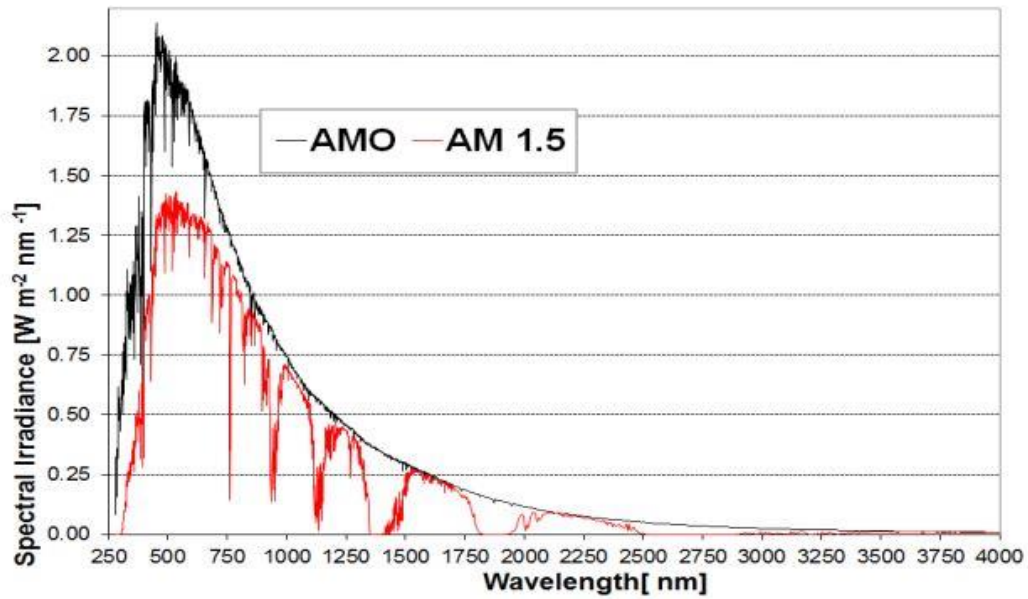
Figure 2.2 Solar spectrum [36]

Quantum efficiency (QE) or External Quantum Efficiency (EQE) is a measure of how efficiently the solar cell is generating the photo generated charges at a particular wavelength of incident light. QE is a function of wavelength which is expressed as the ratio of number of photons incident to the number of generated charge carriers. In equation it can be expressed as:

$$QE(\lambda) = 1240 \times \frac{I_{SC}}{\lambda \times \Phi} \qquad\qquad 2.6$$

where, I_{SC} = Short Circuit Current (mA/cm^2)

λ = wavelength (nm)

Φ = incident radiative light flux (W/m^2)
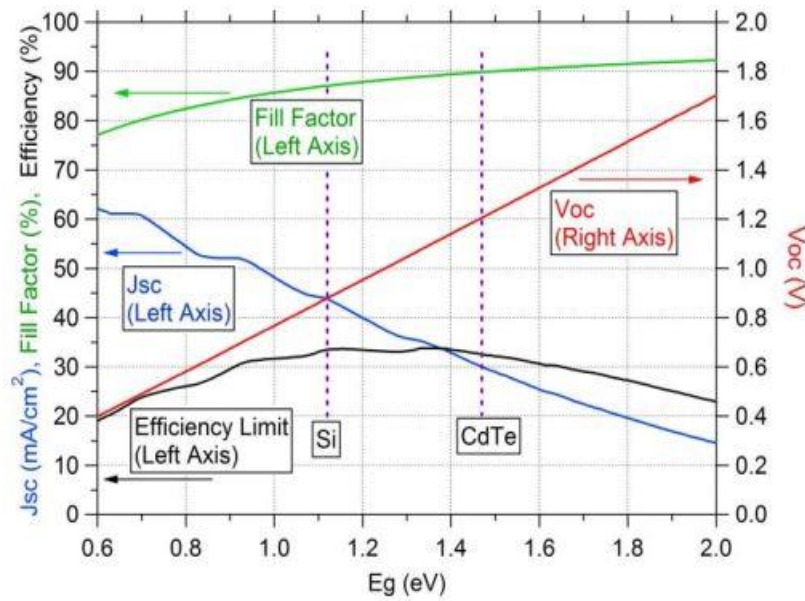
Figure 2.3 Theoretical limits for different solar cell parameters

2.3.2 Solar Cell Function Mechanism

Solar cells basically perform three basic operations in order to generate electricity from the absorption of incident light upon it. These 3 basic mechanisms are: absorption of incident sunlight, from that light energy generating electron hole pairs or in other words photo generated charge carriers, and finally collecting those photo generated charge carriers.

2.3.3 Basic Solar Cell Parameters

The equivalent circuit for solar cell can be drawn with a current source parallel with a forward bias diode, and two additional resistances series resistance (R_S) and shunt resistance (R_{SH}) to show different types of loss mechanisms in the circuitry.

The most important parameter for solar cell like any other electronic device is the efficiency or photo conversion efficiency. It can be measured from the ratio of maximum output power to the input from the sun. Mathematically it can be expressed as;

$$\eta = \frac{V_{OC} \times I_{SC} \times FF}{P_{in}}$$

2.7

12

Fill Factor (FF) which is also the measurement of squareness of the of the cell's I-V curve.

$$FF = \frac{V_m \times I_m}{V_{OC} \times I_{SC}}$$

2.8

when the voltage across the solar cell circuit becomes zero meaning when it short circuited then the current is called the Short Circuit Current, as the cell is short circuited the name is drawn from that idea. Short circuit current is the result due to the collection of photo generated carriers.

$$J_{sc} = \frac{I_{SC}}{A} \ (\text{mA/cm}^2)$$

2.9

The maximum output voltage of the solar cell is the open circuit voltage (V_{OC}) and is measured when the cell is under open circuit condition meaning no load is attached to the cell, thus the name comes from this phenomenon. Open circuit voltage is obtained from the equation below:

$$V_{OC} = \frac{kT}{q} \ln\left(\frac{(N_A + \Delta n)\Delta n}{n_i^2}\right)$$

2.10
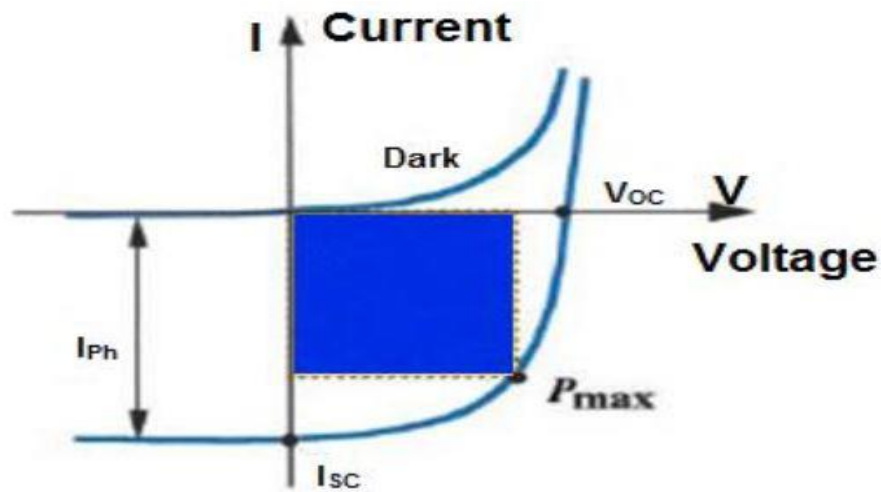
Figure 2.4 I-V characteristics on light and dark condition [37]

CHAPTER 3: CADMIUM TELLURIDE SOLAR CELL TECHNOLOGY AND REVIEW

3.1   Why CdTe Solar Cell?

CdTe is a direct bandgap material, with a bandgap of 1.45 ev an ideal material for PV application, converting the sunlight into electricity. As the absorption coefficient for CdTe is more than 5×10^5 cm^{-1}, meaning that the material only requires few micrometers to absorb all the incident light upon it up to the wavelength of almost 860 nm [19]. As a result, CdTe solar cell requires thinner absorber layer compared to Si solar cells. A relatively low-cost methods can be applied to fabricate CdTe solar cell devices with high efficiencies. The most common fabrication methods for CdTe solar cells are Sputtering, Closed Space Sublimation (CSS), Physical Vapor Deposition (PVD), Electron Vapor Transport (EVT), Metal-Organic Chemical Vapor Deposition (MOCVD), Spray Deposition etc. To be an alternative to fossil fuel and a better commercial product research on CdTe solar cells further pushed ahead, even though CdTe solar cells have overtaken the efficiency of multi crystalline solar cells very recently [11].

3.2   Hazardous Concern for CdTe

People are very concerned about pollution of Cd, since it may cause some health and environmental concerns. However, intensive research has shown that the CdTe solar cell shows the lowest carbon footprint on earth and a very environmentally friendly PV technology [20]. The solubility of CdTe as a compound material is much less than Cd and hence the toxicity of CdTe is much less than Cd only. As Cd is a byproduct from Zinc production, the amount of Cd produced each year is tens of thousands, if this byproduct is not processed industrially then it must be processed as hazardous waste. It only requires only 1% of the Cd produced each year to

manufacture CdTe solar cell in GW/year scale [21]. First solar the leading manufacturing company for CdTe PV conducted a medical study on their one of the employees who work with CdTe material, they found Cd well below the threshold limit in their system [22]. Zero emission Cd can be maintained at plants technically [23]. In case of solar modules and fire hazards, a typical residential fire incident can have temperature risen to 800 to 1000^0C, in this temperature no Cd is released at the surrounding environment [24]. For broken panels from decay or any accident the amount of Cd found there is well below the tolerance limit [25].

3.3   Current Scenario of CdTe Solar Cells

Over a decade research on CdTe solar cell has been going on to improve the cell conversion efficiency. There is a rapid growth in CdTe cell efficiency in recent years. The record cell efficiency has been achieved 22.1% by First solar (FSLR), a leading CdTe solar cell manufacturer. At the university research level, the highest efficiency gain has been achieved by Colorado State University which is 18.3% [26]. Rudolf Frerichs first introduced crystalline CdTe in 1947, through the reaction of Cd and Te under the presence of hydrogen atmosphere [38]. It took seven years to find out that n type and p type conductivity is possible through this material. In 1954 Dietrch A. Jenny and Richard H. Bube obtained p type and n type conductivity through doping [39]. In 1959 Rappaport first fabricated single crystal homojunction CdTe solar cell at RCA laboratory facilities [40]. CdTe as thin film cells was first fabricated by D. A. Cusano in 1963 [41]. The most common device structure for CdTe solar cells CdS/CdTe was first fabricated by Andirovich in 1968, efficiency for that devices as on;y ~1% [42]. Later on Kodak and AMETEK achieved 10% and 19% efficiency respectively. In 1992 C. Ferekides and J. Britt achieved the efficiency of 15.8% [43]. In later part of 90's First Solar improved the efficiency up to 16%.

Table 3.1 Recent trend of CdTe solar cell growth

Year	Institutions	Efficiency %	V_{OC} (mV)	J_{SC} (mA/Cm^2)	FF %	Ref.
1993	USF	15.8	843	25.1	74.5	[27]
1997	Matsushita	16.0	840	26.1	73.1	[28]
2001	NREL	16.7	845	26.1	75.5	[29]
2011	FSLR	17.3	845	27.0	75.8	[30]
2012	GE	18.3	857	27.0	79.0	[31]
2012	FSLR	18.7	852	28.6	76.7	[32]
2014	FSLR	21.4	876	30.25	79.4	[33]
2016	CSU	18.3	863	26.8	79.2	[34]
2016	FSLR	22.1	-	-	-	[26]

3.4   Purpose of Research

The theoretical limit of efficiency or the Schokley-Queisser Limit is 33% for CdTe solar cell devices [34]. The theoretical of Open Circuit Voltage (V_{OC}), Short Circuit Current density (J_{SC}) and Fill Factor (FF) calculated 1.156V, 30.5 mA/Cm^2 and 88.7% respectively [35]. To improve the cell performance these three factors must be improved. In case of J_{SC} the improvement can be perceived by studying the Q.E. curve of the cells (figure 3.1) [44].
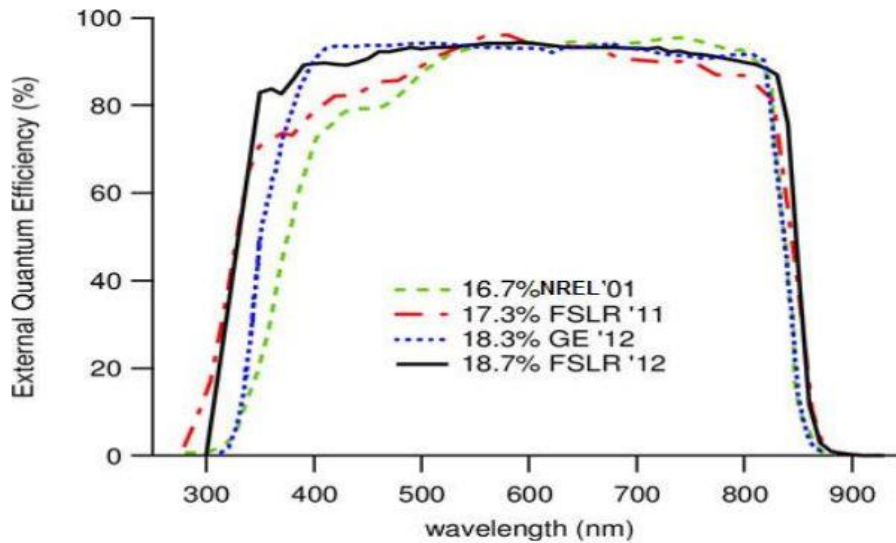
Figure 3.1 Champion cell's QE curve [45]

The absorption of photons in shorter wavelengths typically less than 510 nm suggests the reduction of thickness of window layer, which is CdS in this case. To increase the absorption in longer wavelengths of photons bandgap engineering is done through the incorporation of Se. Factors limiting the V_{OC} and FF cannot be perceived directly from JV or QE curves, cause physics of polycrystalline cells is very complex. But to understand the limiting factors a set of parameters have been suggested called "Third level: metrics", where the metrics finds out each parameter limiting factors like carrier concentration or carrier lifetime to have a better understanding of the cause of the limiting the V_{OC} or FF individually [45]. From this metric it can deduced that the limiting factors for V_{OC} can be attributed to low carrier lifetime, non ohmic contact and poor interface quality between CdTe and CdS.

17

3.5 Strategies for Better Cell Performance

3.5.1 Open Circuit Voltage (V_{OC})

Poor open circuit voltage of the devices can be attributed to many factors, among them poor minority carrier lifetime, poor acceptor concentrations, and non ohmic back contact are the main factors. Improving the acceptor concentrations may improve the V_{OC}, but it will reduce the Fill Factor. Using the Cu doped graphite paste as back contact can help to have a better ohmic contact and better Fill Factor. It also reduces recombination at the CdS/CdTe grain boundaries and improves carrier lifetime.

3.5.2 Short Circuit Current Density (J_{SC})

Low short circuit current is due to the failure of current collection after the electron hole pairs generated and poor absorption at the long wavelengths range. Absorption at the long wavelengths can be improved by alloying Se with CdTe to form $CdSe_{1-X}Te_X$ (CST) layer. As the absorption goes higher so does the carrier collection, because higher photo generated carriers can help to improve the collection probability.

CHAPTER 4: EXPERIMENTAL PROCEDURES AND CHARACTERIZATION

Like any other semiconductor device solar cell performance also depends on the fabrication methods used. In this chapter the cell fabrication details and measurements to evaluate the performance of the fabricated devices will be discussed. All solar cells used in this study are of the superstrate configuration. There are two types of configurations for fabricating solar cells, substrate and superstrate configuration. Superstrate configuration is not only the supporting structure of the cell but also the acts as a window for illumination and as the glass remains above the cell thus the term super. On the other hand, the substrate configuration the glass serves as the *bottom of the cell* where the back contact is deposited first, and light enters thorugh a transparent contact that is deposited last. The basic structure of the superstrate cells is glass/ITO/MZO/CST/CdTe/Back Contact, which is showed in figure 4.1.
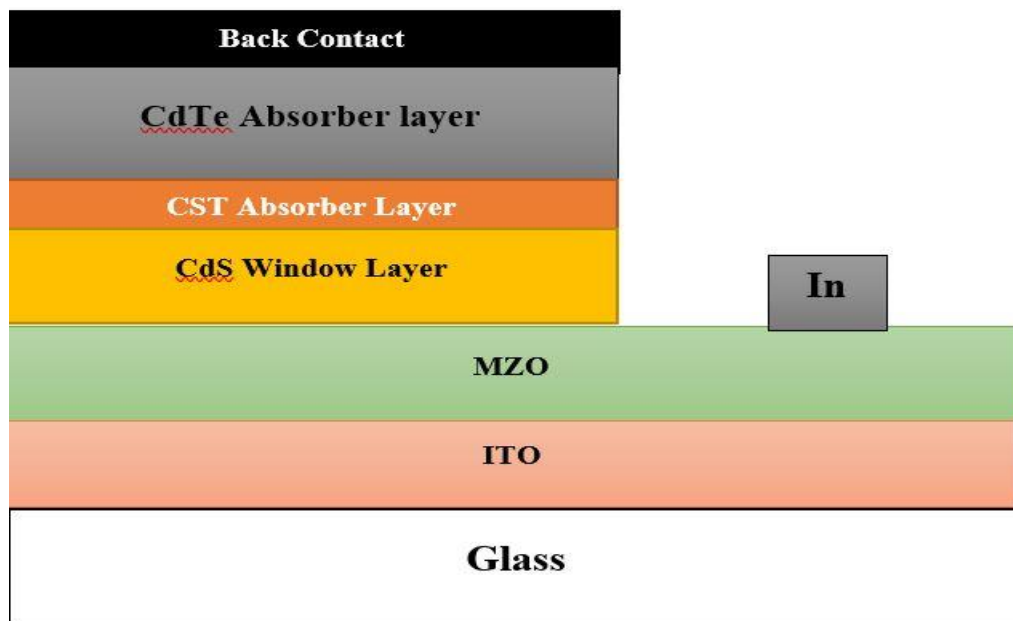

Figure 4.1 Cell structure

4.1 Cell Fabrication

All fabrication steps used for this thesis are discussed in the following sections. The glass on top which all the layers are deposited is Corning Eagle XG 2000 glass. The Corning eagle glass is alkali free and has high optical transmittance up to 90% for incident lights for wavelength of 350-2200 nm. The thickness of the glass is only 0.7 mm with dimension of 1.45inch×1.32inch. All the glass substrates were cleaned with de-ionized water and then etch for 15 seconds in 10% HF solution.

4.1.1 Transparent Conducting Oxide (TCO)

The main characteristics of transparent conducting oxides are: transparency in the range of 400 to 900nm, good thermal stability chemical stability. Electron affinity of TCO should around 4.5 ev in order to form better ohmic contact with CdS layer. For CdTe solar cells there are some common TCOs such as: Florine doped Tin oxide (SnO_2:F), Cadmium Stannate (Cd_2SnO_4) and Tin doped Indium Oxide (In_2O_3:Sn).The TCOs are usually heavily doped and hence their Fermi energy level lies to the near to the conduction band. The TCOs that are deposited should have some characteristics like resistivity lower than 10^{-4} Ω cm, high transmission in the wavelength range of 300 nm -900 nm, chemically stable during high cell processing temperature. Transparent Oxides (TO) usually behave like insulators due their wide band gap as an intrinsic material. By doping the TCOs, conductivity of the material can be enhanced significantly. The formation of oxygen vacancies act as a n-type native defects in TCO materials, thus these materials typically exhibit n-type semiconducting behavior. For this study Indium doped Tin Oxide (ITO) was deposited using RF sputtering technique. The layer was deposited in ultra-high purity (UHP) Ar environment. ITO purity was maintained at 99.999%. the thickness of ITO was $4000A^0$ and the temperature was 275^0 C during the deposition. The resistivity of the TCO was

lower than 2×10^{-4} Ω cm. Tahr et al. showed that they obtained resistivity low as 2×10^{-4} Ω cm [46].

4.1.2 Mg$_X$Zn$_{1-X}$O (MZO) Layer

The Magnesium Zinc Oxide (MZO) is a ternary wide bandgap II-VI semiconductor material. It is an alloy of MgO and ZnO, two highly wide bandgap material, making it a wide tunable bandgap semiconductor material. By optimizing the band alignment between CdTe and Mg$_X$Zn$_{1-X}$O to result in a *spike*, the interfacial recombination velocity can be reduced significantly. The Mg$_X$Zn$_{1-X}$O films were deposited by RF Sputtering from a compound target with 99.999% purity. The diameter of the target was 3 inch and the distance between the target and the substrate was 25 cm. For all the samples the Mg composition (X) was 0.23 and deposition was done at room temperature with 10% Oxygen at 5×10^{-3} torr mixed with Argon. To maintain the uniformity of the deposition the substrate holder constantly rotated during the deposition. As mentioned earlier that the MZO and CdTe interface could reduce the interface recombination through the formation of band alignment called "spike", which can help lower the recombination at the interface, hence improving the minority carrier collection.

4.1.3 Window Layer (CdS)

CdS is used in CdS/CdTe solar cells as window layer and the n-type heterojunction partner the pn junction . As CdS has bandgap energy of 2.4 eV, it allows light to pass through it in the visible solar spectrum wavelength greater than 500 nm. Maximum theoretical short circuit current density of CdTe solar cell with CdS is 23 mA/cm^2; however, there is absorption in the short wavelength range for CdS causing to lose equivalent short circuit current density of 8 mA/cm^2 [47]. The carriers which are generated in this layer cannot generate photocurrent due to

recombination centers and low minority carrier lifetime. So there is a window loss in the range of 300 to 500 nm. To reduce this loss pragmatic steps would be to reduce the thickness of CdS as much as possible. Henceforth thickness of CdS is maintained less than 100 nm. However, if the thickness of CdS is too thin then that can cause some adverse effects as well like reducing the V_{OC} and FF. Another problem associated with CdS is the formation of pinholes resulting the formation of micro junctions between CdS and TCO demeriting the cell performances. So, the optimization of CdS thickness is important to get maximum current. In high temperature CdS dissociates into its elements and recombines as a film on the substrate. D. Marinskiy et al. studied the impacts of CdS/CdTe solar cells fabricated the CdS layer with Close Space Sublimation (CSS) and produced highly efficient devices with CSS CdS [49]. To minimize the above discussed losses the thickness of CdS was maintained ~100 nm, the deposition was under He and He+O_2 ambient. Under O_2 ambient the sulfur vacancies are observed to be reduced.

During high deposition temperature or post CdCl$_2$ treatment reaction between CdS and CdTe forms an interfacial layer of $CdS_{(1-X)}Te_X$. It is assumed that due to the formation of this layer the lattice mismatch between CdS and CdTe gets reduced and improves the junction quality [47]. As mentioned the bandgap of CdS is 2.4 eV, the corresponding wavelength is 510 nm. Significant amount of solar spectrum wavelengths lies below the 510 nm, meaning for this poor quality of CdS almost 8 mA/cm^2 current is lost if the thickness of CdS is 500A^0 or thicker [48].

### 4.1.4 CdSe$_{1-x}$Te$_x$ (CST) Layer

Theoretically reduction of bandgap (from 1.45 eV to 1.36 eV) in CdTe materials would increase the photocurrent generation, however there would also be a reduction in open circuit voltage. Incorporating Se in CdTe, where the composition of Se can be varied, resulting a bowing effect of bandgap causing the bandgap of the alloy to be lower than CdTe [50]. For this study

CST was deposited by the CSS deposition technique, under 15 Torr He and 10 Torr O_2 ambient. Samples with 7%, 15%, and 19% Se composition were fabricated. For all the samples the substrate temperature was 580^0C and source temperature was 680^0C. CdTe and CdSe of 99.999% purity were used to prepare the source material. The source was deposited on glass under conditions pre-determnied to result in the compositions listed above. Prior to the CST CST all the samples were annealed at 400^0C for 20 minutes. Due to the reduction of bandgap of the CST alloy there is an enhancement in current collection at longer wavelength of the cells.

4.1.5 Absorber Layer (CdTe)

As mentioned earlier that CdTe is a direct bandgap material with high absorption coefficient, therefore only 2 microns of CdTe is enough to fabricate a solar cell to absorb more than 90% of the incident light. For all the samples the total thickness of CdTe and CST were 4 µm. Several fabricating techniques can be applied to deposit polycrystalline CdTe. Among them the most common are sputtering [50], screen printing [51], metal organic chemical vapor Deposition (MOCVD) [52], electrodeposition [53] [54], and close spaced sublimation (CSS) [55] [56]. Among these methods' CSS has been the most efficient method for CdTe deposition. This deposition method is based on reverse dissociation of CdTe at high temperature. The way it gets dissociated is:

$$2CdTe(s) \leftrightarrow 2\ Cd(g) + Te_2(g)$$
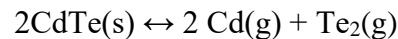
These elements recombine on the surface of the substrate to form the film. Ferekides et. al reported that sublimation of CdTe by CSS has better CdTe film characteristics with larger grains, resulting a lower defect density and shorter grain boundaries [57]. Films fabricated with CSS technique has better quality than Sputtering or Physical vapor deposition, because CSS can produce large crystalline grain size meaning lower concetration of grain boundaryl defects

associated with the film. Many researchers have also suggested that oxygen ambient during the deposition of CdTe with CSS shows better optical and crystalline characteristics. For this study CdTe was deposited in 15 Torr He ambient and 10 Torr O_2 ambient from 99.999% pure CdTe source. For all the samples substrate temperature was 580^0C and source temperature was 680^0C. Deposition time was varied to adjust the thickness of CdTe layer.

4.1.6   CdCl$_2$ Evaporation and Heat Treatment (HT)

One of the most important processing steps for CdTe solar cells is CdCl$_2$ evaporation and post heat treatment (HT). The CdCl$_2$ treatment of CdTe improves the interface of CdTe/CdS through interdiffusion of these two compounds [59], recrystallizing the grain structure by enhancing the size of grains [60], enhancing the minority carrier collection at longer wavelengths [61], increasing minority carrier lifetime by passivating grain boundaries and deep defects [62]. The 99.999% pure CdCl$_2$ was loaded in stainless steel holder. The distance between the samples and the holder was approximately 15 cm. The samples were mounted on quartz tube, and the quartz tube was supported by a frame of stainless steel. During the deposition a high vacuum chamber was always maintained. The thickness of CdCl$_2$ was 12000A^0 and during the deposition the substrates were heated. Thickness was measured with a thickness monitor. After the deposition the samples were heated with 390^0C, 410^0C,420^0C and 430^0C in an ambient of He/O$_2$ for 25 min.

4.1.7   Back Contact

One of the biggest challenges to fabricate CdTe solar cells is to make non-rectifying, low resistance and stable back contact. The electron affinity of CdTe is 4.5 eV and bandgap 1.45 eV, so the work function of this material becomes almost 5.8 eV. The metal which would be used as back contact must have work function greater than p type CdTe to align the metal fermi level and

upper valence band edge with CdTe. However, there is no metal available which has high work function enough to form an ohmic contact with CdTe. Using lower work function metal causes forming Schottky barriers at the back of the device. As result there is always an impedance present for hole transportation. Cu is the most commonly used element in the back contact formation process. It is assumed Cu can increase p type doping near or at the back contact for CdTe cells. However, as it can diffuse through CdTe very easily it is also considered as one of reasons for performance degradation for CdTe solar cells. Cu doped graphite paste helps to create ohmic contact between the back contact and the absorber layer. For this study graphite paste was applied with brush and samples were left for overnight to dry. Then the samples were annealed at 275^0C under He ambient. Due to the presence of Cu two possible mechanisms could appear in the cell: i) a substitutional defect (Cu_{Cd}) or ii) an interstitial defect (Cu_i) could appear. The interstitial defect is a shallow level donor (0.01eV) whereas the substitutional defect is a deep level acceptor (0.15-0.34 eV) [63].

4.2 Characterization Techniques

4.2.1 Current Voltage or JV Measurement

JV measurement was taken using solar simulator calibrated under AM 1.5 condition and the reference was a Si solar cell for calibration. From the JV data open circuit voltage (V_{OC}) and Fill Factor were extracted. A four point probe was used with a keithley 2410 source meter to solve problem of contact resistance and the with a voltage swept from -1.5V to 1.5V current was measured. Then all the data collected in a LabVIEW software, which calculated the V_{OC} and FF of each cell.

4.2.2 Spectral Response

Spectral response (SR) measurements were used to determine the Quantum Efficiency (QE) and Short Circuit Current Density (J_{SC}) of the cell. An Oriel monochromator with a light source of GE400W/120V Quartz lamp was used as the light source and a Si cell was again used for calibration purpose. Both the reference and fabricated samples were measured for 300 to 1000 nm wavelength. . The mathematical equation that calculated the QE is given below

$$\text{QE}_{\text{sample}} = \frac{Device\ Current}{Reference\ Current} \times \text{QE}_{\text{reference}}$$

4.2.3 XRD and AFM

X-ray Powder Diffraction was used to understand the composition of the devices and phase identification of the devices as well. XRD is the one of the most important characterizing techniques that are being applied to understand crystallinity and phase of the material, and can also reveal information about unit cell of the material present in the device. All the crystalline peakkes wewre collected at 2θ angle, in the range of 20^0 to 80^0 angle, and X ray diffraction wavelength maintained at 1.54056 Å. The peak orientation was calculated by using the forula: 2dsinθ= nλ, where, n is a positive integer and λ is the wavelength of incident wave. For crystalline solid the interplanar spacing d can be expressed as : d= a/√h^2+k^2+l^2, where a is the lattice spacing and h,k,l are miller indices, with the help of XRD the CST composition was studied.

4.3 Overview of the CSS System

As the main two layers of the device CdTe and CST were fabricated with CSS, understanding the system is important.. In figure 4.2 a schematic of the CSS is given. The source and sample both can be loaded in the graphite plates or holders. To keep the separation between the source and

substrate graphite spacers were used. The separation between the source and substrate was 2 mm. Thermocouples were used to monitor and control the temperature for the source and substrate. Two 2 kW tungsten halogen lamps were used to heat the graphite holders. There was a gas inlet to introduce the gases for the deposition. Another port was used to evacuate the chamber. There were controllers attached to the system to control the temperature of the two graphite plates.
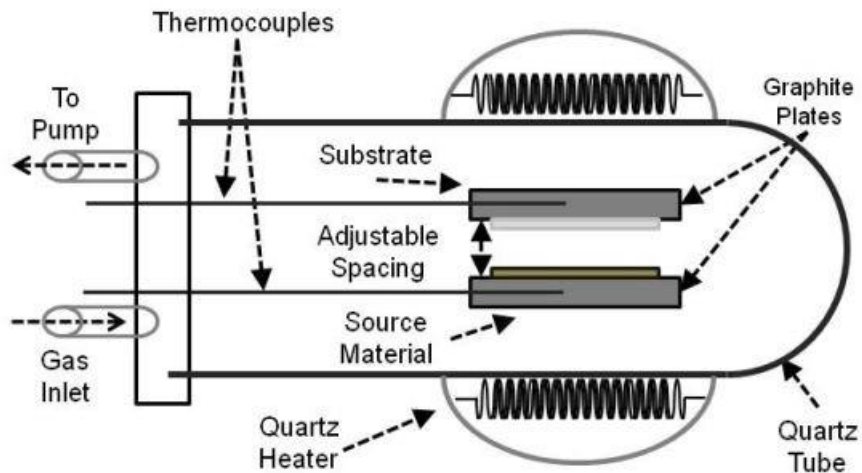

Figure 4.2 Schematic of CSS chamber [57]

CHAPTER 5: RESULTS AND DISCUSSION

5.1   Se Composition in CST Alloy

Alloying CdTe with CdSe causes reduced bandgap of the CST compound (E_g= 1.32- 1.41 ev), which also increases short circuit current density J_{SC} of solar cells, however, it also limits the maximum achievable open circuit voltage V_{OC} [58]. For this study we can see that as the amount of selenium increases in the CST alloy, the short circuit current density improved from 27.44 to 28.54 mA/cm^2 and there is also a reduction of open circuit voltage. It is a clear indication that the results are consistent with the current theory of CdTe/CST solar cells. CST films with three different compositions 7%, 15% and 19% were used. As more Se is incorporated in the CST alloy the V_{OC} decreased from 770 mv to 720 mv.

Table 5.1 Performance of cells with different Se composition

Se Percentage (%)	V_{OC} (mV)	J_{SC} (mA/cm$^{2)}$	FF %	Efficiency %
7	770	27.44	52.3	11.05
15	760	27.90	47.4	10.05
19	720	28.54	51.8	10.06

There is clear indication from figure 5.1 that as the Se composition gets higher so does the short circuit current of the devices. The JV characteristics for the devices in table 5.1 are shown in

Figure 5.1. All devices exhibited a *kink* around VOC. The origin of the kink could be related to the front interface – i.e. MZO/CdTe – or the back contact.
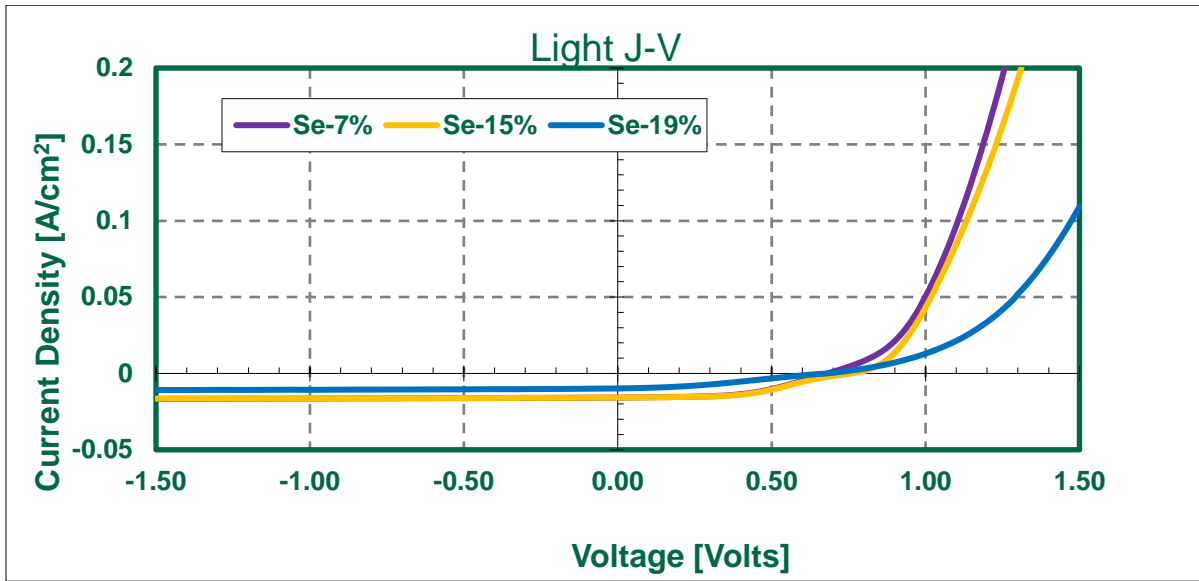
Light J-V

Figure 5.1 Light J-V of different Se composition

It is evident from the SR as the Se composition increases and the bandgap of absorber layer gets smaller, the absorption shifts to longer wavelengths..
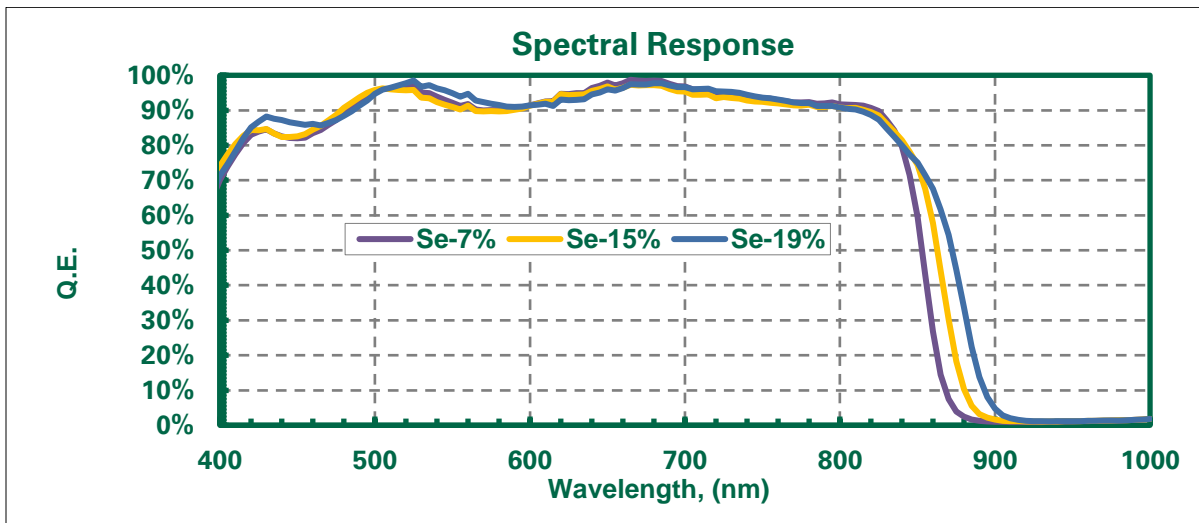
Spectral Response

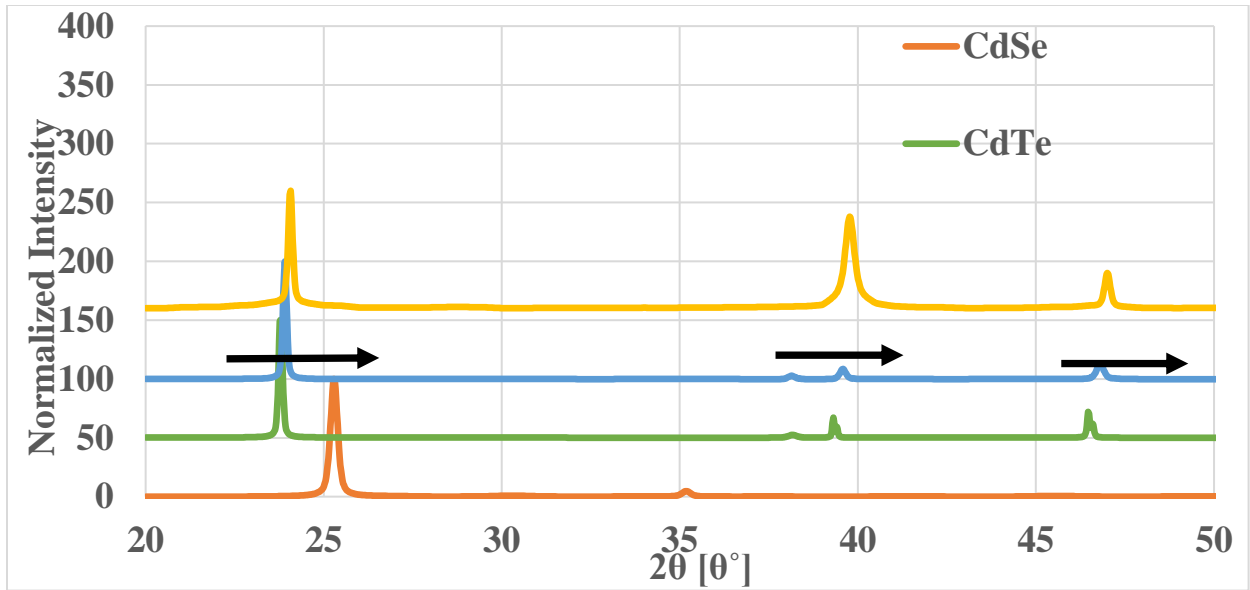Figure 5.2 Spectral response of different Se composition

Figure 5.3 XRD of CdSe, CdTe, and CST

In figure 5.3 it is shown that as the Se composition gets higher the (111) peak shifts towards CdSe. From the width of the peak it is also revealed that the CST has wider peaks than CdTe, suggesting the grain size of CST is smaller than CdTe.
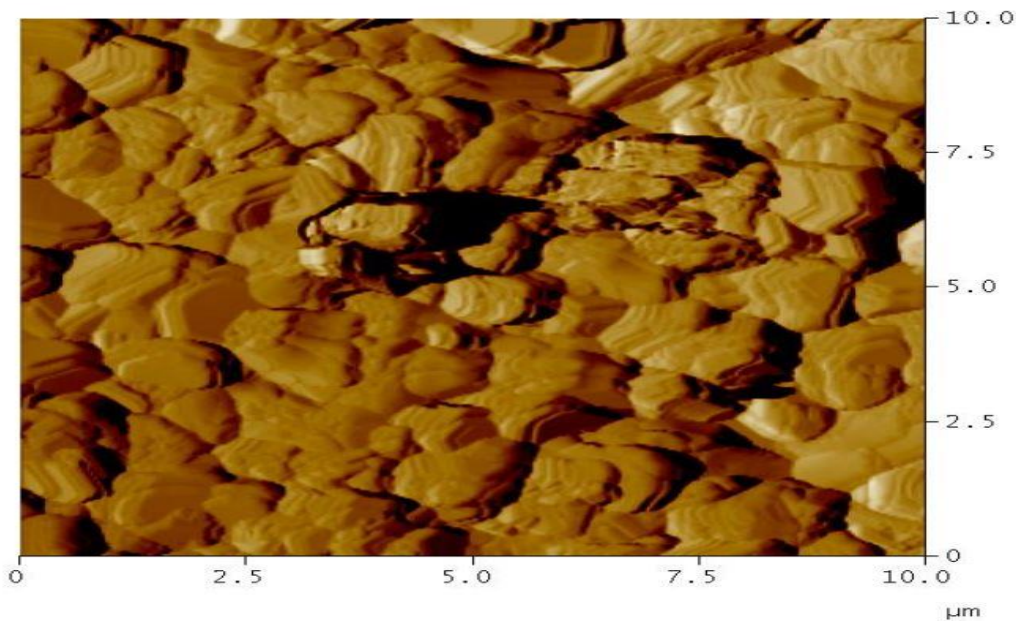

Figure 5.4 2D image of 19% CST from AFM

One of the advantages of CSS system is controlling the grain size of the deposited films [59]. Figure 5.4 reveals the grain size of 19% CST, the garin size is just above 1 µm. The figure also shows that the grains are also very comapct. The 3D imgae of the same film in figure 5.5 suggests uniform deposition.

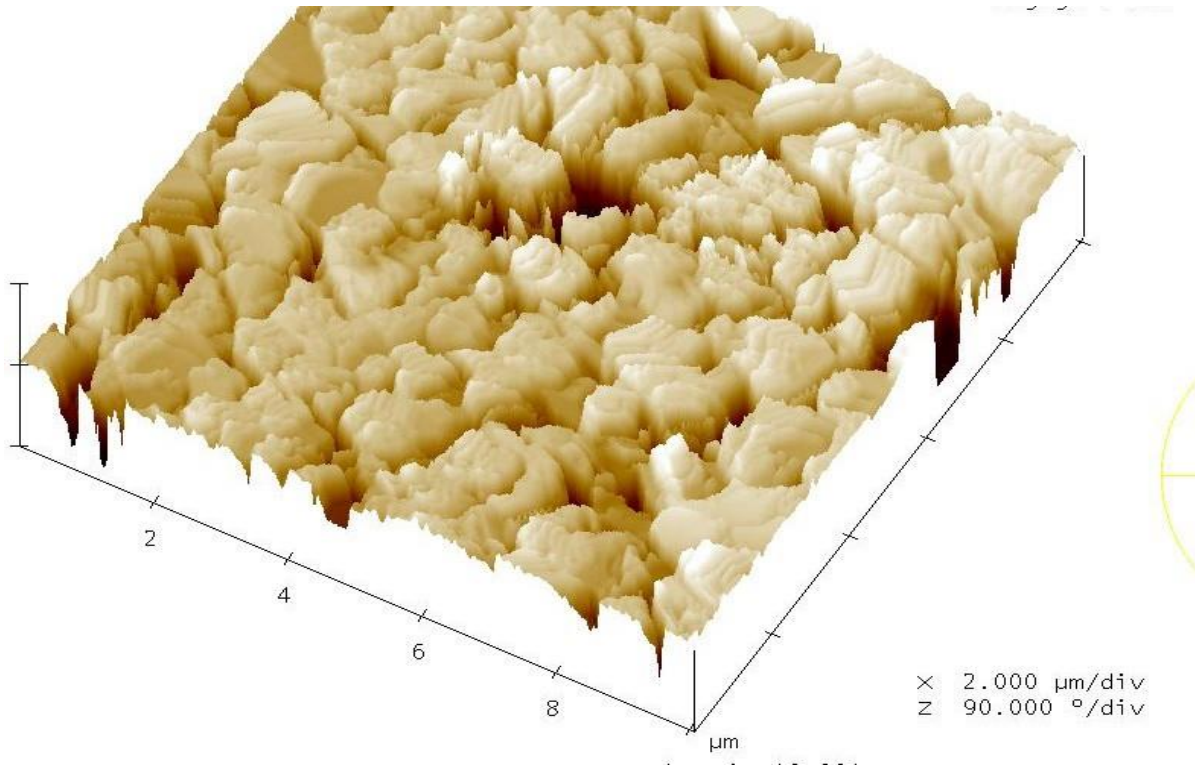Figure 5.5 3D image of CST from AFM

5.2 CdCl$_2$ Heat Treatment

After the CdCl$_2$ evaporation, all the cells went through post heat treatment or annealing. The four annealing temperatures were 390^0 C, 410^0 C, 420^0C, and 430^0C. The duration of the post heat treatment was 25 minutes. At temperatures above 420^0 C cell performance started to degrade. The reason for this could be from excessive interdiffusion of CdTe/CdS/MZO junction. Other research groups have also suggested delamination and loss of adhesion as the cause of lower performance [60].
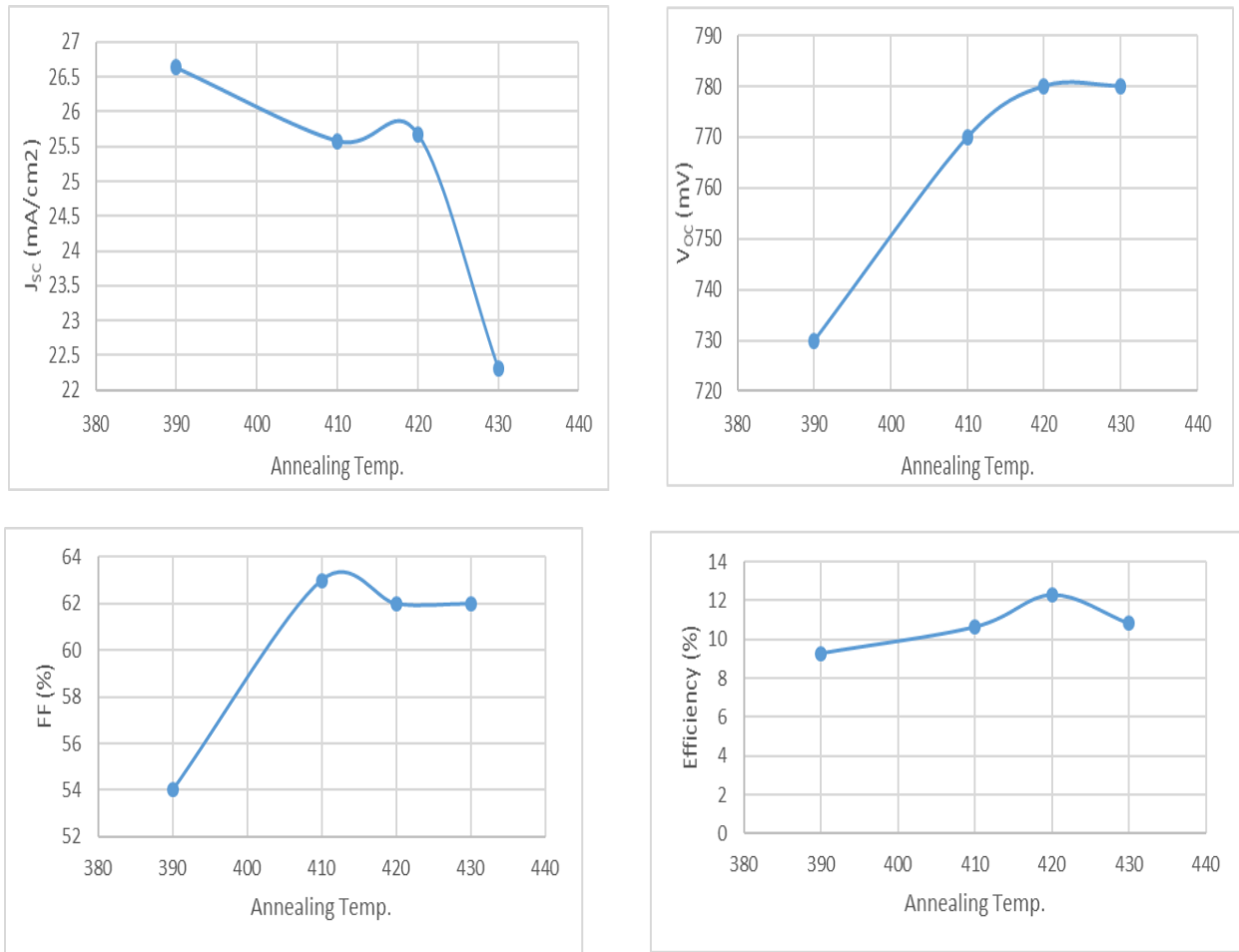
Figure 5.6 J_{SC} & V_{OC} (top) and FF & efficiency (bottom) with respect to annealing temperature

Though for annealing temperature 420^0C and 430^0C had the same open circuit voltage but the short current was higher in case of 1 µm CST. Better performance at higher annealing temperature suggests chlorine passivation is more effective at higher temperature. This could be either because of better recrystallization causing larger grains or smaller grain boundary volume or increased chlorine has diffused in the grain boundaries. At 430^0C performance starts to degrade potentially because of excessive chlorine incorporation, and/or junction damage. .

5.3   Thickness of the CST Alloy

After choosing the best composition and $CdCl_2$ annealing temperature the thickness of the CST alloy was varied to determine its impact. The four CST thicknesses were 0.5 µm, 1 µm, 2

µm and 3 µm. As the thickness of CST alloy gets greater than 1 µm the open circuit voltage of the cells starts to degrade. For 0.5 micron CST though V_{OC} is maximum, however, the J_{SC} is comparatively low due to insufficient amount of Se. As in figure 5.7 it is projected that as the Se composition increases so does the J_{SC}, this is due to increased carrier generation in longer wavelength range.
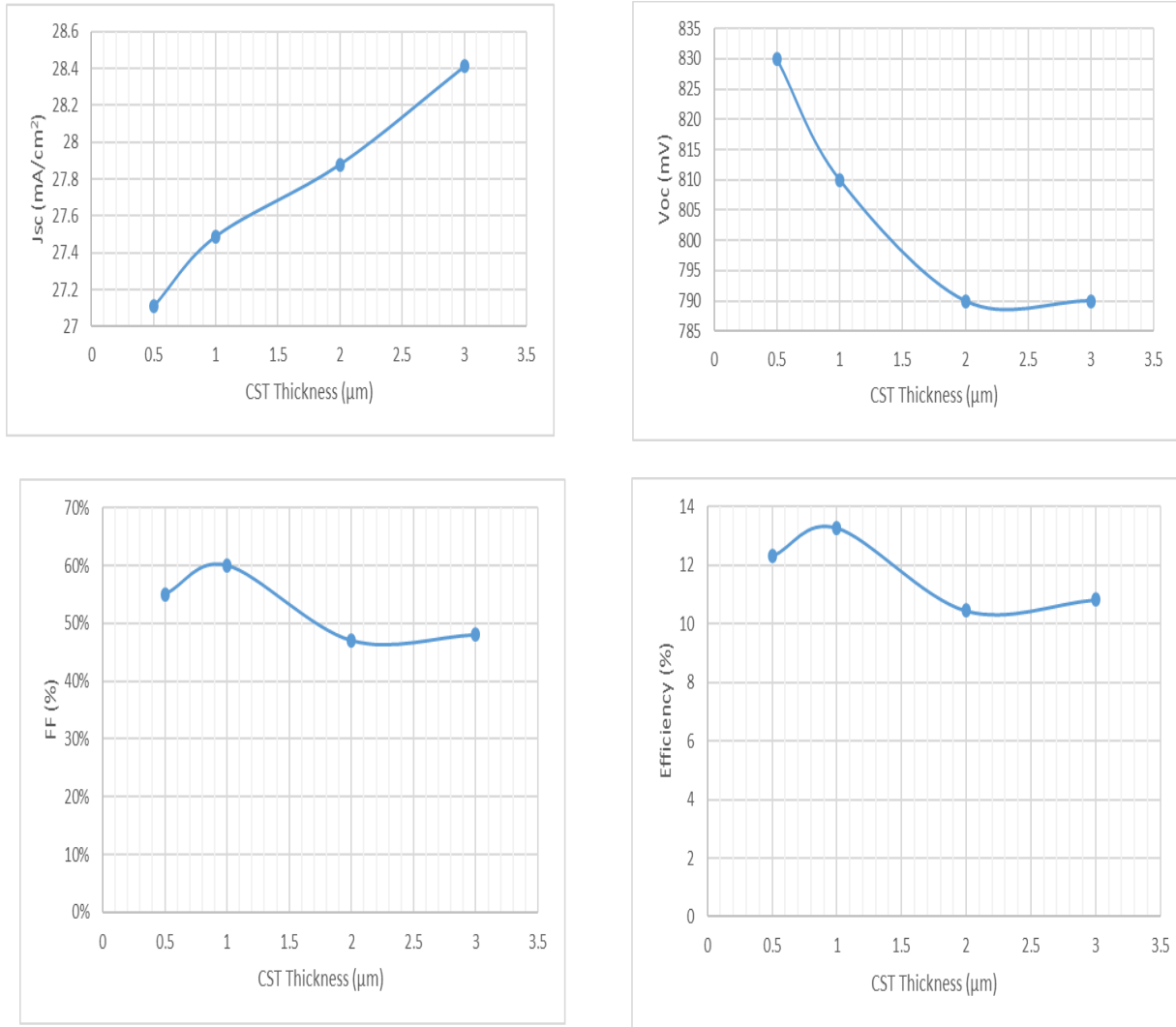
Figure 5.7 J_{SC} & V_{OC} (top) and FF & efficiency (bottom) with varied CST thickness

It is evident from the above results that 1 µm CST resulted in the best efficiency as an optimum between the increase in the current and decrease in voltage was achieved. The best efficiency was13.27%..

Table 5.2 Best cell performance

CST Thickness	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF (%)	Efficiency (%)
1	810	27.11	60	13.27
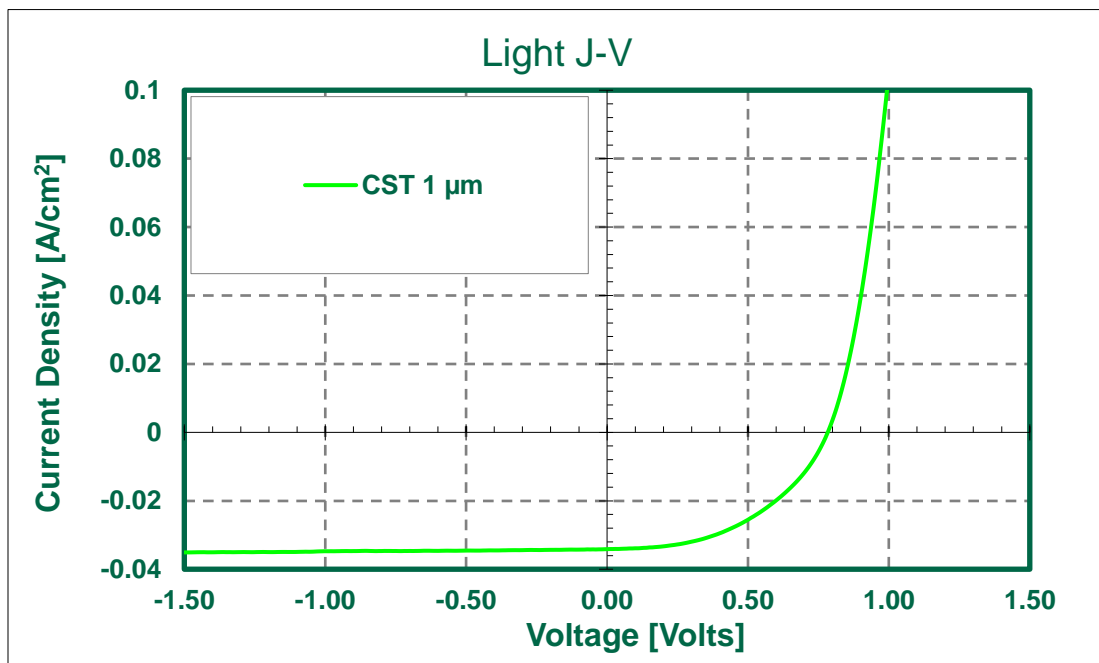
Figure 5.8 Light J-V for 1 µm CST
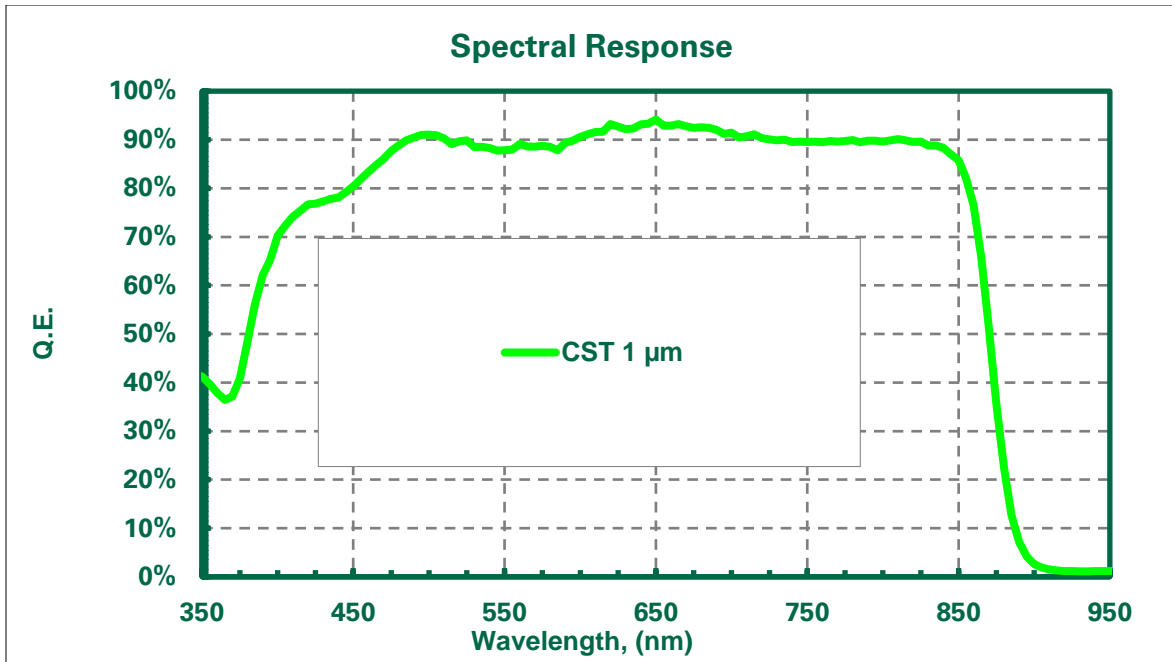
Spectral Response

Figure 5.9 Spectral response for 1 µm CST

The 1 µm CST showed better performance than all the other cells. It showed absorption beyond 900 nm wavelengths and improved absorption in short wavelengths as well due to very thin CdS. The J-V curve showed better shunt resistance and lower series resistance compared to the other cells. Hence, the efficiency reached more than 13.27%. So from the above analysis it is evident that the best cell condition for this study is 1 µm CST thickness with 19% Se composition with 420^0C CdCl$_2$ annealing temperature.

CHAPTER 6: CONCLUSION AND FUTURE PROSPECT

6.1 Conclusion

The effect of Se on CdTe solar cells with different Se composition and thickness was investigated in this work. For that purpose, bandgap engineering was employed to form $CdSe_{1-x}Te_X$ alloy. The composition of Se was varied with 7%, 15%, and 19%. The effect of $CdCl_2$ annealing was investigated for four different temperatures 390^0C, 410^0C, 420^0C, and 430^0C. Then the thickness of the CST alloy was also investigated with four different thicknesses 0.5 µm, 1 µm, 2µm, and 3 µm.   As the amount of Se increased the short circuit current density J_{SC} increased due to bandgap reduction in the absorber layer. However, there is an optimum level of Se that can be incorporated in the cell, otherwise the open circuit voltage V_{OC} would decrease significantly.. The $CdCl_2$ heat treatment played an important role in achieving higher performance of the cell, as it improved the crystallinity of the absorber material throughout the absorber thickness. Devices showed a graded Se profile which was treated at 420^0C, suggesting that the Se profile also could be adjusted using different $CdCl_2$ heat treatment.   The best cell performance was found to be the 19% Se with 1 µm CST thickness with the efficiency 13.27%.

6.2 Future Prospect

As the theoretical limit for short circuit current density is approaching the limit, and the theoretical limit for open circuit voltage is lagging, there is much scope to work with the open circuit voltage. To improve the open circuit voltage a grain boundary study would be a good topic for future research. Along with this, doping of the absorber layer is a challenging task. Doping

would improve the minority carrier lifetime. An investigation on back contact to form ohmic

contact with the absorber layer is also an important issue to look after.

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APPENDIX A: LIST OF ACRONYMS

A.1 List of Acronyms

CB- Conduction Band

CdTe- Cadmium Telluride

CSS- Closed Space Sublimation

CST- Cadmium Selenide Telluride

FF- Fill Factor

GB- Grain Boundary

JV- Current- Voltage Density

J_{SC}- Short Circuit Current Density

PV- Photovoltaic

QE- Quantum Efficiency

SR- Spectral Response
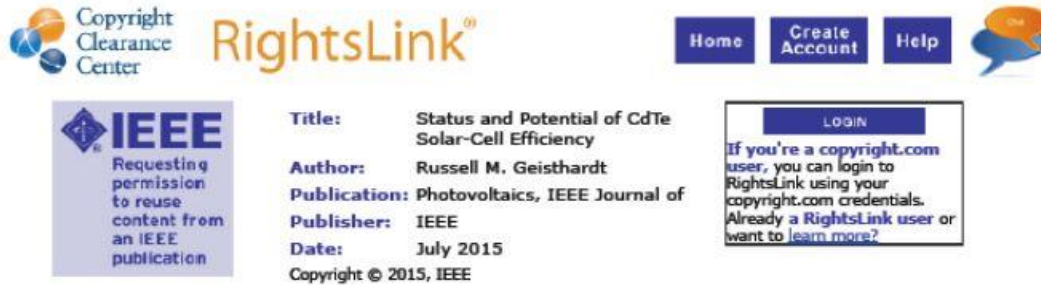
TFSC- Thin Film Solar Cell

UHP- Ultra High Purity

USF- University of South Florida

VB- Valence Band

V_{OC}- Open Circuit Voltage

APPENDIX B: PERMISSION FOR FIGURES

B.1   Permission for Figure 2.3

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