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Effect of Heat Treatments and Reduced Absorber Layer Thickness on Cu(In,Ga)Se2 Thin Film Solar Cells

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Effect of Heat Treatments and Reduced Absorber Layer Thickness on $Cu(In,Ga)Se_2$ Thin Film Solar Cells

by

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DEDICATION

To my parents and sister

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ABSTRACT

Thin film solar cells with Copper Indium Gallium Diselenide ($Cu(In,Ga)Se_2$) absorber layers is one of the most promising candidates to emerge as an efficient solar cell technology in the near future. CIGS cells with efficiencies of 19.2 % have already been reported [1]. In this study, CIGS absorber layers are fabricated by a two-stage all-solid-state manufacture-friendly process. In the first stage, designated as precursor deposition, Copper and Gallium are sequentially deposited followed by co-deposition of Indium and Selenium. In the second stage, designated as selenization, the substrate is annealed at high temperatures in a selenium environment during which a thin layer of copper is also deposited. The typical thickness of the absorber layers fabricated by this process is around 2μm. The ZnO transparent front contact of these cells is a bi-layer with a thin intrinsic layer and a thicker Al doped n-type layer. These layers have been fabricated by different methods using Al-doped and undoped ZnO targets. The effect of the intrinsic layer thickness on the device performance was studied. Best performances were obtained when the intrinsic layer was around 350 Å thick and fabricated from an Al-doped ZnO target with excess oxygen partial pressure during deposition.

The main focus of this work is to reduce the thickness of the CIGS absorber layers with no or minor loss in efficiency as this would translate directly into reduction in production costs and the amount of material being used. Reducing the thickness can be done either by reducing the deposition rates or duration of deposition. Due to the complex time-

temperature profile during fabrication, reducing the thickness by reducing the deposition time would also affect the duration for which the substrates will be at high temperatures. To understand what effect this would have in film formation and performance of the device, and if any post-deposition annealing would be required to compensate for the reduced time at temperatures, experiments were carried out with the cells being annealed at different stages before and after completion of the device itself. Annealing was done at 250°C in both air and vacuum. Although annealing the finished devices always yielded poorer performance, it was certainly helpful in understanding which aspects of the device were affected.

Devices with reduced absorber layer thicknesses of 1.5µm, 1.0µm and 0.65µm were fabricated. The devices showed improved V_{oc}'s when the absorber layer thickness was reduced to 1.5µm and 1.0µm but the J_{sc}'s dropped by 2-3 mA/cm^2. The 1.0µm thick devices also showed an increase in band gap. The thickness of the Molybdenum back contact layer was increased to see if the amount of Sodium from the substrate had any effect on the device performance. The Ga/In ratio was altered and its effect was also studied. The 0.65µm thick devices showed a large reduction in V_{oc}'s and J_{sc}'s. The effect of Selenization time and Selenium flux during Selenization were studied at each of the different thicknesses.

CHAPTER 1

INTRODUCTION

We use energy every day in different forms, such as light, heat, and electricity. Most of our energy supply comes from coal, oil, natural gas, or radioactive elements. They are considered non-renewable because once they are removed from the ground and used, they are not immediately replaced. In fact, the world's natural gas, crude oil and coal deposits took millions of years to form. Uranium, which is used for nuclear energy, has limited supply as well. Humans will have used up most of these deposits in less than 200 years. Once they are gone, non-renewable energy supplies cannot be replaced within human time scales.

1.1 Renewable Energy

Renewable energy on the other hand quickly replaces itself and is usually available in a never-ending supply. Renewable energy comes from the natural flow of sunlight, wind, or water around the Earth. With the help of special collectors, we can capture some of this energy and put it to use in our homes and businesses. As long as sunlight, water and wind continue to flow, we have access to a ready supply of energy.

1.2 Importance of Renewable Energy

In the last three years, we have seen large fluctuations in the cost of natural gas, oil, and electricity due to global economics, market deregulation, and political events in some parts of the world. Renewable energy is not subject to sharp price changes because it comes from sources such as sunshine, flowing water, wind, and biological waste, all of which are free. This gives people greater certainty about the cost of energy, which is

good for the society and economy. By comparison, fossil fuels are limited in their supply, and their price will increase as they become scarcer.

Air pollution is a major problem in many cities around the world. The biggest cause of air pollution in cities is the burning of fossil fuels, including fuels used for transportation. The great advantage of using renewable energy in place of fossil fuels is that renewable energy adds very few pollutants to the environment. Renewable energy is considered "clean" and "green."

Renewable energy supplies will never run out. While the supplies of coal, oil, and natural gas are limited, sunshine, wind, biomass, and water power are considered almost limitless resources.

Renewable energy sources include biomass, geothermal energy, hydropower, solar energy, and wind energy. They are called renewable energy sources because they are replenished in a short time. Day after day, the sun shines, the wind blows, and the rivers flow. We use renewable energy sources mainly to make electricity.

1.3 Solar Energy

For billions of years, the sun has poured out huge amounts of energy in several forms, including light, heat, radio waves, and even x-rays. The earth, in orbit around the sun, intercepts a very small part of the sun's immense output. On Earth, direct sunlight is available from sunrise until sunset, except during solar eclipses. Solar collectors and modules are designed to capture some of the sun's energy and change it from radiation into more usable forms such as heat or electricity. In fact, sunlight is an excellent source of heat and electricity, the two most important forms of energy we consume. Solar energy is becoming increasingly popular for remote power needs such as telecommunication towers, agricultural applications (irrigation and pasture management) in tropical countries that are not connected to an electrical grid, for heating swimming pools, and many other applications around the world. The simplest photovoltaic cells power watches, calculators

and the like, while more complex systems can light houses and provide power to the electrical grid.

1.4 Photovoltaics

In 1839, Edmond Becquerel discovered the process of using sunlight to produce electric current in a solid material. But it took more than a century to truly understand this process. Scientists eventually learned that the photoelectric or photovoltaic (PV) effect caused certain materials to convert light energy into electrical energy at the atomic level.

The photoelectric effect is the basic physical process by which a PV cell converts sunlight into electricity. When light shines on a PV cell, it may be reflected, absorbed, or pass right through. But only the absorbed light generates electricity. Photovoltaics is a semiconductor technology that silently converts light energy into direct-current (DC) electricity, with no moving parts, burning no fuel, and creating no pollution. This can be used directly or converted into AC, and it can be stored for later use.

1.5 Solar Cell Materials

Solar cells can be fabricated with many different materials. Crystalline silicon was the material used in the first successful devices and is still the most widely used. However, to be used efficiently in solar cells, silicon needs to be refined to 99.9999% purity. Although Silicon solar cells have produced high efficiencies, high processing costs make it unsuitable for large scale requirements. Moreover, because silicon is an indirect band-gap material, larger thickness is needed to absorb the incident sunlight. Because of these drawbacks associated with silicon, the PV industry started looking for alternative absorber materials processing technologies. Thin-film technology is one of the promising candidates because of the following advantages. Thin-films use much less material. The thickness of the absorbers used in thin-film solar cells is usually 1 to10 micrometers which is very thin when compared to the 100 to 300 micrometers needed for silicon. Thin-films can be fabricated with much lower processing costs. Thin film photovoltaic

cells can be attached to an inexpensive backing such as glass, flexible plastic, or stainless steel.

Semiconductor materials for use in thin films include amorphous silicon, copper indium diselenide (CIS), and cadmium telluride (CdTe). Amorphous silicon has no crystal structure and is gradually degraded by exposure to light. Figure 1.1 [29] shows the absorption coefficient for various semiconductor materials. Copper Indium Diselenide ($CuInSe_2$ or CIS) has an extremely high absorptivity, which means that 99% of the light shining on CIS will be absorbed in the first micrometer of the material. Adding small amounts of gallium to the CIS layer boosts its bandgap from its normal 1.0 eV to up to 1.7 eV, which improves the theoretical the efficiency of the device. This particular variation is commonly called a Copper Indium Gallium Diselenide or CIGS cell.

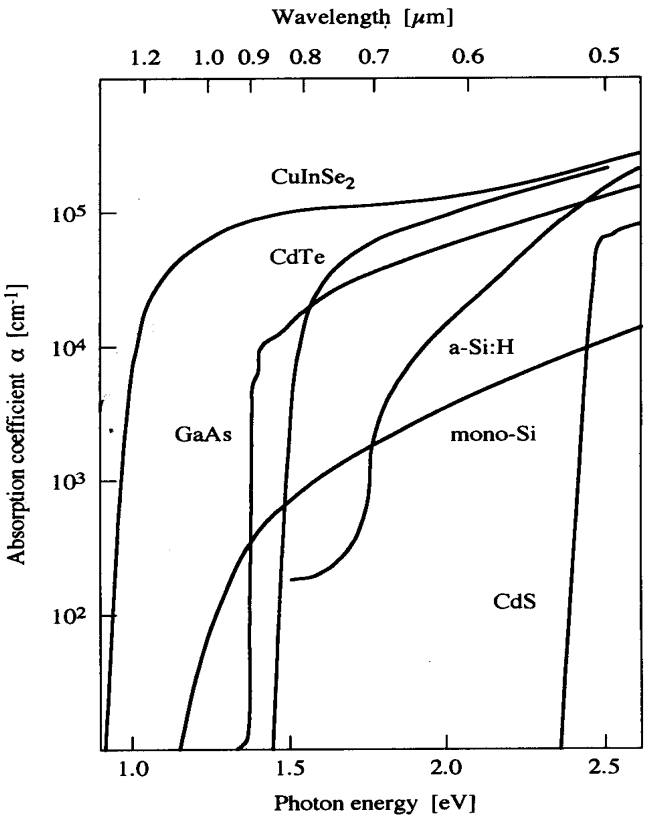

Figure 1.1: Absorption Coefficients of Various Semiconductor Materials

CHAPTER 2

SOLAR CELL DEVICE PHYSICS

A solar cell is a semiconductor device that converts sunlight directly into electricity. In essence, a solar cell is a p-n junction where a p-type material is brought in contact with an n-type material. Contacts which are either metallic or transparent are used to collect the carriers from the p-n junction. In photovoltaic cells, semiconductors have two properties that are most important for the cell to produce electricity.

1. Electrons, which are the constituents of electricity, are freed in a semiconductor when photons of sufficient energy are absorbed within them.

2. When two different semiconductors are joined at a common boundary, a fixed electric field is usually induced across that boundary.

2.1 Semiconductor Basics

Most semiconductors have very well ordered atomic structures called crystal lattices. In their most perfect form, such ordered semiconductors are said to be single crystals. In PV, we often deal with multi-element crystals – compound semiconductors made of more than one element. One example is Cadmium Telluride (CdTe), which is made of equal amounts of cadmium and tellurium. Many, more-complex shapes are also possible. We may have three atoms – such as in the PV semiconductor, Copper Indium Diselenide (CIS).

Because its atoms are so well ordered, a single-crystal structure is the most perfect form of a semiconductor. Unfortunately, making single crystals can sometimes be too costly to be practically used in PV, where cost is a very important element. On the other hand,

many of the properties of single crystals are maintained in materials that are less than perfect and cost much less to make.

Within ordered semiconductors, electrons have very well-defined roles. Each atom can have numerous electrons. Some of these electrons are tightly held by the nucleus and do not play much of a role in the material's chemistry. The outer electrons; away from the nucleus have a key role in holding the semiconductor lattice together and in the material's electronic properties. These outer electrons are called valence electrons.

In general, an element's incomplete outer shell (of electrons) plays the important role in its chemistry. In fact, these outer electrons are the basis of the chemical bonding that holds lattices together. Atoms are most stable when they have a complete outer shell of electrons. Each outer shell is complete when it has eight electrons. Two or more atoms with incomplete outer shells can bond to each other although they are individually electrically neutral.

At low temperatures, electrons in a crystal occupy the lowest possible energy states. According to Pauli's exclusion principle, each allowed energy state can be occupied by, at most, two electrons, each of opposite spin. Hence, at low temperatures, all available states in a crystal up to a certain energy level will be occupied by two electrons. This energy level is called the Fermi level (E_f) [28].

At room temperature, semiconductors have an electronic structure with one band of allowed states virtually completely occupied by electrons (the valence band) that is separated by a forbidden energy gap (E_g) from the next band of allowed states, which is virtually devoid of electrons (the conduction band). At higher temperatures, some levels in the originally completely filled valence band are now vacant and some in the next highest band; the conduction band, are occupied. Current flow in a semiconductor is due to both motion of electrons in the conduction band and the effective motion of vacancies or holes in the valence band. Semiconductors can be divided into direct and indirect band-gap types, depending on the form of the relationship between the energy of electrons in the conduction band and their crystal momentum.

2.2 n and p Type Conductivity

A material with conductivity in between highly conductive metals and highly resistive insulators is called a semiconductor. In a semiconductor material at room temperature, the shared outer electrons of the lattice are well bound to each other, but have a small probability of picking up enough heat to break loose. But at high temperatures, there is a higher probability of an electron gaining enough extra vibrational energy to slip free.

But our interest is in the behavior of these materials near room temperature. At these temperatures, a small fraction of electrons can accidentally gain enough energy to break free. They are called conduction band electrons. The place in the lattice from which they emerged is called a hole – the absence of a needed electron. Each electron (and hole) can move freely for a very long time without encountering a hole (electron) with which they recombine. This period of free movement is called a free-carrier lifetime. This number of free electrons and holes created by heat is a very small fraction of the total number of bound outer electrons. A material with this few free carriers is not much different from an insulator.

Impurity atoms can be used in semiconductors to alter their electronic properties in favorable ways. The kind of impurities that we are interested in are those with one electron more or less than that in the actual material. Such a semiconductor with extra electrons is called n-type because it is dominated by free negative charges, electrons. The impurity atoms that are introduced to add the extra electrons are called donors, because they donate a free electron to the conduction band. A vast majority of these donors will be ionized. So, the total number of electrons in the conduction band can be approximated to the number of donor impurity atoms N_D.

p-type semiconductors also exist; they are dominated by holes – positive free charges. p-type semiconductors are created when impurities with one fewer outer electron are introduced in the lattice. Since the impurity that adds extra free holes to the lattice accepts a nearby electron to create the free hole, such an impurity is called an acceptor. The hole concentration can be approximated to the number of acceptor atoms N_A. Together, they

are called dopants, in the sense that their introduction in a relatively pure material alters its electronic properties.

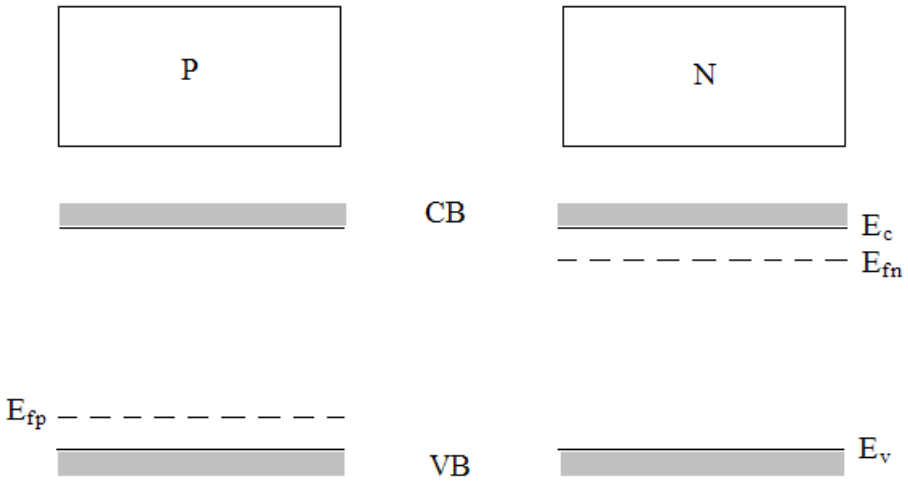

Figure 2.1: p-type and n-type Semiconductors with Corresponding Energy-band Diagrams

In intrinsic semiconductors, the Fermi level (E_f) is in the middle of the bandgap. In n-type doped semiconductors, the Fermi level is shifted towards the conduction band E_c and in p-type doped semiconductors, the Fermi level moves towards the valence band E_v. Figure 2.1 shows the energy band diagrams of isolated n and p type materials. The position of the Fermi levels can be determined from the equations given below.

For n-type, $E_{fn} - E_c = kT/q \ln (N_D/N_C)$

For p-type, $E_v - E_{fp} = kT/q \ln (N_A/N_V)$

where k is the Boltzmann constant, T is the absolute temperature, E_{fn} and E_{fp} are the Fermi levels, E_c is the energy level at the bottom of the conduction band, E_v is the energy level at the top of the valence band, N_C and N_V are the effective density of states in the conduction and valence band respectively, N_D and N_A are the donor and acceptor concentrations respectively.

2.3 The Built-In Electric Field

It is important to note that both n-type and p-type semiconductors are electrically neutral. There are no more electrons than protons in either of them. Yet one can have a million-billion free electrons per cubic centimeter and very few holes; the other a million-billion free holes and very few electrons. But charge neutrality remains unbroken in both conditions.

If we let n- and p-type semiconductors share a common boundary, free electrons from the n-side diffuse across the boundary and settle in bonds on the p-side. This changes the charge neutrality in both the materials. As an electron crosses, it leaves behind a positive charge and as it settles into place, it adds a negative bias to the p-side. In a narrow region on both sides of the interface between the two materials, an electric field builds up. Each new electron that would pass from the n-type side to fill an incomplete bond on the p-side finds it harder to climb the growing electric field. Finally, equilibrium is reached, and the

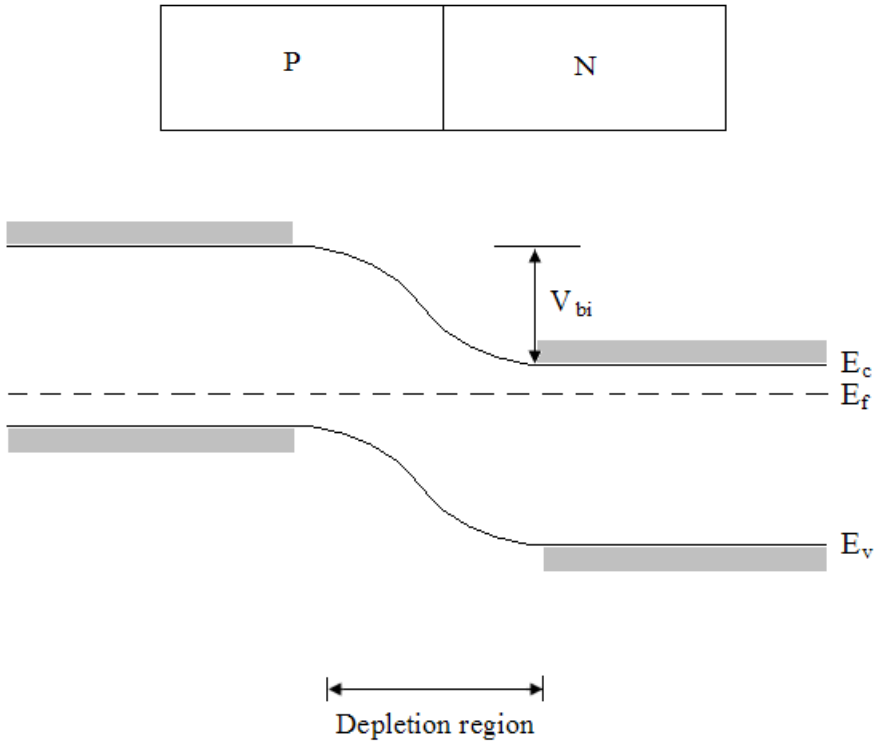

Figure 2.2: Energy-band Diagram of a p-n Junction at Thermal Equilibrium

net charge movement stops. Although the bulk of the n-type material (away from the electric field) still teems with electrons, and the p-type side still teems with holes, the electric field at their interface forms a barrier keeping them apart.

The area of the field is called the depletion region because in that region there are no free carriers – all are either in bonds or swept away by the field. Far enough from the metallurgical junction, the conditions would remain unperturbed from those in the isolated materials. But, in the depletion region near the junction, a potential difference exists which is called the built-in potential, V_{bi}.

$V_{bi} = kT/q \ln (N_A N_D / n_i^2)$

Where n_i is the intrinsic carrier density

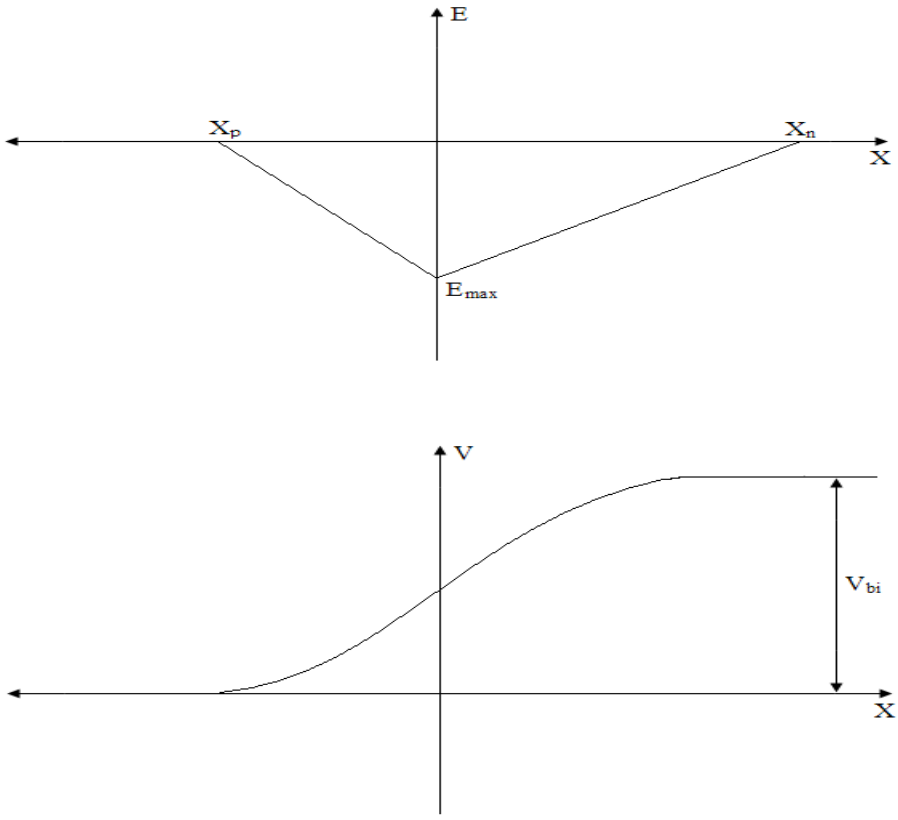

Figure 2.3: Electric Field and Potential Distribution of an Abrupt p-n Junction

The electric field in the depletion region is quite strong, capable of accelerating electric charges that pass through it to very high velocities [30]. The electric field and potential distribution across the depletion region are shown in figure 2.3.

2.4 Heterojunctions

A heterojunction is a junction formed between two different semiconductor materials. Based on whether the type of conductivity for both the materials is the same or different, heterojunctions can be classified as isotype or anisotype respectively. Heterojunctions have been extensively studied and used in applications like photo detectors, light emitting diode, and solar cells [27]. The two materials forming the heterojunction have different bandgaps E_g, different permitivities ε, different work functions Φ_m and different electron affinities χ as shown in figure 2.4. When a junction is formed between these two materials, the Fermi level on both sides of the junction should coincide in equilibrium.

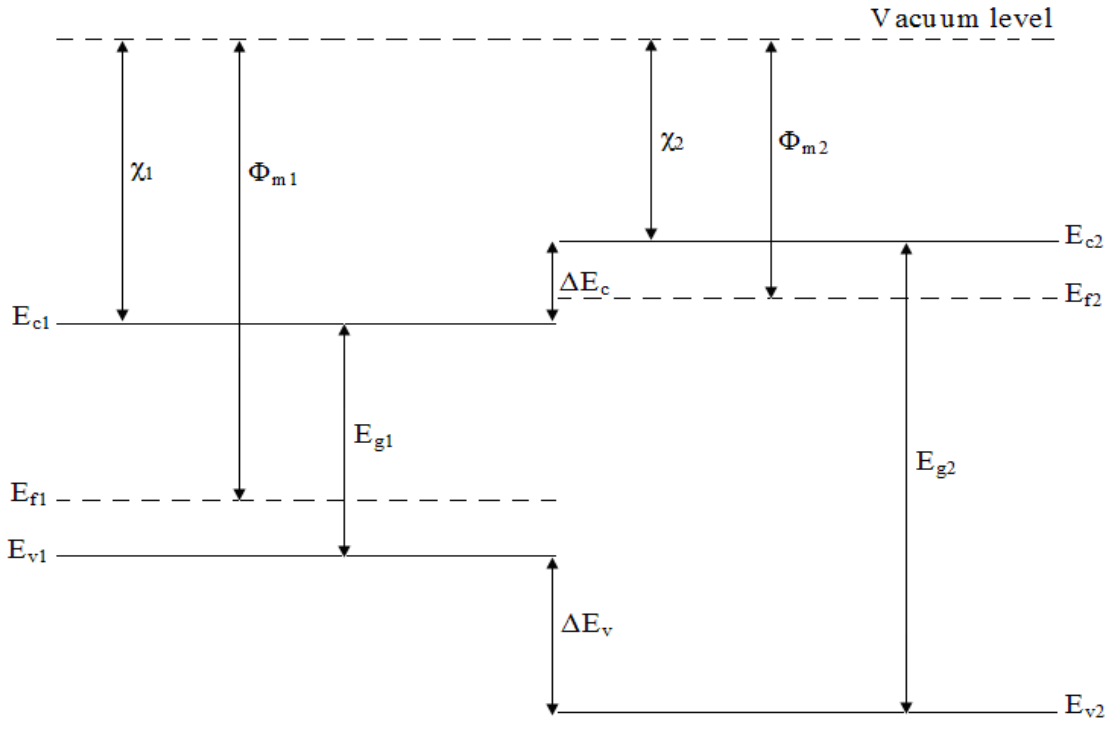

Figure 2.4: Energy-Band Diagram for Two Isolated Semiconductors in which Space-Charge Neutrality is assumed to Exist in Each Region

This leads to discontinuities in the conduction and valence band edges. These discontinuities can be very large and can have an adverse effect on the current flow since they act as barriers to the mobile charge carriers.

From figure 2.5, we can see a spike in the conduction band which is called as the conduction band offset. This offset acts as a barrier to the electron flow from the p-side to the n-side of the junction when it is illuminated. Similar to the conduction band offset, there can be a valence band offset too. Heterojunctions also suffer from lattice mismatches and differences in electron affinities which cause interface states at the junction which act as recombination centers. In order to obtain maximum performance from the device, these offsets and mismatches have to be minimized. The factors that

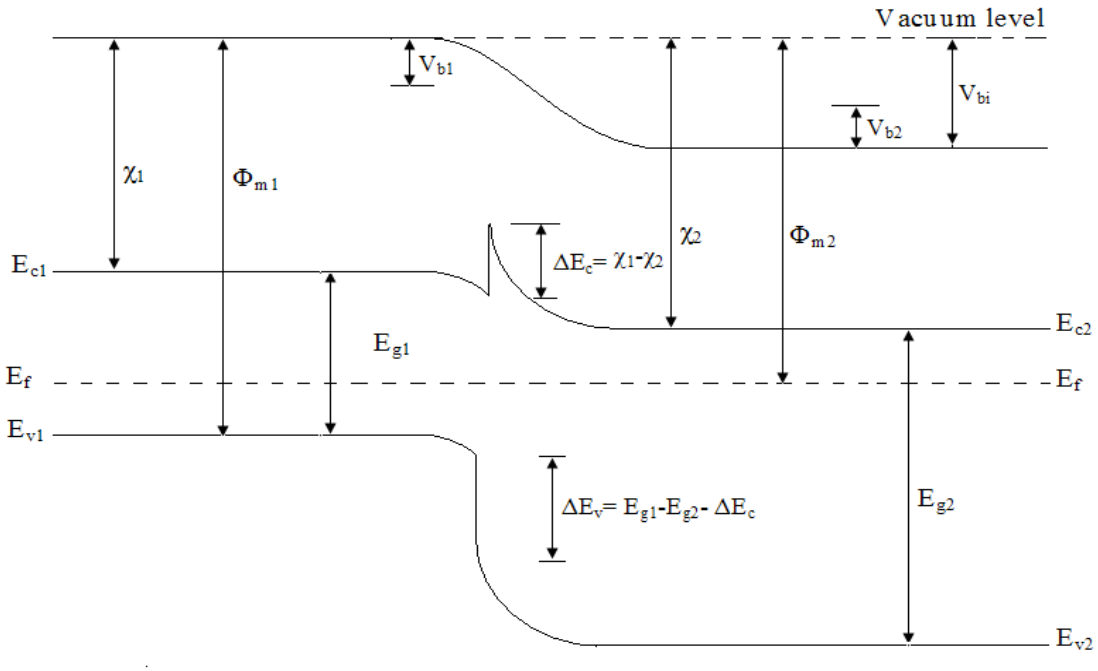

Figure 2.5: Energy-Band Diagram of an Ideal p-n Anisotype Heterojunction at Thermal Equilibrium

govern the mismatches are primarily inherent properties of the semiconductor material itself. Hence, proper selection of materials for the device plays a vital role in its performance. The Cu(In,Ga)Se_2 / CdS solar cell, which is the subject of study here, is a anisotype heterojunction.

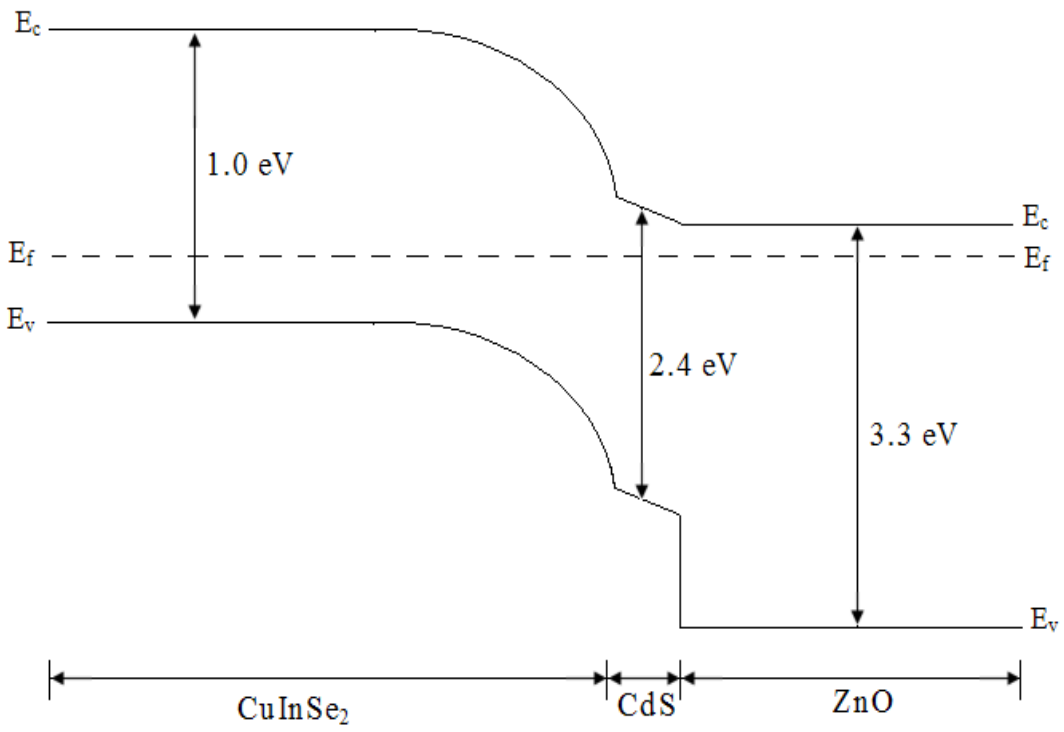

Figure 2.6: Energy-Band Diagram of a $CuInSe_2$/CdS/ZnO Heterojunction Solar Cell

The energy band diagram of a $CuInSe_2$ / CdS / ZnO heterojunction solar cell is shown in figure 2.6. ZnO is the front transparent contact. Because of its high band gap, almost all the light passes through to the underlying layers. Most of the incident light passes through the wider band-gap window layer CdS and is absorbed in the lower band-gap $CuInSe_2$ layer.

2.5 Working of a Solar Cell

Diodes are very familiar solid-state devices used in everything from clocks to stereos to battleships. If used in a circuit, it would let current flow easily in one direction and prevent it from flowing in the opposite direction. PV devices are not exotic - they are simply light driven diodes. As we know, photons of sufficient energy absorbed in a semiconductor can free electrons from a bond in the lattice. This process is called the formation of an electron-hole pair, because a free hole is created at the same time as a free electron.

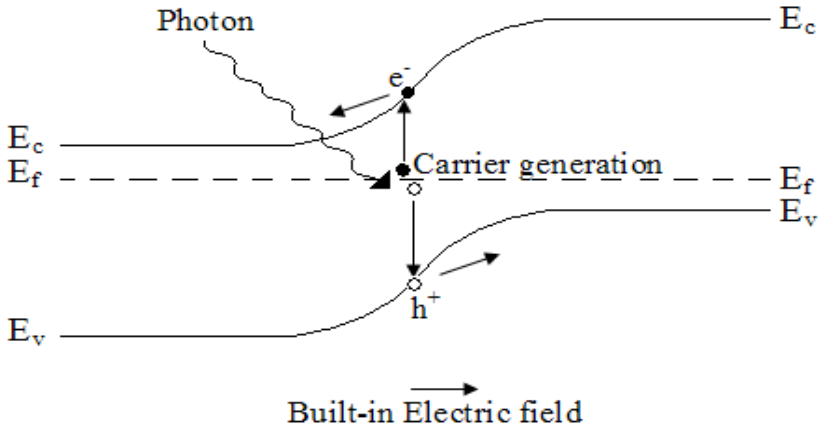

Figure 2.7: Conceptual Working of a p-n Junction Solar Cell

Suppose this electron-hole pair were formed in the p-type side of the junction. The p-type side has many free holes in it already, but almost no free electrons. The new light generated electron would have only a short time to move around randomly before it would fall back into one of the numerous holes on the p-type side. However, in that short time, the electron might encounter the built-in electric field. The electric field opposes electrons flowing from the n-type region to the p-type region. On the other hand, it favors electrons moving from the p-type region to the n-type one. Hence, if the free electron on the p-type side encounters the electric field, it will be driven across the interface to the other side. An analogous process occurs on the other side of the cell. The built-in electric field works in a symmetrical manner to propel electrons from the p-type side into the n-type side; and to propel holes from the n-type side into the p-type side. In effect, it separates the light-generated free charges (holes and electrons) formed within the n-type or p-type region of the cell.

2.6 Placing the Electric Field

A semiconductor's absorption length is the critical parameter controlling PV device design. The key action in a PV device is the separation of electrons and holes by a built-in field, and for this to happen, the light generated minority carriers have to be near enough to the built-in field for the field's influence to send them to the other side of the

PV device. The proper placement of the electric field in relation to the absorbed light is the most crucial aspect of an effective PV device.

2.7 Current from a Solar Cell

The concept of semiconductor band gap is essential to estimate how many photons contribute to the electric current. Each semiconductor material has a unique band gap. A material's band gap is simply the energy at which a photon will dislodge an outer electron from its bond. This characteristic energy varies for different semiconductor materials, because each of them has different bond strength. The materials whose bonds are weak have small energy band gaps; those with strong bonds have high band gaps.

Semiconductors are almost totally transparent to photons that have less energy than their band gaps (E_g) because this kind of light does not have enough energy to be absorbed. Such photons pass right through the semiconductor as if it were glass. But almost all light with more energy (E) than that needed to free an electron in a given semiconductor generates free electrons and holes.

$$E = hc / \lambda > E_g$$

where h is the Planck's constant, c is the velocity of light and λ is the wavelength of the incident light.

Semiconductors can be very powerful absorbers of light. In some cases, only a micron is sufficient to absorb 99% of the photons with energy greater than their band gaps. The absorption of light in a semiconductor is governed by the equation

$$I = I_0 e^{-\alpha t}$$

where α is the absorption coefficient, I_0 is the intensity of incident light and 't' is the depth of semiconductor material from the surface of incidence.

If we wanted to absorb all the solar photons, the semiconductor band gap would have to be very small. The currents would be as large as possible. But, the voltage would be negligible. This is because the electric field that drives the current is proportional to the material's band gap. A small band gap means a small voltage. In practice, a compromise has to be made and a material with a band gap that allows both reasonable current and voltage has to be chosen.

The band gap at which spectrum-driven losses are smallest in single-junction cells is about 1.4 eV. However, a plateau of band gap values at which losses are still manageable extends from about 1.0 eV to 1.8 eV. Within this band gap range, the theoretical sunlight-to-electricity conversion efficiency limit with the simplest of all PV designs is 23-30 % [27].

2.8 Current-Voltage Characteristics of a Solar Cell

The current voltage characteristics of a solar cell under both dark and light (illuminated) conditions are shown in figure 2.8. The solar cell, under dark conditions, is a p-n junction diode. Hence, the dark current is given by the diode equation.

$$I = I_0 (e^{qV/kT} - 1)$$

The current from the illuminated cell is given by

$$I = I_0 (e^{qV/kT} - 1) - I_L$$

where I is the total current, I_0 is reverse saturation current, and I_L is the light generated current.

In the typical current-voltage curve of a device, we can define three parameters that give a rather complete description of the electrical behavior. The first one is the short-circuit current I_{sc}, which is obtained for V=0. The second parameter is the open-circuit voltage V_{oc}, which is obtained for I=0. In the ideal case, the expression for open-circuit voltage can be derived as

$V_{oc} = kT/q \ln [(I_L / I_0) + 1]$

V_{oc} is determined by the ratio I_L / I_0 and thus by the absorption and light-generation processes and the efficiency with which the charge carriers reach the depletion region.

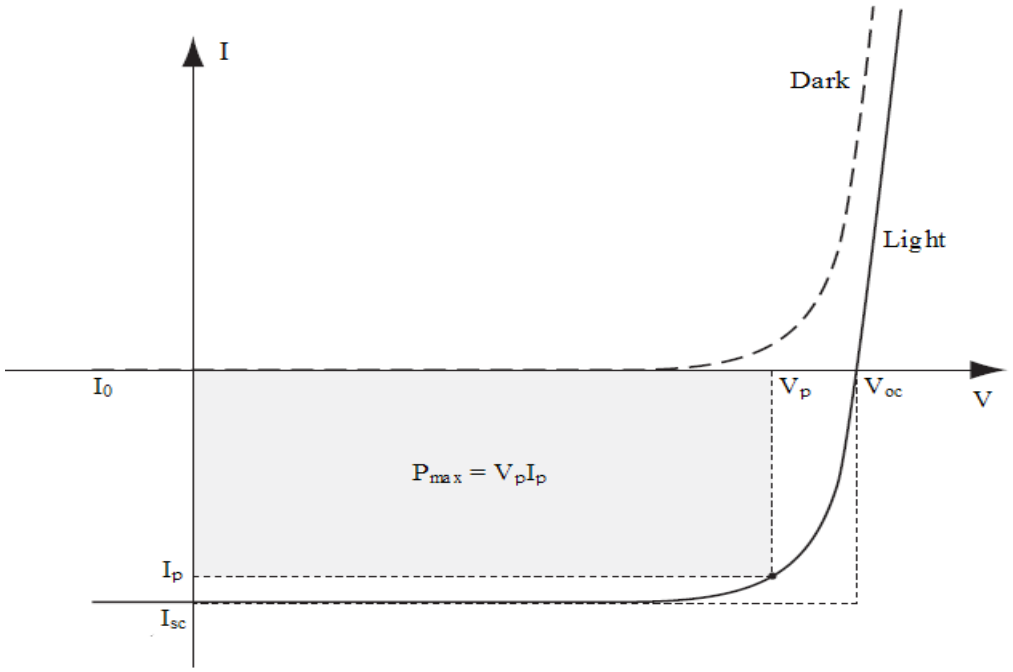

Figure 2.8: I-V Characteristics of a Solar Cell Under Dark and Illuminated Conditions

The performance of the solar cell is eventually determined by the fraction of the total power of incident light that can be converted into electrical power. Under illumination, the junction is forward biased and the external load resistance determines an operating point on the current-voltage curve. The electrical power output (P = IV) is equal to the area of the rectangle that is defined by the corresponding values V_p and I_p.

In general, the solar cell will be operated under conditions that give the maximum power output. The maximum possible area $P_{max} = V_p I_p$ for a given current-voltage curve determines the fill-factor FF, which is defined by

$FF = V_p I_p / V_{oc} I_{sc}$

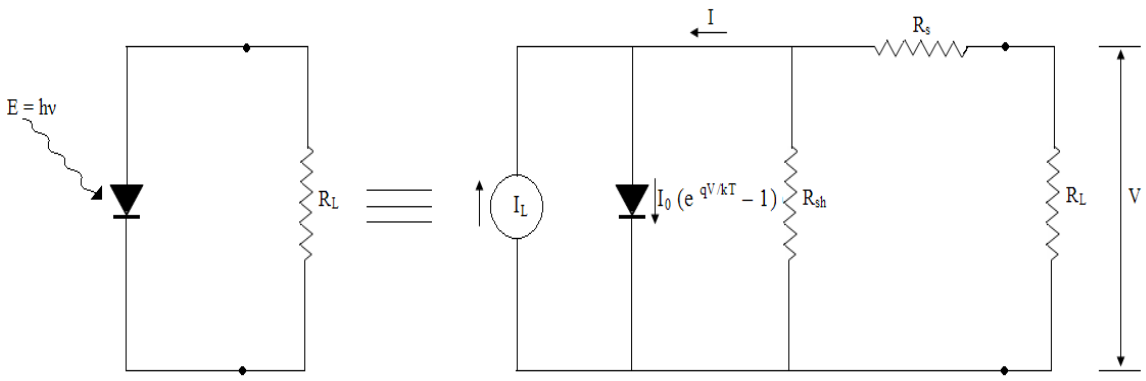

Figure 2.9: Equivalent Circuit of a Solar Cell

The current-voltage characteristics of the p-n junction are further modified because of a parasitic series R_s and a shunt resistance R_{sh} associated with the solar cell. The bulk resistance of the semiconductor material and the resistance of the contacts and interconnections are the origin of the series resistance. The shunt resistance can be caused by lattice defects in the depletion region, such as grain boundaries or large precipitates. Another reason for shunts could be leakage current around edges of the cell. The equivalent circuit of a solar cell with the series and shunt resistances is shown in fig 2.9.

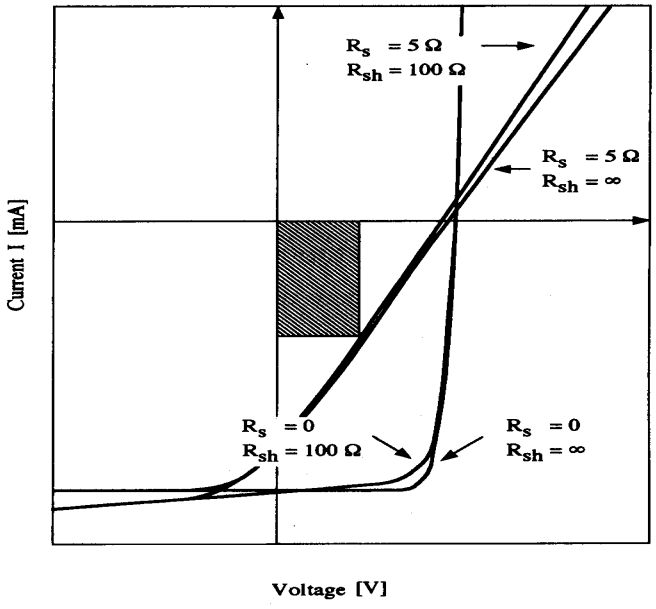

Figure 2.10: Effect of Series and Shunt Resistances on the IV Characteristics

To evaluate the effect of these parameters on the current-voltage characteristics, they must be included in the equation for current. A plot of the equation for various combinations of series and shunt resistances, as in figure 2.10, shows that the shape of the current-voltage characteristics and hence fill factor changes. Ideally, the series resistance of the cell should be zero and the shunt resistance should be infinite. As can be seen, a shunt resistance as low as 100 Ω does not appreciably change the power output of the device, but a small series resistance of only 5 Ω reduces the total efficiency by 30% [28].

The three parameters V_{oc}, I_{sc} and FF are sufficient to calculate the energy-conversion efficiency η of the solar cell, which is defined by

$$\eta = V_p I_p / P_{in} = FF\ V_{oc} I_{sc} / P_{in}$$

where P_{in} is the total power of incident light.

CHAPTER 3

CIGS SOLAR CELLS

3.1 Introduction

Current emphasis in photovoltaics is directed towards the development of high-performance inexpensive solar cells that can serve in the long term as viable alternatives to the single crystal silicon technology. The choice of semiconductors for photovoltaic conversion is based on a number of requirements including the following for a solar cell material.

1. A direct band gap with nearly optimum values for either homojunction or heterojunction devices.

2. A high optical absorption coefficient, which minimizes the requirement for high minority carrier lengths.

3. The possibility of producing n and p-type material, so that the formation of homojunction as well as heterojunction devices is feasible.

4. A good lattice and electron affinity match with large band gap window layer materials such as CdS and ZnO so that heterojunctions with low interface state densities can be formed and deleterious band spikes can be avoided.

These requirements are satisfied by a number of II-IV compounds and a wide range of multinary semiconductors mainly based on copper ternary compounds with the chalcopyrite structure. Foremost among those materials, that have emerged as leading candidates are the chalcopyrite-type Copper ternaries; primarily $CuInSe_2$ [28].

3.2 $CuInSe_2$ Thin Film Photovoltaics

$CuInSe_2$ is a ternary alloy belonging to the I-III-VI class of semiconductors with a direct band-gap of 1.0 eV and an absorption coefficient of 3.6 x 10^5 /cm which is the highest reported, to date [32]. The CIS-based solar cells are simple to produce and they also exhibit features like chemical stability, stability with time, and doping versatility [5]. The absorbing layer is the key element of solar converters, which is produced mainly from the p-type semiconductor [5].

$CuInSe_2$ crystallizes in the chalcopyrite structure as shown in figure 3.1, which is primarily a diamond like lattice with a face centered tetragonal unit cell. Each Selenium atom serves as the center of a tetrahedron of two Cu and In atoms. In turn, each metallic atom is surrounded by a tetrahedron of chalcogen atoms.

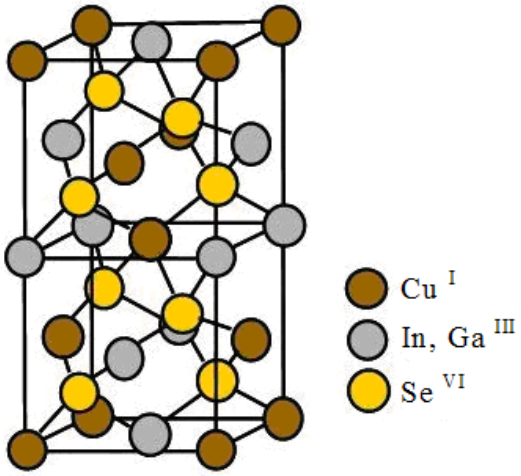

Figure 3.1: Chalcopyrite Structure of CI(G)S

The electrical properties of Cu ternary semiconductors are basically determined by native defects. A high degree of compensation between native donors and acceptors as determined for $CuInSe_2$, seems characteristic [18]. The possible electrically active intrinsic defects are vacancies, interstitials and antisite defects. Depending on these defects, the material can have either n type or p type conductivity. For $CuInSe_2$, the

electrically active intrinsic defects are Copper vacancies (V_{Cu}) and Copper on Indium antisite defects (Cu_{In}) in a p-type material and the defects that make the material n-type are Selenium vacancies (V_{Se}) and Indium on Copper antisite defects (In_{Cu}). Copper rich material is generally p-type and highly conductive. This kind of material is not preferred mainly because of the formation of Copper Selenide (Cu_2Se). Cu_2Se being highly conductive, shorts out the junction. Adding more Indium than copper reduces the formation of Cu_2Se but it causes other defects like V_{Cu} and In_{Cu} which are compensating in nature. Hence, the Copper to Indium ratio (Cu/In) is always maintained around unity. Samples with p-type conductivity are grown if the material is Cu-poor and is annealed under high Se vapor pressure, whereas Cu-rich material with Se deficiency tends to be n-type [6]. $CuInSe_2$ films when suitably manufactured tend to be p-type because of the low energy of formation of Copper vacancies which give the material its conductivity [12].

3.3 $Cu(In,Ga)Se_2$

One of the issues with $CuInSe_2$ solar cells is their relatively lower V_{oc}'s which is mainly due to its small band gap. This limitation is overcome by adding controlled amounts of Gallium to replace Indium in the CIS structure. The band gap of $CuIn_{(1-x)}Ga_xSe_2$ varies according to the equation

$$Eg = 1.011 + 0.664x – 0.249x (1-x)$$

Depending on the [Ga]/ [In+Ga] ratio, the bandgap of CIGS can be varied continuously between 1.02 eV and 1.72 eV [14]. Employing $CuInGaSe_2$ together with CIS extends the spectral range to the IR region [5]. The addition of about 30% Ga in CIS increases the bandgap to 1.4 eV. This has a closer match with the AM 1.5 solar spectrum.

Addition of Gallium not only increases the band gap but also has other beneficial effects. The addition of Ga improves the adhesion of the film to the Mo substrate. The carrier concentration in the absorber is also reported to increase with addition of gallium. Moreover, defect chemistry, electron and hole affinities, film morphologies and lattice constants are also affected by the addition of Ga.

The addition of Ga in the film can be done in a way that the concentration of Ga is the same throughout, resulting in homogenous films with uniform bandgap everywhere. The Ga profile in the absorber can also be varied resulting in graded band gap structures. By using graded compositional profiles, i.e. higher gallium concentration towards the back contact, a back-surface field (BSF) is achieved since a higher concentration of gallium mainly increases the conduction band level in the CIGS layer. A reduced back-contact recombination has earlier been demonstrated by the use of such a BSF [2]. Band-gap grading creates a quasielectric field due to the conduction band bending, moving the electrons towards the junction, thereby increasing the probability of their collection. Further, graded band gap structures could be developed which could result in an improvement in V_{oc} without reduction in I_{sc} [5].

Though it is beneficial to add Ga to improve the properties of CIS, there is a limit to which it serves favorable. Higher Ga content of 40% has a detrimental effect on the device performance, because it negatively impacts the transport properties of the CIGS absorber film [7]. The current, high-efficiency devices are prepared with bandgaps in the range 1.20–1.25 eV, this corresponds to a [Ga]/[In+Ga] ratio between 25 and 30% [7].

3.4 Device Structure of CIGS Solar Cells

The basic device structure of Mo/CIGS/CdS/ZnO solar cells is shown in figure 3.2. The devices are fabricated on soda lime glass substrates. These devices fall under the category of substrate configuration because the layers are fabricated on top of the substrate and light enters the cell through the front transparent contact, ZnO.

3.4.1 Substrate

The most widely used substrate for CIGS solar cells is soda lime glass (SLG). Low cost soda lime glass is an alkali containing substrate from which sodium diffuses into the CIS layer during semiconductor formation and improves grain growth and cell performance. SLG also shows a near optimum match in the thermal expansion coefficient with $CuInSe_2$ (CIS) and $Cu(In,Ga)Se_2$ (CIGS). The soda lime substrate acts as a sodium source for the

CIS thin film and the molybdenum back contact exhibits controlled sodium permeability [5].

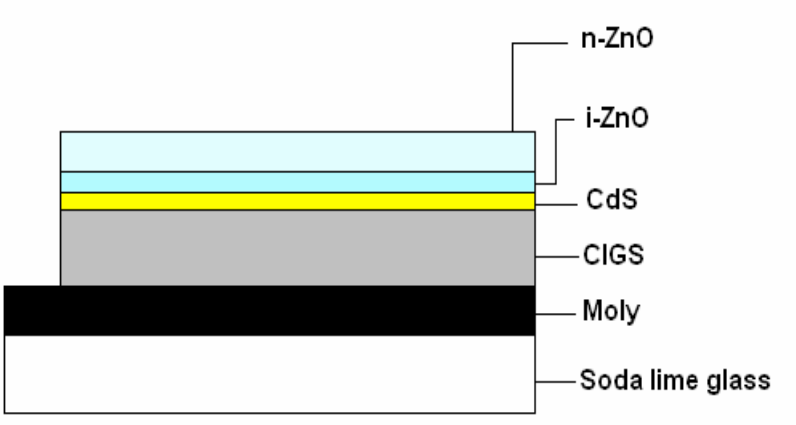

Figure 3.2: Device Structure of CIGS Solar Cells

The most important electronic effect of Na incorporation into CIGS films is a decrease in resistivity by up to two orders of magnitude. An increase in carrier concentration by typically one order of magnitude is often associated with a lower number of compensating donors [12].

Though glass is the most commonly used substrate, recently some effort has been made to develop flexible solar cells on polyimide, metal foils and stainless steel substrates. Highest efficiencies of 12.8% and 17.6% have been reported for CIGS cells on polyimide and metal foils, respectively [12].

3.4.2 Back Contact

The basic requirements for a back contact material other than being conductive are that it should form an ohmic contact to the CIGS layer, have a low recombination rate for minority carriers, exhibit some inertness to the subsequent processing steps and preferably have a high light reflectance [3]. Molybdenum (Mo) is so far the best back contact material for CIGS solar cells because it satisfies most of the above mentioned requirements [3].

Recombination at the back contact can become a critical issue in the cell performance. Back contact recombination becomes dominant as soon as the diffusion length becomes equal to or larger than the thickness of the absorber [6]. Various metal contacts to p-type CIS were examined by Matson et al. concluding that only Au and Ni ensure an ohmic contact. Early results by Russell et al. suggested that Mo back contacts for CIS form a Schottky-type barrier. But recently, work of Shafarman et al. who analyzed the Mo/CIS interface separately from the cell shows the contact to be ohmic [6]. Various materials like W, Mo, Ta, Nb, Cr, V, Ti and Mn have also been investigated as possible back contact materials [15]. The cells with the highest reported efficiency of 19.2% were fabricated with Mo as the back contact.

The thickness of the Mo back contact is usually 1μm and widely deposited by sputtering. The properties of the film like electrical resistivity and adhesion to the substrate have been found to be dependent on the deposition parameters [16]. Films deposited at higher pressure exhibit higher resistivity but have good adhesion to the substrate. Films deposited at low pressures have low resistivity but poor adhesion to the substrate. Hence, a bi-layer of Mo is used to have both low resistivity and good adhesion. The resistivity of the Mo layers fabricated in our lab is $5e^{-5}$ Ω-cm [17]. Nowadays, Mo growth by sputtering or e-beam evaporation is the most commonly used back contact for CIGS solar cells [12].

3.4.3 CIGS Absorber Layers

The properties of $Cu(In,Ga)Se_2$ (CIGS) materials have already been discussed in sections 3.2 and 3.3 of this chapter. Given here, are some of the processing details and film properties of other research groups. It is likely that improvements in short circuit current, I_{sc}, and fill factor, FF, can be achieved by improved device design. In contrast, improvements in V_{oc} may require modifications of the cell materials [5].

CIGS films can be manufactured in many different ways. The most commonly used methods are co-evaporation of the precursors, sequential evaporation and selenization [3], sputtering, closed space vapor transport [5] and Spray pyrolysis [18].

There are various parameters in processing that can affect the nature of the films that are grown. It was found that the Se to metal flux ratio affects the grain growth of CIGS thin films. In wide band-gap devices (1.4 eV) large grains of CIGS thin films grew as the Se to metal flux ratio was 51. On the other hand, only small grains formed for a Se to metal flux ratio of 118 [4].

Annealing the CIGS films at high temperature in inert Argon atmosphere was identified to promote interdiffusion of In and Ga in segregated CIS and CGS phases, resulting in a homogeneous CIGS phase [12]. According to the defect chemical model of oxidation effects, surface (including grain boundary) formation in CIGS is accompanied by the formation of donor defects, which are due to the "dangling bonds" resulting from the bonds that need to be broken to form the surface. These can be viewed as Se vacancies and the vacant sites can be occupied by Oxygen atoms. From an electrical point of view, the grain boundary donors are detrimental to solar cell performance in two ways: First, they act as traps for the recombination of photo-generated electrons with holes, which has been identified as a major loss mechanism in polycrystalline photovoltaic devices in general and in CIGS based photovoltaic devices in particular. Second, they result in a positive surface charge, situated at the grain boundaries. This positive charge results in a depletion region and a potential barrier for electrons in the vicinity of the grain boundary. Thus, the effective p-type doping of the CIGS layer is decreased. The placement of Oxygen as a substitute for the missing Se immediately cancels both effects and explains why oxidation is beneficial [7].

It has been found that the CIS compound can be formed directly by electrodeposition from a chemical bath, but the as-deposited layers did not yield efficient devices. Therefore, annealing, is typically done at 400°C in an Se atmosphere, which is required to increase the grain size, form a proper stoichiometric compound, improve the electrical properties and finally obtain efficiencies of up to 8.8% [12].

3.4.4 Importance of Thickness Reduction

It is expected that CIS and CIGS cells should be substantially cheaper than wafer based crystalline silicon modules. However, if and when CIS and CIGS solar cell technology reaches a production volume on the scale of a few 100 MW/ year, the availability and the price of Indium will become a major issue. The availability of Indium in the Earth's crust is comparable to that of silver, and because of this relative scarcity, Indium has been subject to erratic fluctuations in world market price [11]. A reduction of materials usage is particularly important for indium and gallium since the supply of these metals might become an issue if CIGS thin-film solar cells are produced in very large volumes. The deposition time of the CIGS layer could also be reduced for thinner CIGS layers, which would directly lower production costs [2].

The standard thickness of the $Cu(In,Ga)Se_2$ (CIGS) layer in CIGS thin-film solar cells is presently 1.5–2μm. If this thickness could be reduced, with no, or only minor, loss in performance, production costs could be lowered. Reduction of absorber layer thickness, however, is associated with a number of problems. Though the absorption coefficient of CIGS is extremely high, reducing the amount of light absorbed in the CIGS will reduce as the amount of material reduces. In a study conducted by Lundburg et al. [2], when the absorber layer thickness was reduced, the devices became electrically shunted. Shafarman et al [19] reported an increase in the shunt conductance as the thickness was reduced. Another potential problem when the thickness of the CIGS is reduced is that the carriers will be generated closer to the back contact and have a higher probability of back contact recombination. Also, the thinner CIGS films had smaller grains and thus relatively larger grain boundary area which could also be the reason for recombination losses [2]. Lundburg et al. also observed increase in recombination close to the interface for thinner CIGS layers and have attributed this to enhanced tunneling recombination [3].

Correlation between QE and absorption coefficient for varying CIGS film thickness have been analyzed. It was found that for thin CIGS layers (0.8 μm), the absorptance was only slightly lesser than the thick layer (1.8 μm) but the QE decreased significantly in the long

wavelengths. This indicates that the current collection is high in the whole CIGS layer when it is thick but due to a higher recombination probability for electrons generated by long-wavelength light deeper in the CIGS layer at the back contact or in the bulk of the layer, the QE in the long wavelength reduces in thin layers. The calculated absorptance for the 0.36 μm CIGS film was much lower than the absorptance in the thicker CIGS layers. In the short-wavelength region, almost all the incoming light was still absorbed, but for the light with longer wavelength the absorptance decreased rapidly. The QE for this device decreased significantly over the whole wavelength region, showing that a relatively high fraction of the generated electrons do not contribute to the current, in spite of the fact that they are generated very close to the surface [2].

The short-circuit current decreased by about 4mA/cm^2 when the CIGS thickness was reduced from 1.8 to 0.9 μm. For absorber layers thinner than 0.8 μm a more pronounced loss was observed. It was observed that although the CIGS thickness is reduced more than ten times for the thinnest CIGS layer, the short-circuit current was still at half its original value [3].

3.4.5 Cadmium Sulfide Window Layers

Semiconductor compounds with n-type conductivity and bandgaps between 2.0 eV and 3.6 eV have been applied as window layers for CIGS solar cells. However, Cadmium Sulfide (CdS) remains the most widely investigated buffer layer, as it has continuously yielded high-efficiency cells [12]. In high efficiency devices, chemical bath deposition (CBD) has been used to fabricate CdS layers. The deposition temperature and the pH of the solution determine the growth rate of the film [20]. CBD deposition of CdS provides complete coverage of the rough polycrystalline absorber surface even at a film thickness of 10 nm. The CdS layer provides protection against damages and chemical reactions resulting from the subsequent ZnO-deposition process. The chemical bath removes the natural oxide from the film surface and, thus, re-establishes positively charged surface states [12]. However, the CBD process of depositing CdS has a low yield [21] and also poses difficulty in terms of generation and disposal of hazardous waste materials.

Though CdS for high-efficiency CIGS cells is generally grown by CBD, which is a low-cost, large-area process, it faces incompatibility with in-line vacuum-based production methods. Physical vapor deposition (PVD)-grown CdS layers yield lower efficiency cells, as thin layers grown by PVD do not show uniform coverage of CIGS and are ineffective in chemically engineering the interface properties [12].

In the CdS, a current loss of approximately 6 mA/cm^2 is estimated [22]. Hence, the recent trend in window layers is to substitute CdS with 'Cd-free' wide-bandgap semiconductors and to replace the CBD technique with in-line-compatible processes. As an alternative to CdS, various materials have shown promising results. These include layers of CBD-ZnS, MOCVD-ZnSe, ALD-ZnSe, CBD-ZnSe, PVD-$ZnIn_2Se_4$, Co-sputtered ZnMgO and ALD-In_2Se_3 [12].

3.4.6 Zinc Oxide – Transparent Conductive Oxide

The front contact for a solar cell has the requirement that it has to be both transparent and conducting. There are a few different Transparent Conductive Oxides (TCO) that have been experimented and Zinc Oxide (ZnO) doped with Aluminum (ZnO:Al) is the most commonly used. Zinc Oxide has a wide band-gap of 3.3 eV and has good electrical and optical properties. Films with transmission of 90% in the 400-1000nm range and resistivity of $9e^{-4}$ Ω-cm have been fabricated in our lab [23]. Due to free carrier absorption, the transmission begins to drop at higher wavelengths, and this effect increases with increase in doping. Hence, a compromise has to be made in terms of low resistivity and free carrier absorption.

CIGS solar cells employ more frequently, RF-sputtered Al-doped ZnO. A combination of an intrinsic (i-ZnO) and a doped ZnO layer is commonly used, as this double layer yields consistently higher efficiencies [12]. It was found that cell parameters, in particular, the fill factor (F.F.) varied with the thickness of the i-ZnO layers. The highest efficiency was achieved when the thickness of the i-ZnO layer was about 70 nm [8]. Although cells fabricated with very thin or without the i-ZnO layer showed comparable performance initially, stability was an issue in those cells. On the other hand, when the i-ZnO layer

was very thick, the cell performance degraded due to the increase in series resistance [8]. Hence an optimum thickness of the i-ZnO layer is needed for best performance of the solar cell.

It has also been suggested that though cells are fabricated with a thin intrinsic layer, because the substrate is maintained at a temperature of 100°C, some of the Al from the doped layer diffuses into the intrinsic layer causing the device structure to be Heavily doped ZnO/ Lightly doped ZnO/ CdS/ CIGS/ Mo [8].

Several deposition techniques such as spray pyrolysis, CVD [24, 25], and sputtering [26] have been successfully employed to fabricate ZnO films. Sputtering has been the preferred method for its production.

Doping of the conducting ZnO layer is achieved by group III elements, particularly with Aluminum. However investigations show Boron to be a feasible alternative, as it yields a high mobility of charge carriers and a higher transmission in the long-wavelength spectral region, giving rise to higher currents [12]. Also, for high-efficiency cells, the TCO deposition temperature should be lower than 150°C in order to avoid the detrimental interdiffusion across CdS/CIGS interface. In the filed of TCO's, a number of materials such as CdO, $CdSnO_4$, In_2O_3, ITO, and SnO_2 are also being actively investigated [7].

3.5 Device Fabrication Details

The substrates that we use to fabricate CIGS solar cells are Soda Lime Glass substrates. The glass is 2 mm thick and is cut into 4" X 2" pieces. The first step in the fabrication process is the cleaning of glass substrates. Cleaning is very important to ensure that the substrate is free of any contaminant molecules. The substrate is soaked in Deionized (DI) water containing a cleaning agent for 3 hours and then scrubbed thoroughly to remove any particulates. The substrate is then rinsed several times in DI water. Following this, the substrates are cleaned in an ultrasonic bath containing 2-Propanol. After rinsing in DI water again, the substrates are placed in a hot water bath at 70°C for 30 minutes. Then, they are covered and stored immersed in water for subsequent processing.

3.5.1 Molybdenum Deposition

Molybdenum, the back contact for our device, is 1 μm thick and is deposited by DC magnetron sputtering. The substrates are loaded in the Load Lock of the sputtering chamber and heated to 150°C according to a certain time-temperature profile and maintained in Argon ambient for 25 minutes to remove any moisture from the substrate. The substrate is then transferred to the Main Chamber where Mo is deposited. Molybdenum is deposited as a bi-layer with Argon as the sputtering gas. The first layer is sputtered to a thickness of 3000Å with 5 mTorr Argon pressure. This layer has good adhesion to the glass substrate but has a higher resistivity. The second layer which is 7500Å is sputtered at a lower pressure (1.5 mTorr) of Argon. This layer has a denser structure and low resistivity. Typical resistivity of the Mo layers fabricated in our lab is around $5e^{-5}$ Ω-cm [17].

3.5.2 CIGS Absorber Layer Deposition

$Cu(In,Ga)Se_2$ (CIGS) absorber layers in our lab are manufactured by a two-stage all-solid-state manufacture-friendly process. The Mo deposited substrates are cut in two halves each measuring 2" X 2". In the first stage, designated as precursor deposition, with the substrate heated to 275°C, Copper and Gallium are sequentially evaporated followed by co-evaporation of Indium and Selenium. In the second stage, designated as Selenization, the substrate is annealed at high temperatures according to a certain time-temperature profile in a selenium environment during which a thin layer of copper is also deposited. It is likely that the copper will move to wherever it can and has bonded. The processing details for the CIGS layer are as given below.

PRECURSOR DEPOSITION:

1250Å of Copper is deposited at 0.8 Å/Sec

800Å of Gallium is deposited at 1.2 Å/Sec

3100Å of Indium is deposited at 2.3 Å/Sec with a Selenium flux of 25 Å/Sec

SELENIZATION:

The Se flux is maintained at 25 Å/Sec throughout Selenization. The substrate is heated from 275°C to 450°C in 4 minutes and maintained at 450°C for 7 minutes. Following this, the substrate temperature is increased from 450°C to 550°C in 4 minutes and maintained at 550°C for 7 minutes and then cooled down from 550°C to 425°C. A thin layer of top copper (~25 Å) is deposited at the 17th minute of Selenization. The time temperature profile of Selenization is shown in figure 3.3.

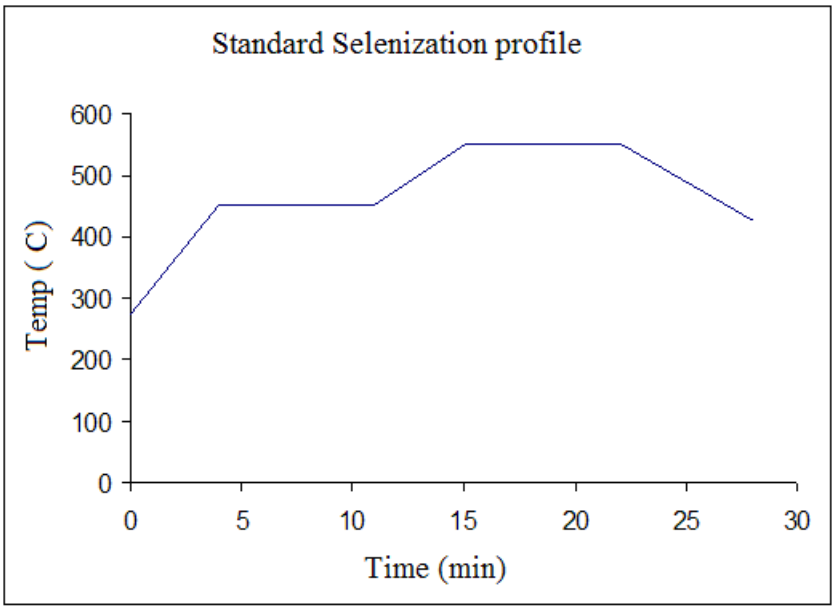

Figure 3.3: Time-Temperature Profile During Selenization

The typical thickness of the absorber layers fabricated by this process is around 2µm. The thickness of the CIGS layer was reduced by reducing the deposition time and Selenization time. The experimental details for the thin CIGS layers are given in the later sections of this chapter.

3.5.3 CdS Window Layer Deposition

A thin layer of CdS, typically 300-500 Å, is deposited on the absorber by Chemical Bath Deposition. The CBD solution contains 150 ml of water and 27.5 ml of ammonium

hydroxide. 22 ml of 0.015M Cadmium acetate solution is added, which acts as the source for Cadmium ions. The cleaned substrate is placed in this mixture and placed in a hot water bath. When the temperature of the solution is 30°C, 22 ml of 0.15M Thiourea, which acts as the Sulfur source, is added. The temperature of the solution is raised gradually to 80°C. To ensure uniform deposition of the CdS layer, the solution is constantly stirred with a magnetic stirrer.

3.5.4 Zinc Oxide Front Contact Deposition

After the deposition of CdS, the substrates are blow dried using pure nitrogen gas and loaded in the RF sputtering system. A mask is used to define active circular dots of 0.1 cm^2 area. On each 2" X 2" substrate, 25 of these dots can be defined. The substrate is maintained at a temperature of 125°C throughout the deposition time. For the standard cells used in this study, ZnO is deposited as a bi-layer consisting of a thin intrinsic layer (350 Å) and a 4500 Å thick Al-doped n-type layer (ZnO:Al). Both the intrinsic layer and the doped layer are sputtered from a 99.995% pure ZnO with 2% Al_2O_3 target. The intrinsic layer is sputtered with a mixture of 0.4 mTorr of Oxygen and 1 mTorr Argon gases. The n-type layer is sputtered in pure Argon ambient with Ar pressure of 1 mTorr. The typical resistivities of the doped ZnO films are 8-12 e^{-4} Ω-cm.

3.5.5 Thin CIGS Layers

The thickness of the CIGS absorber layer in this study was reduced by reducing the deposition time and maintaining the same deposition rates as the standard device. Devices with reduced absorber layer thicknesses of 1.5 μm, 1.0 μm and 0.65 μm were fabricated.

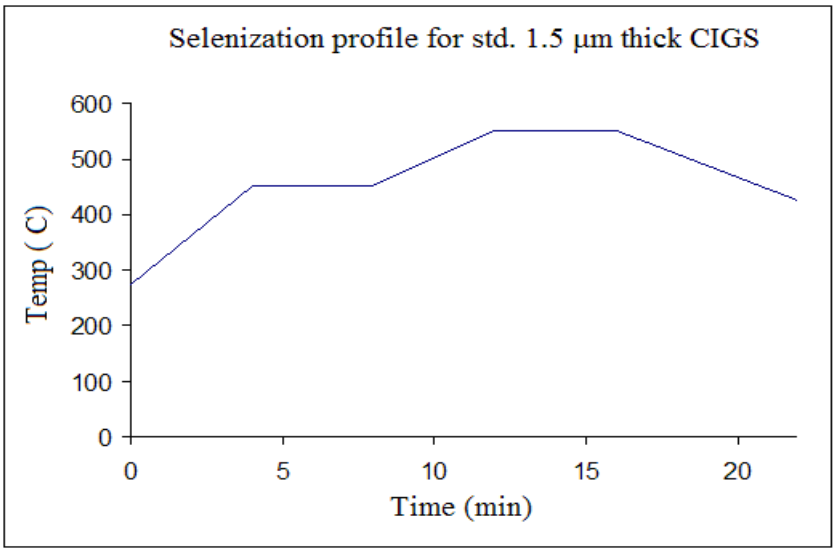

Figure 3.4: Selenization Profile for std. 1.5µm Thick CIGS

At each of the different thicknesses, the selenization time was both reduced proportionally according to the thickness of the CIGS and left unchanged compared to the standard time. The time temperature profiles for the reduced selenization times are shown in figures 3.4 to 3.6. The Selenium flux during selenization was reduced for the thinnest devices for both reduced and standard selenization times.

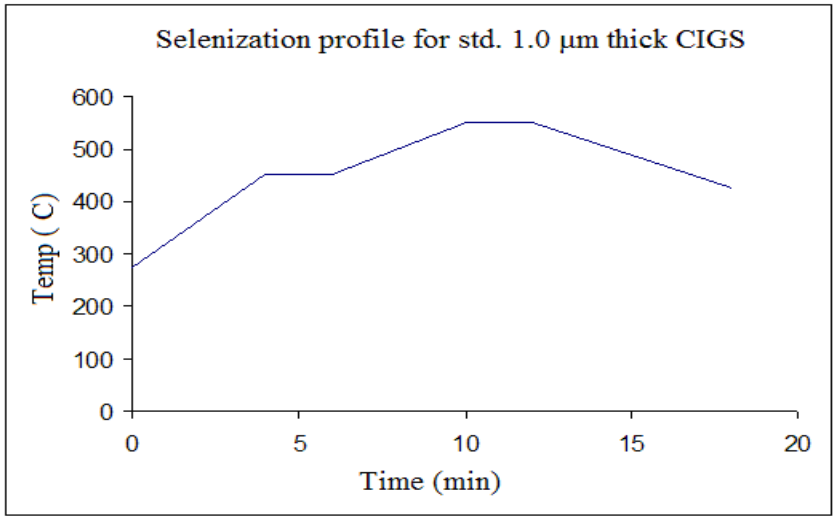

Figure 3.5: Selenization Profile for std. 1.0µm Thick CIGS

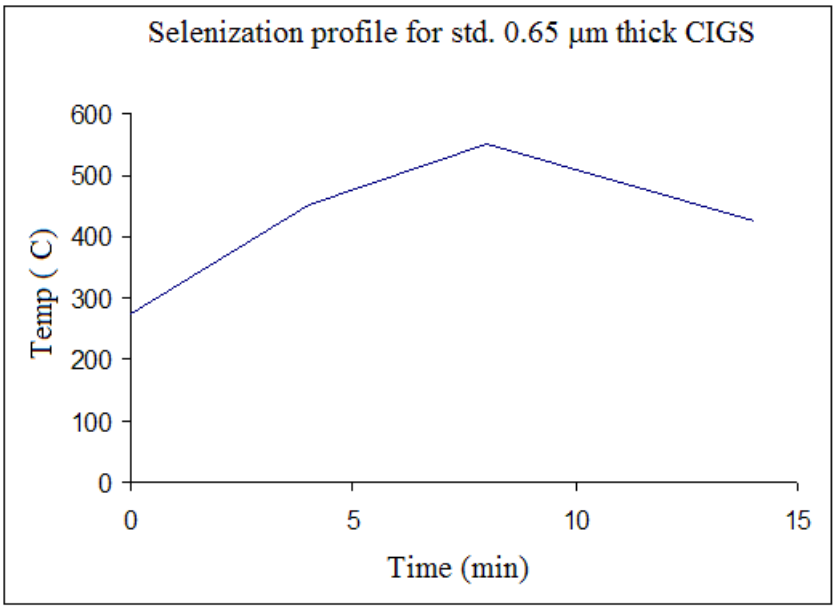

Figure 3.6: Selenization Profile for std. 0.65µm Thick CIGS

Because of the complex nature of our time/temperature profile during fabrication, reducing the deposition time reduces the time for which the substrate is at high temperatures also. To understand what effect this would have in film formation and performance of the device, and if any post-deposition annealing would be required to compensate for the reduced time at temperatures, experiments were carried out with the cells being annealed at different stages before and after completion of the device itself. Annealing was done at 250°C in both air and vacuum.

3.6 CIGS Deposition System

The CIGS deposition system has a substrate holder that can hold a 2" X 2" substrate and has a lamp arrangement to heat the substrate. There are four source evaporation tungsten boats, one each for Cu, In, Ga and Se. The arrangement of sources with respect to the substrate is shown in figure 3.7. A source separation shield, to prevent cross contamination of the sources, is placed between the four sources. The system also has a substrate shutter to shield the substrate from all the four sources. As mentioned earlier, we can have 25 cells on a 2" X 2" substrate. The order in which the cells are numbered

with respect to the position of the sources is also shown in figure 3.7. This kind of an arrangement provides a rich data set with gradients in the metal ratios along both the axes on the substrate.

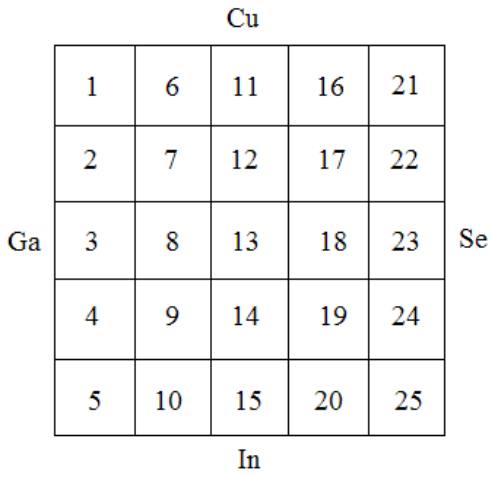

Figure 3.7: Source Arrangement with Respect to the Devices

CHAPTER 4

RESULTS AND DISCUSSION

The main objective of this work was to reduce the thickness of the CIGS layer in our devices. But, before experimenting with the thickness of the absorber, the Zinc Oxide front contact had to be optimized. All previous work done on CIGS solar cells in our lab had a Zinc Oxide front contact that was RF-sputtered from a pure ZnO target with pieces of Alumina. Argon and Oxygen were used as sputtering gases to deposit the intrinsic layer and Argon only was used to deposit the n-ZnO layer. Due to unavoidable reasons, the chamber for ZnO deposition had to be changed. Hence, a series of experiments were conducted to develop and optimize the conditions for ZnO deposition, in order achieve the standard performance of devices.

4.1 Development of Zinc Oxide as a Front Contact

With the old configuration i.e. Alumina pieces on an undoped ZnO target, we were not able to produce Al-doped Zinc Oxide films in the new chamber. The main difference was that the spacing between the target and the substrate was much larger than that in the old chamber. Hence, a ZnO target with 2% Al_2O_3 was used to deposit the doped layer and an undoped target was used to deposit the intrinsic layer. With the substrate directly above the target, both the layers were deposited, but with a vacuum break in between, so that the targets could be changed. The thickness of the i-ZnO layer was 400 Å and the thickness of the doped layer was 4000 Å. The devices fabricated with this contact showed very poor performance especially in terms of Jsc's which were limited to 9mA/cm^2. The Voc and FF distribution of this sample (C001) is shown in figure 4.1 and the spectral response in figure 4.2.

290 39%	230 30%	340 40%	390 57%	210 27%
410 60%	410 64%	360 54%	390 54%	400 52%
340 33%	400 38%	x	x	x
320 55%	380 35%	400 53%	360 56%	220 31%
230 28%	400 41%	400 40%	190 31%	410 55%
380 48%	400 52%	410 62%	400 57%	350 48%

Figure 4.1: Voc and FF Distribution in C001

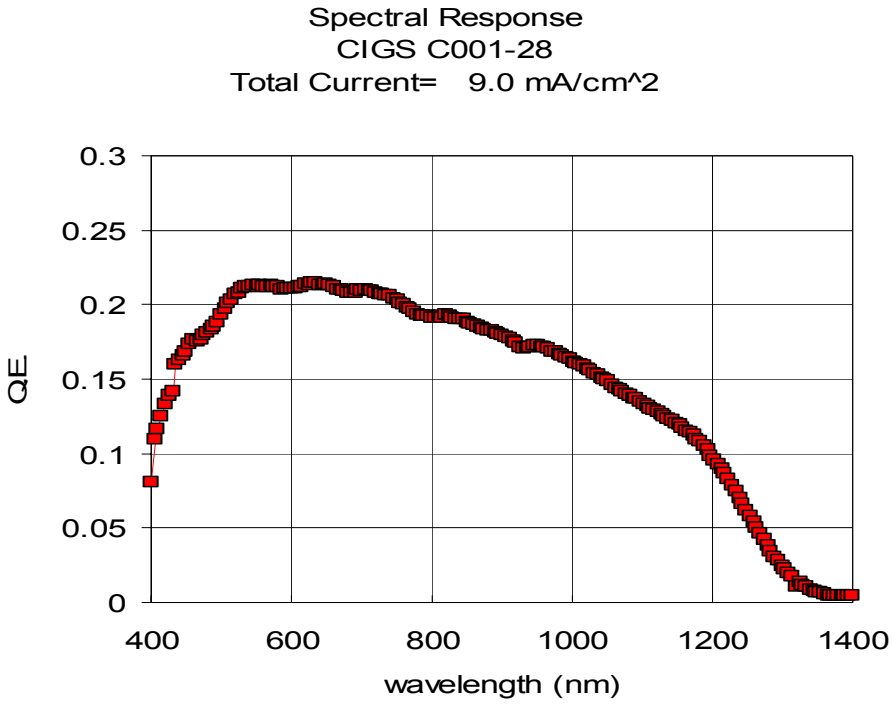

Figure 4.2: Spectral Response of Device C001-28

As can be seen from figure 4.2, the low current is due to the low QE at all wavelengths in the spectral response and this is suggestive of a dominant interface recombination mechanism. The main reason that was thought to affect the performance to this extent was the vacuum break in-between the ZnO layers. Because of the vacuum break, the substrate had to be cooled down from 125°C to room temperature and heated again before the ZnO: Al layer deposition.

The alternative was to use two separate guns for the two layers and avoid the vacuum break in between. Since the i-ZnO layer required is thin (500 Å), the undoped target was placed on the gun away from the substrate and sputtered at an angle. The doped target was placed directly below the substrate. The performances of these devices (C004) are shown in figures 4.3 and 4.4. The current had increased by 2-3 mA/cm^2 compared to the previous device, but was still far from our standard values.

380 45%	410 55%	410 46%	410 47%	410 45%
340 30%	290 32%	400 47%	410 49%	420 45%
360 48%	350 29%	320 28%	390 40%	380 33%
 x	340 34%	410 43%	400 41%	380 38%
 x	400 49%	330 29%	260 28%	410 53%

Figure 4.3: Voc and FF Distribution in C004

From previous work, it was seen that the devices showed poor performance when the substrates were placed directly above the target. This is because of the atomic/molecular

bombardment by the high energy ions during sputtering, which cause damage to the underlying layers. Hence, the substrate's position was moved in between the two guns to

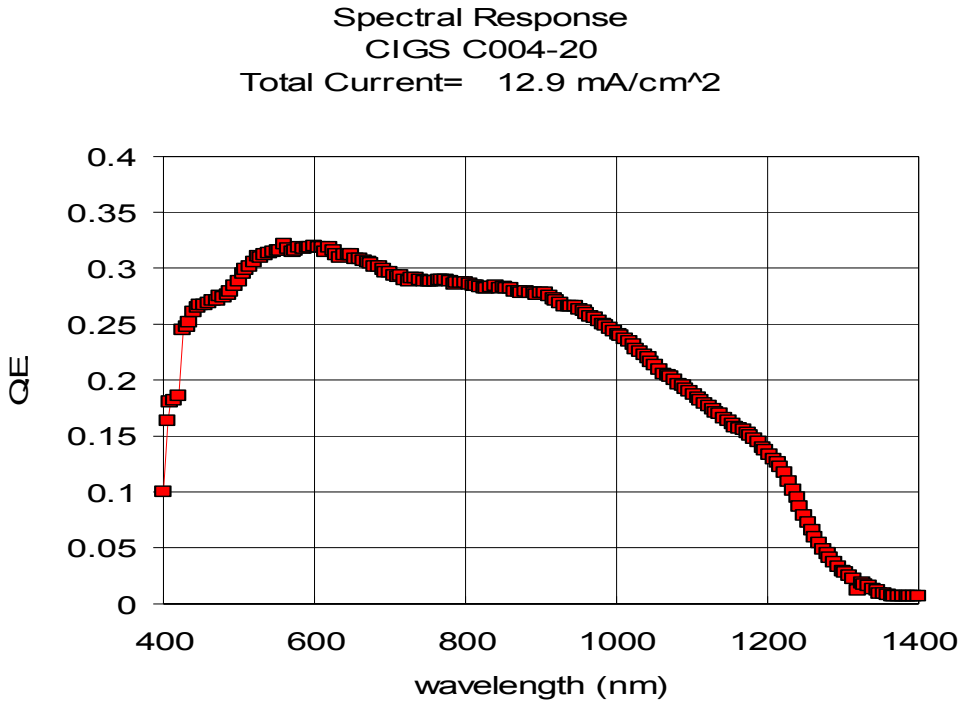

Figure 4.4: Spectral Response of Device C004-20

avoid high energy ions from hitting the substrate directly and causing damage to the deposited films. The V_{oc} and FF distribution of the devices (C009) fabricated by moving the substrate away from the targets is shown in figure 4.5 and the current density is given in table 4.1. With this configuration, the device performance showed marked improvement, but was still off from our standard performance values.

From previous work, it was seen that the thickness of the i-ZnO layer played an important role in device performance. Hence, we started to optimize by varying the i-ZnO thickness. Devices with i-ZnO ranging from 250 to 500 Å were fabricated. Although the device performance was certainly better, more optimization was needed to produce the standard results. Table 4.1 shows the performance of three devices with varying i-ZnO thickness. It can be seen that the performance improves as the thickness is reduced. The values of

Jsc's level off after reaching 25 mA/cm2 and do not increase for further reduction in i-ZnO thickness.

380 45%	410 55%	410 46%	410 47%	410 45%
340 30%	290 32%	400 47%	410 49%	420 45%
360 48%	350 29%	320 28%	390 40%	380 33%
x	340 34%	410 43%	400 41%	380 38%
x	400 49%	330 29%	260 28%	410 53%

Figure 4.5: Voc and FF Distribution in C009

Table 4.1: i-ZnO- Sputtered From an Intrinsic Target: Variation in Device Performance with Respect to i-ZnO Thickness

Sample No	Thickness of i-ZnO (Å)	Voc (mV)	Jsc (mA/cm^2)	Fill Factor (%)
C009	500	420	21	55
C010	350	410	25	60
C011	240	430	25	63

The next possible solution was to deposit the i-ZnO layer with the doped target. To do this, excess Oxygen partial pressure had to be used while sputtering. Intrinsic behavior for the ZnO films was observed when the O_2 partial pressure was about 23 % (0.3 mTorr O_2 + 1 mTorr Ar). With this method of deposition for the i-ZnO, the thickness of the layer was varied to obtain the optimum thickness. Table 4.2 shows the performance of

three devices with varying i-ZnO thickness where the i-ZnO layer was sputtered with 0.3 mTorr Oxygen and 1 mTorr Argon.

Table 4.2: i-ZnO- Sputtered with 0.3 mTorr O_2: Variation in Device Performance with Respect to i-ZnO Thickness

Sample No	Thickness of i-ZnO (Å)	Voc (mV)	Jsc (mA/cm^2)	Fill Factor (%)
C012	500	350	20	50
C013	300	450	26	60
C014	200	400	30	55

The O_2 partial pressure was also varied to see if the performance improved. It was found that the V_{oc}'s started to become worse though there was not much change in current, when the Oxygen partial pressure was increased more than 0.4 mTorr. Table 4.3 shows the performance of devices with varying oxygen pressure.

Table 4.3: Variation in Device Performance with Varying Oxygen Partial During i-ZnO Deposition, i-ZnO Thickness = 300 Å

Sample No	Oxygen Partial Pressure (mTorr)	Voc (mV)	Jsc (mA/cm^2)	Fill Factor (%)
C013	0.3	450	26	60
C015	0.4	420	28	52
C017	0.5	370	30	57

Devices with i-ZnO deposited at 0.3 mTorr Oxygen showed limitation in J_{sc}'s and those deposited at 0.5 mTorr showed limitation in V_{oc}'s. Hence, more experiments were carried

out at 0.4 mTorr Oxygen partial pressure by varying the thickness of the i-ZnO layer. Table 4.4 shows the performance of devices where the i-ZnO was deposited with 0.4 mTorr Oxygen and 1 mTorr Argon, and the thickness was varied.

Table 4.4: i-ZnO- Sputtered with 0.4 mTorr O_2: Variation in Device Performance with Respect to i-ZnO Thickness

Sample No	Thickness of i-ZnO (Å)	Voc (mV)	Jsc (mA/cm^2)	Fill Factor (%)
C015	300	420	28	52
C016	440	350	35	47
C021	380	440	34	62

440 60%	440 61%	440 60%	440 63%	430 62%
440 63%	440 60%	440 63%	430 52%	430 59%
430 60%	430 60%	440 60%	420 47%	430 56%
400 48%	420 56%	420 55%	420 55%	320 57%
310 32%	310 34%	410 50%	360 38%	390 49%

Figure 4.6: Voc and FF Distribution for the Standard Run

It was seen that best device performances for all parameters namely V_{oc}, J_{sc} and Fill Factor were obtained for i-ZnO thickness of 380 Å with the layer being deposited with

0.4 mTorr Oxygen. This was adopted as the standard and the V_{oc}'s and FF's of the standard devices are shown in figure 4.6. A sample spectral response is shown in figure 4.7. The variation in performance of the devices as seen in figure 4.6 is because of the intentional gradient in the metal ratio of the CIGS absorber layer.

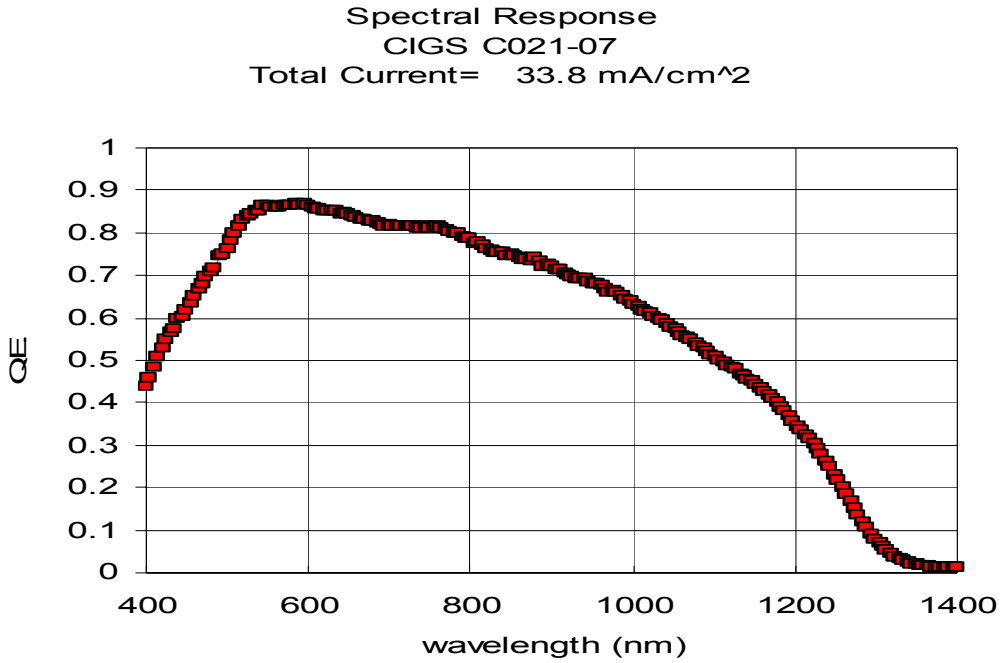

Figure 4.7: Typical Spectral Response of a Standard Device

4.2 Effect of Heat Treatments

Once the ZnO layer was optimized, the main focus was on reducing the absorber layer (CIGS) thickness. This would reduce the processing time and material utilization thereby reducing production costs. Thickness reduction can be achieved by reducing the deposition time and maintaining the standard deposition rates or by reducing the deposition rates and maintaining the standard deposition time. Because of the complex nature of the time-temperature profile during the fabrication of the absorber layer, reducing the thickness by reducing the deposition time will also alter the time for which the substrate is at high temperatures. It is important to understand what role this plays in

film formation and device performance. Also, it is important to understand whether post deposition annealing would be required to compensate for the lowered thermal exposure during growth. Hence, experiments were conducted to determine the effect of annealing on device performance.

Annealing experiments were carried out in air and vacuum at 250°C for 2 minutes after the completion of the device. The run sequence was also interrupted at strategic steps, and annealing was done at intermediate stages before depositing the next layer. The

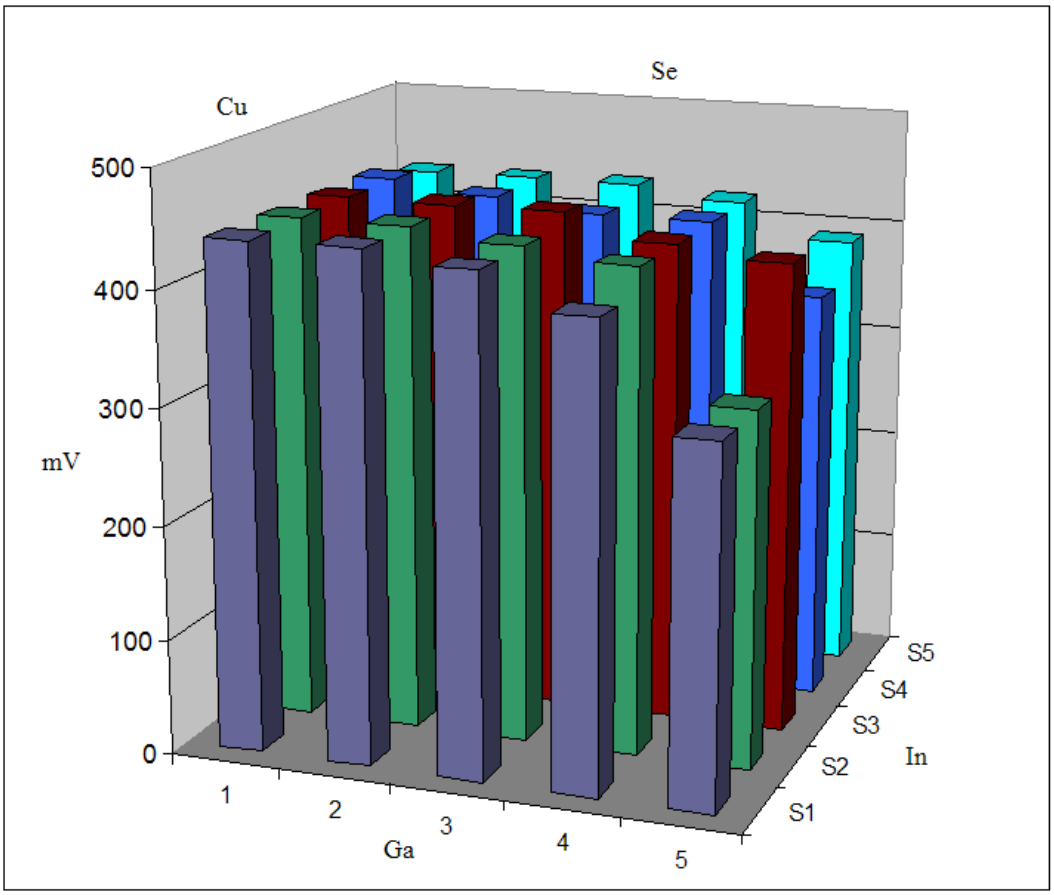

Figure 4.8: Voc Profile for the Standard Run

conditions for annealing and the stages at which it was done are given in table 4.5. Figure 4.8 gives a better perspective of how the V_{oc}'s of devices on the same substrate vary with

metal ratios. The Cu/In ratio is about 1.1 on the Cu side and decreases gradually to about 0.9 on the In side. Ga/In is on average about 0.15; the highest being near the Ga source and decreasing as it goes towards the Se side. As it can be seen, best device performances are obtained in the high Cu/Group III region with Cu/In dominating. The device performance can be made more uniform by increasing the Cu level, but these compositional gradients provide a rich data set to analyze the effect of annealing on different compositions. The QE profiles for three devices in the higher Cu/Group III region are shown in figure 4.9. It can be seen that the performance is very uniform. There is no shift in bandgap in spite of the Ga gradient. Such shifts are often observed as threshold effects in which a small amount of additional Ga causes a significant increase in bandgap. Apparently, we are below that threshold here.

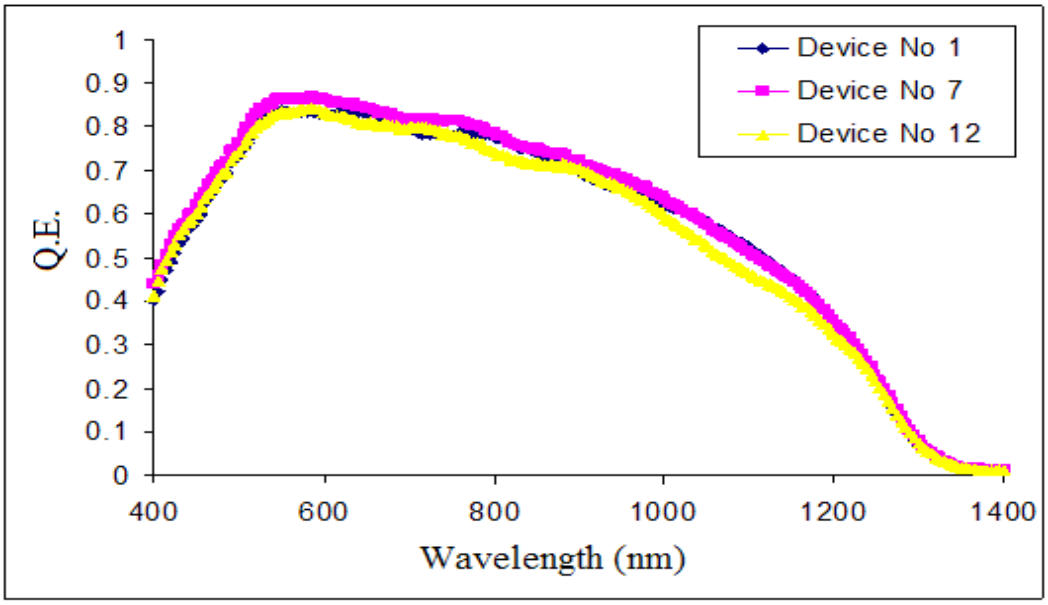

Figure 4.9: QE Profiles of Three Devices on the Standard Run

Figures 4.10 and 4.11 show the effect of annealing on current at different stages. Figure 4.10 shows the actual QE profiles, and figure 4.11 shows the ratio of the QE profiles of annealed devices to the standard device. As it can be seen from table 4.5, annealing the finished device results in a loss of Jsc down to 28.5 mA/cm^2. From figure 4.10, it can be

seen that the loss is mainly due to an overall downward shift in the QE spectrum with somewhat higher loses in the blue region than in the red. AMPS analysis indicated that this is associated with the junction interface region [31]. It has been suggested in the literature that diffusion of Al from the ZnO: Al layer into the intrinsic (i-ZnO) layer could be a possible reason for the loss [9].

Table 4.5: Annealing Stages and Conditions

Conditions	Ambient	Temperature/Time	Voc (mV)	Jsc (mA/cm^2)
Reference Device			438	33.8
Anneal after:				
CdS Deposition	Vacuum	250 C/ 2 minutes	352	29.7
CdS Deposition	Air	250 C/ 2 minutes	394	32.1
Intrinsic ZnO Deposition	Vacuum	250 C/ 2 minutes	400	24.3
Finished (Reference) Device	Vacuum	250 C/ 2 minutes	400	28.5

To verify this, the sample was annealed right after the i-ZnO layer deposition before the ZnO: Al layer. It was seen that there was a greater loss in Jsc down to 24.3 mA/cm^2. From figure 4.10, it can be seen that, in this case there is a downward shift of the whole QE profile with somewhat higher losses in the red. Again, the dominant effect is the downward shift which is indicative of the junction interface region. The loss is larger compared to the loss after annealing the finished device. This indicates that the exposure of the i-ZnO layer to vacuum during anneal enhanced its deterioration. This also suggests that Al diffusion into this layer is not the dominant loss mechanism. Also, higher loss in the red in this case suggests that annealing affects the space charge region also. One possibility for this is a redistribution of the electric field due to deterioration of the interface properties.

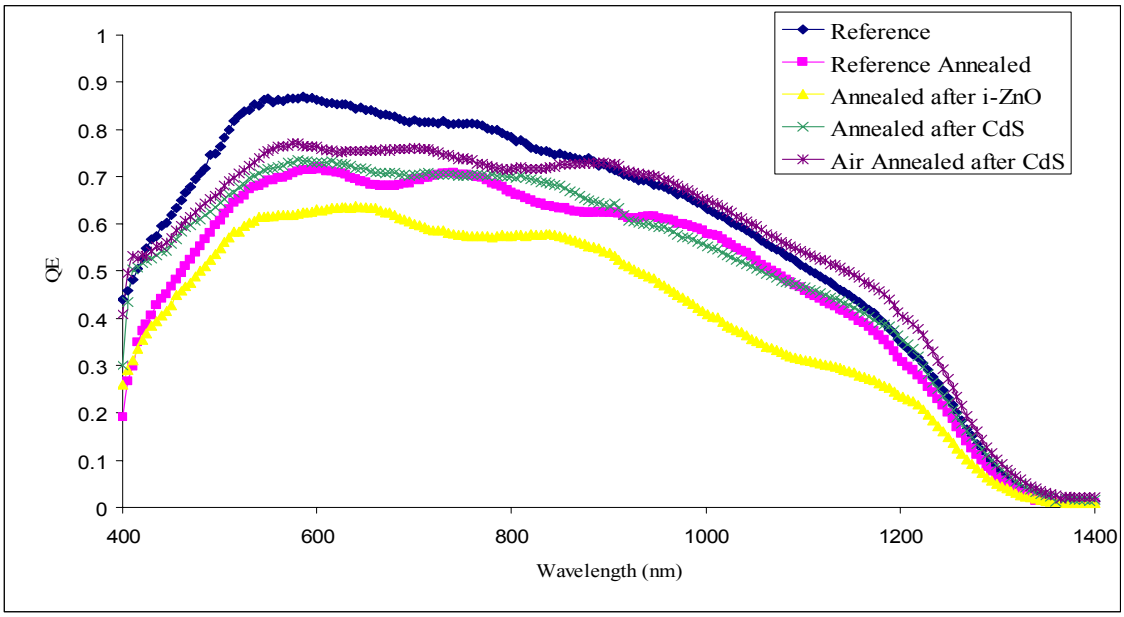

Figure 4.10: QE Profiles for Reference and Annealed Devices

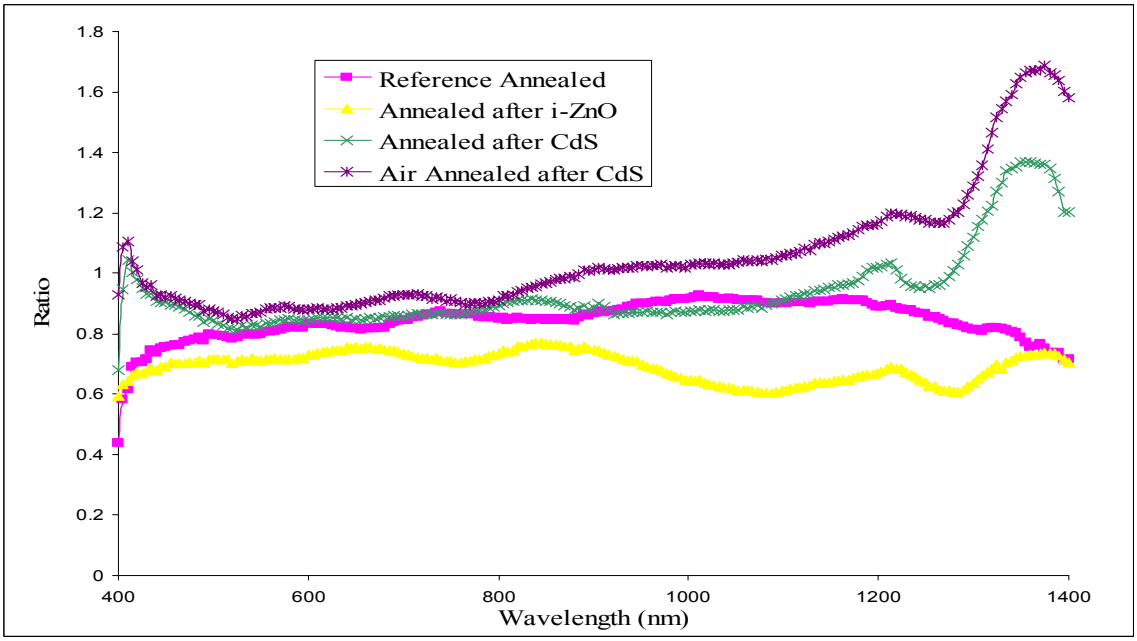

Figure 4.11: Ratio of Annealed Device QE to Reference QE

Two experiments were done to determine the effect of annealing on the CdS layer and its effect on device performance. The samples were annealed after the deposition of CdS in vacuum and air. The sample annealed in vacuum at 250°C showed a loss in Jsc to 29.7 mA/cm^2. The QE response of this device is very similar to that of the device annealed after completion, but with a loss of $1mA/cm^2$ less. This suggests that both the CdS layer and the i-ZnO layers deteriorate during annealing. Also, the QE responses show that the interfaces are contributing to the loss.

It is also possible that if the CdS layer is protected by the ZnO layers, it will not deteriorate. The next experiment was done to test this point. The sample was annealed after the deposition of CdS, but in air. The devices showed a Jsc of 32.1 mA/cm^2. which is at the low end of the reference (standard) sample range. This shows that the air ambient acts as a barrier to losses from the CdS layer, that occur in vacuum. This also supports the idea that, if the CdS layer is protected by the ZnO layers, it will not deteriorate.

From these experiments, it is clear that the primary losses in Jsc's are due to the i-ZnO layer, though there are some contributions to the losses by the CdS layer. It can also be concluded that the i-ZnO layer or its interfaces are deteriorating rather than Al entering the layer from the ZnO:Al layer. From these results, it can also be concluded that any annealing of thinner finished devices will suffer the same losses due to buffer layer deterioration.

4.3 Effect of Annealing on V_{oc}'s

The values of Voc after each stage of annealing are given in Table 4.5. These Voc's are from the high Cu/Group III region. As can be seen, Voc losses occur for all anneal steps, with the highest loss for annealing in vacuum after CdS deposition. This effect seems to be reduced by annealing in air. Except for the device annealed in vacuum after CdS, the losses are almost the same for all other annealing conditions.

A detailed look at the profile of V_{oc} reveals additional insights. In figure 4.12, the V_{oc} profile for the devices after annealing is shown, and figure 4.13 shows the profile of V_{oc} after the anneal steps divided by the reference V_{oc}. Each data point is the average of the 5 devices in a row with the same Cu/In ratio. Position 1 is the closest location to the Cu source and thus has the highest Cu/Group III ratio. Towards to the right, the Cu/In ratio drops monotonically because the devices are further from the Cu source and closer to the In source at position 5. It can be seen that the effect of anneal is not the same for all compositions.

The trends are better seen in figure 4.13 where the data is normalized against the reference. This is necessary because, as mentioned earlier, there is an intentional profile of metal ratios which results in decreasing V_{oc} in the reference with decreasing Cu/In ratio.

In the normalized data in figure 4.13, the trend clearly indicates that the biggest impact of any anneal step is in the high Cu/group III devices. It is not evident why this would be the case, but the end result is an overall leveling of V_{oc} with composition.

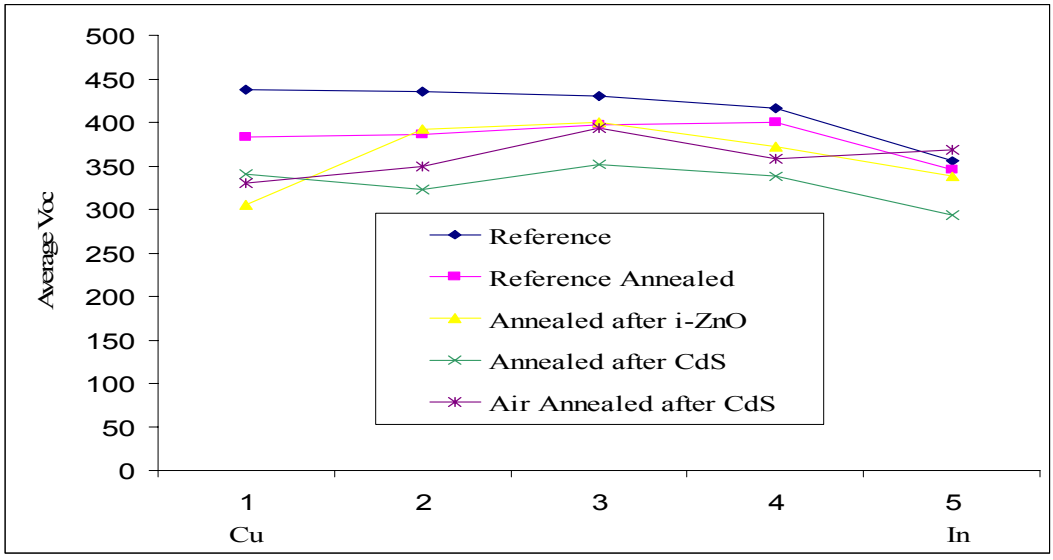

Figure 4.12: Voc Profile After Various Anneal Steps Along Cu-In Gradient

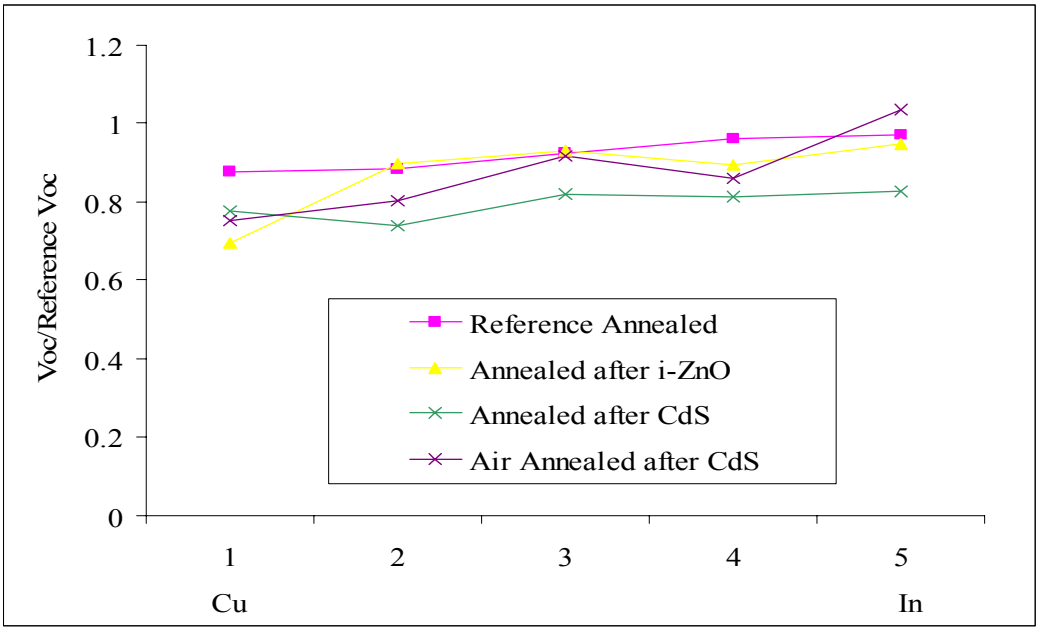

Figure 4.13: Voc/Reference Voc Profile After Various Anneal Steps Along Cu-In Gradient

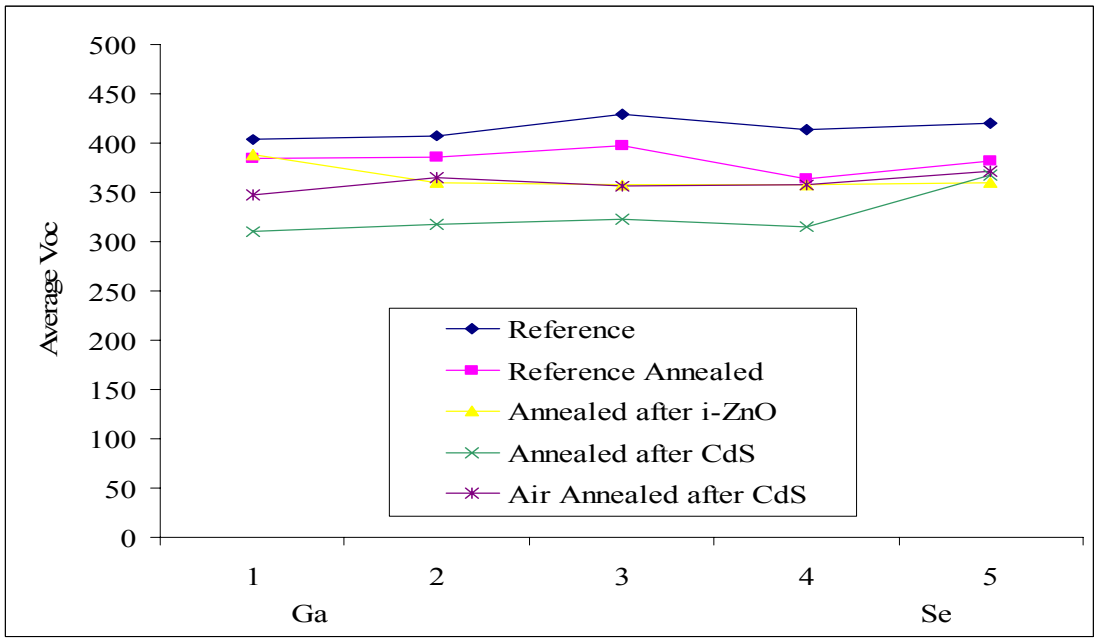

Figure 4.14: Voc Profile After Various Anneal Steps Along Ga-Se Gradient

The other compositional gradient on the substrate is the one for Ga and Se. The corresponding data for profiling across the Ga to Se compositional range are shown in figures 4.14 and 4.15. There are no strong trends observed along this range. Since it is clear from the previous data that the low Cu/group III is less affected by annealing, it is not surprising that the loss in V_{oc} is lesser near the Ga end. These results show that the V_{oc}'s are affected mainly by the ratio of Cu/In, with Ga perhaps playing a secondary role in the dependence on Cu/Group III ratio.

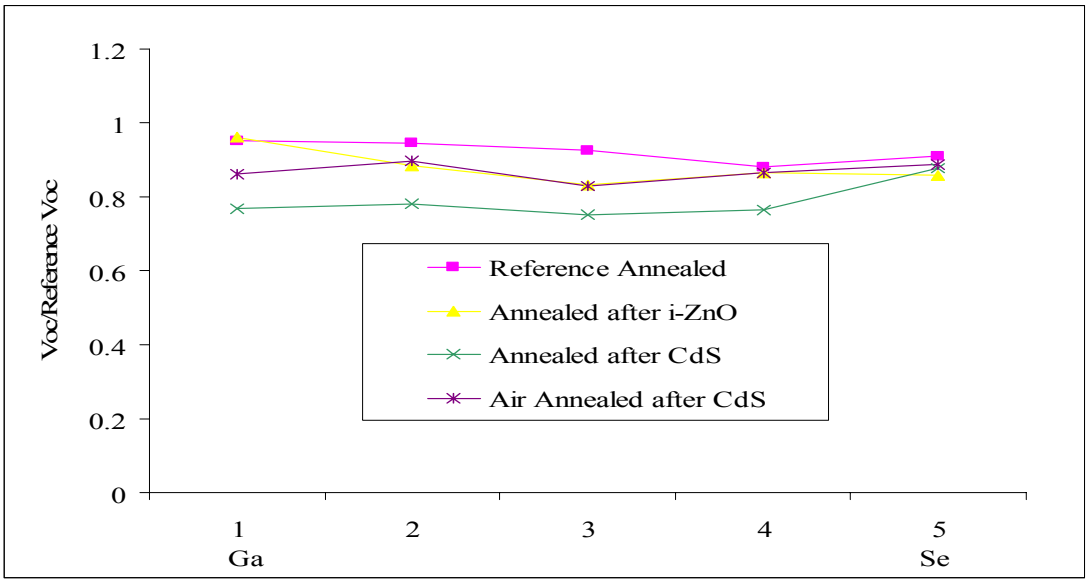

Figure 4.15: Voc/Reference Voc Profile After Various Anneal Steps Along Ga-Se Gradient

4.4 Effect of Top Copper

Data from the previous sections suggest that the films most affected by annealing are those with high Cu/Group III ratio (near unity). This could be because of the thin layer of Cu that is deposited during Selenization. The main Cu layer is deposited first and it has maximum time to react, but the top Cu is deposited towards the end of the process. Though this thin layer of top Cu is exposed to the highest temperature of the process during deposition, it still has a shorter reaction time. The main reason for depositing top

Cu is to avoid any Cu vacancies near the surface. From previous work in our lab, it has been seen that best performances of our devices are obtained only with this thin layer of top Cu. But we know that all high quality p-type CIGS films are fabricated with Cu/Group III ratio lesser than unity and they are filled with numerous Cu vacancies. Hence, we can speculate that not all of this Copper is properly bonded and that it moves and reacts unfavorably with the post-deposition annealing. It could fill the metal vacancies, if any, in the CdS and i-ZnO layers. This would alter the location of the Fermi level in these films which would lower the effective contact energy thereby reducing the V_{oc}'s. The loss in J_{sc} would be explained in terms of an unfavorable effect on the interface states.

4.5 Thin CIGS Layers

The standard devices have CIGS absorber layers that are around 2µm thick. In an attempt to reduce the material consumption and deposition time, the thickness of these layers were reduced to 1.5µm, 1.0µm and 0.65µm. As it was learnt from the previous experiments, annealing the devices at any stage always proves to be detrimental. This also suggests that the time/temperature profile during deposition could play a critical role in device performance. Hence, it was decided to reduce the time/temperature profile proportionally as the thickness to obtain optimal device performance. Devices were also fabricated with reduced absorber layer thickness but longer selenization times.

4.5.1 1.5µm Thick CIGS Layers

The thickness of the CIGS layer was reduced to 1.5µm from the standard 2.0µm i.e. 75 % of the standard thickness, by reducing the thickness of each metal precursor to 75 % of the standard value. This way, the thickness is reduced without affecting the Cu/ Group III metal ratios which remain the same as those of the standard samples. The Selenization time was also reduced from 22 minutes to 16 minutes which is 75% of the standard. The thickness of the top copper was also reduced to 75 % of the standard thickness. All other

parameters including the thickness of the other layers were left unaltered. The device performance obtained for this run is shown in figure 4.16. It can be seen that the V_{oc}'s are slightly higher than the standard values. Also, the best device performances are still obtained in the high Cu/Group III ratio region. It is also clear that the metal ratios are unaltered and the effect of the metal ratio gradient on V_{oc}'s is the same as it was in the thicker devices.

The spectral responses of two devices in the high Cu/Group III region are shown in figure 4.17. The Jsc's of these devices were around 30 mA/cm^2. Reducing the thickness of the CIGS layer caused a slight increase in V_{oc}'s, but resulted in a current loss of around 2 mA/cm^2. The loss in current can be explained by figure 4.18, where the spectral response of the thin device is compared to the standard device. As can be seen, the loss in current is due to an overall downward shift of the entire spectrum. This effect, as mentioned earlier, is mainly due to the interface region.

450 59%	440 55%	420 47%	440 58%	330 52%
450 60%	450 57%	420 50%	430 58%	330 54%
430 57%	460 57%	400 45%	380 42%	410 48%
400 47%	400 52%	410 53%	420 54%	410 54%
430 50%	360 35%	430 52%	420 50%	420 55%

Figure 4.16: Voc and FF Distribution for 1.5µm Thick CIGS

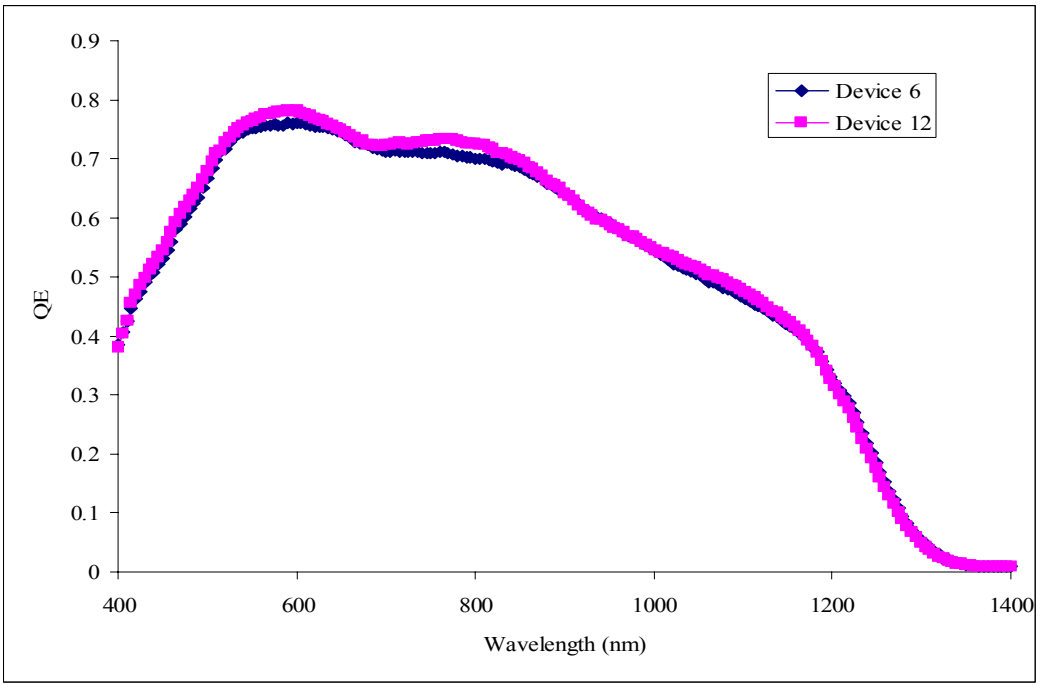

Figure 4.17: Spectral Response of Two Devices with 1.5µm Thick CIGS

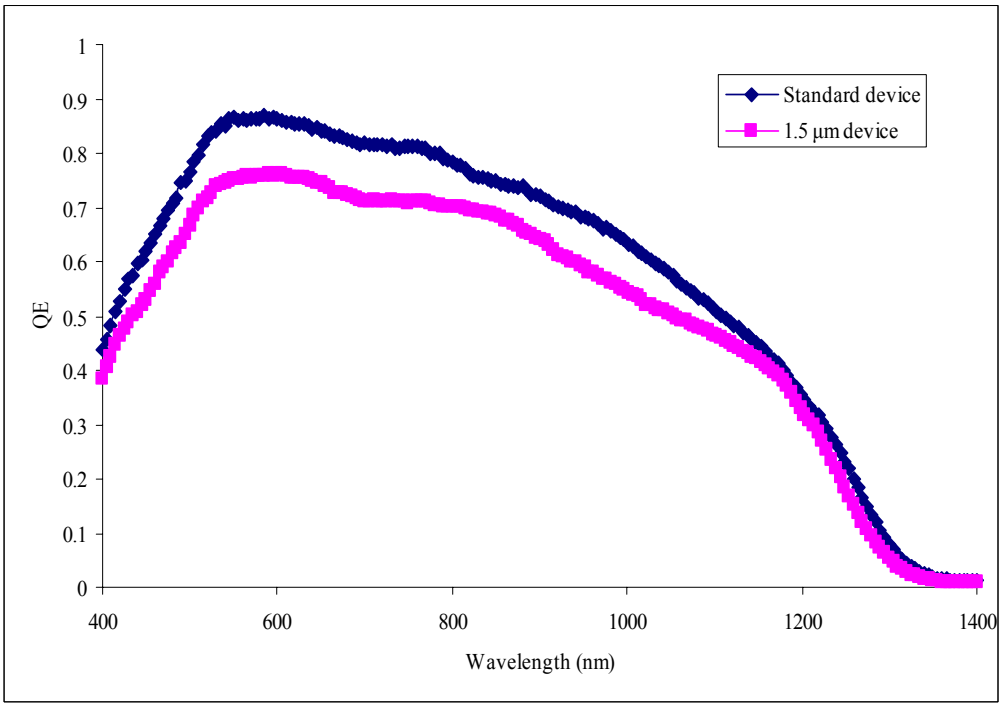

Figure 4.18: Spectral Responses of Standard and 1.5µm Thick CIGS Devices

It can also be seen that there is a very slight increase in the band-gap of the device. This could be attributed to the fact that as the thickness is reduced, more Gallium enters the space-charge region causing an increase in band-gap. The increase in V_{oc} could be due to the increase in band-gap of the devices, although the increase is much less. The presence of interface states has opposite effects on V_{oc}'s and J_{sc}'s [33]. The QE show that the J_{sc}'s have reduced. Hence, the increase in V_{oc} could also be attributed to the interface states.

Figure 4.19 shows the effect of more Ga being incorporated in the space-charge region. Device 2 which is the closest to the Ga source has the highest Ga thickness and it reduces as we move towards the Se source. Accordingly, it can be seen that the highest increase in band-gap is for Device 2 which has the highest amount of Ga. This effect is more pronounced as the thickness is further reduced.

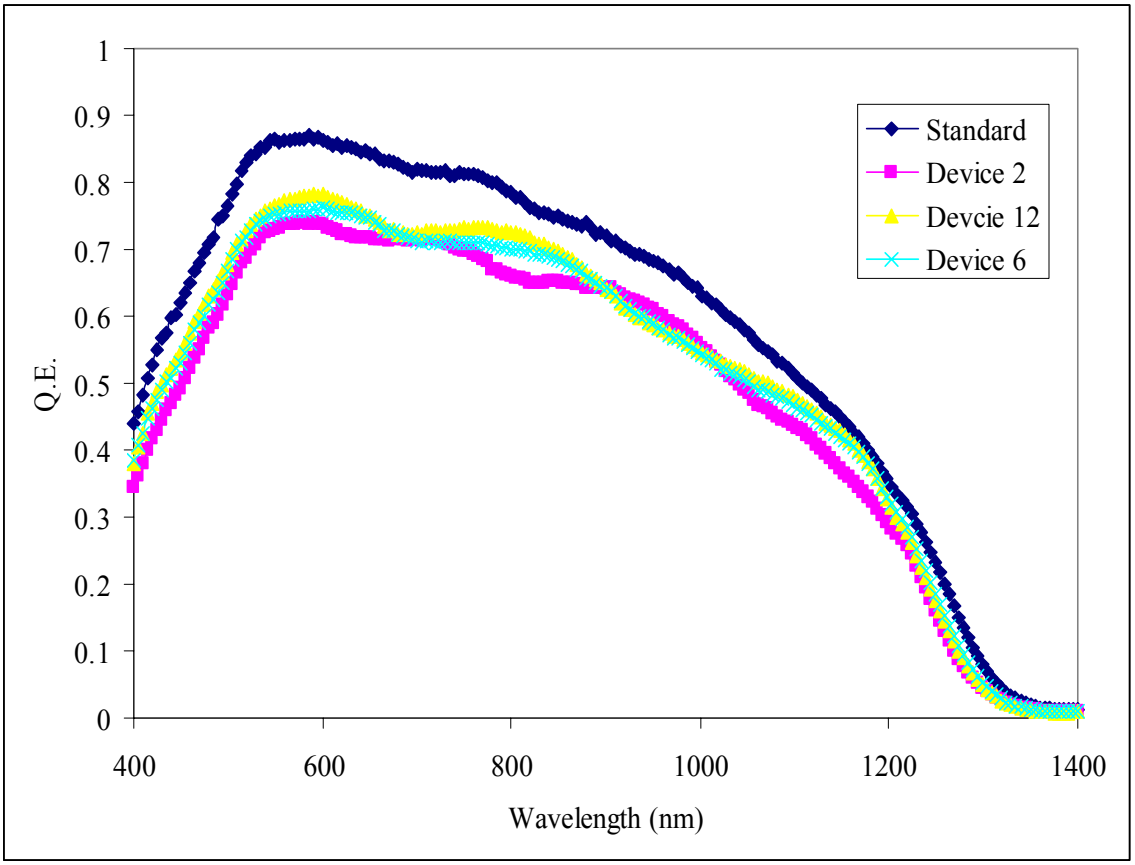

Figure 4.19: Variation in Band-gap of 1.5μm Thick CIGS Devices

4.5.2 1.0µm Thick CIGS Layers

Devices with CIGS layer thickness of 1.5µm showed good performance. Hence, it was decided to further reduce the thickness. Devices with 1.0µm thick CIGS absorbers were fabricated. To start with, the reduction on thickness was done the same way as the 75 % thick devices. The metal precursor thicknesses were cut down in half and the Selenization time was also cut down in half in run C026. The deposition rates were maintained the same as that of the standard process. The values of V_{oc}'s and FF's of these devices are shown in figure 4.20.

It can be seen that the V_{oc}'s and FF's have increased uniformly throughout the sample. The maximum Jsc obtained for these devices was 29 mA/cm^2. Figure 4.21 shows the spectral response of one of the devices on this substrate. It can be seen that there is a significant increase in the band-gap of the device which contributes to higher V_{oc}'s.

470 62%	310 27%	470 60%	460 58%	440 60%
450 59%	450 57%	440 54%	440 55%	430 59%
450 57%	430 47%	440 51%	440 58%	420 57%
430 52%	x	440 56%	440 58%	420 59%
420 45%	410 44%	430 51%	430 55%	410 52%

Figure 4.20: Voc and FF Distribution for 1.0µm Thick CIGS – C026

Comparing the QE spectrum of the standard, 1.5µm thick and 1.0µm thick devices as shown in figure 4.22 shows that the main reason for the drop in Jsc's for the 1.0µm thick devices is the increase in band-gap. The QE spectrum has shifted downwards overall

compared to the standard. But it was seen that this effect due to the interface was observed as soon as the thickness was reduced to 1.5µm. Hence it is clear that there is no further loss in current due to the unfavorable interface effects, but mainly due to the change in band-gap. The V_{oc}'s are also higher by 20-30 mV compared to the standard devices which is again due to the increase in the band-gap.

It is known that most of the Ga in the CIGS tends to accumulate near the back contact region and away from the space-charge region. As the thickness of the CIGS layer is reduced, the junction and hence the space-charge region is brought closer to the back contact. This would lead to more Ga in the space-charge region which essentially increases the band-gap of the material. This effect can be seen clearly from the fact that the band-gap of the devices with 1.0µm devices are much higher than that of the 1.5µm devices.

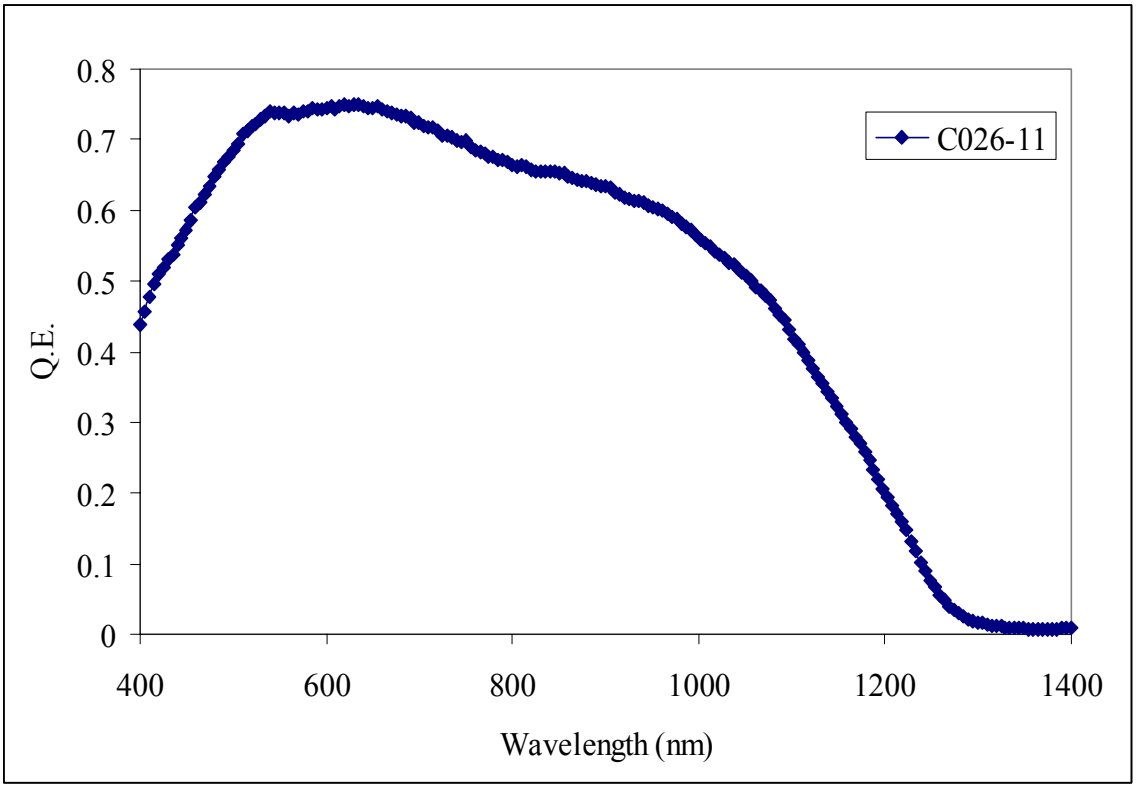

Figure 4.21: Typical Spectral Response of 1.0µm Thick CIGS Devices

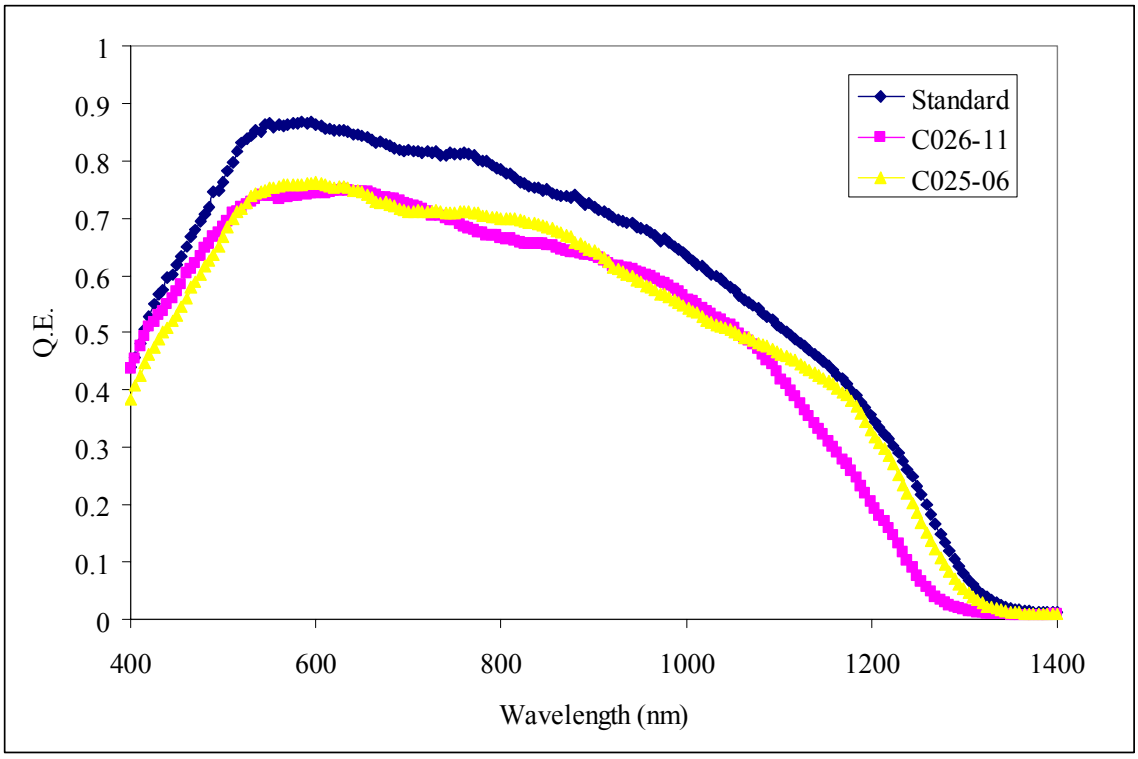

Figure 4.22: Spectral Response of Devices with Standard, 1.5μm and 1.0μm Thick CIGS

To confirm this, C-V measurements were done on both these devices. It was found that the width of the space-charge region, though on the lower end of the standard values, is almost the same for all the devices. This supports the contention that more Ga is incorporated in the space-charge region.

4.5.3 Devices with More Indium

In an effort to bring the band-gap back to the standard value, more Indium was deposited so as to control the increase in Ga incorporation in the space-charge region. It was assumed that adding more Indium than required, would result in a compound with more bonded Indium than Gallium thereby decreasing the band-gap. On the contrary, it was seen that adding more In did not adjust the band-gap to the original value. The band-gap remained the same as it was for standard Indium thickness. It is speculated that, since Gallium is deposited before Indium in our process, it is more likely that Ga is

incorporated in the lattice compared to In which is deposited after Ga. Another interesting observation that could be made from the Voc profile of these device (C027) shown in Figure 4.23, is that the best device performances had now moved towards the In side. It is not clear why this would happen, because adding more Indium alters the metal ratio such that the Cu/ Group III ratio is reduced. From previous experiments, it was found that best device performances are obtained when the Cu/Group III ratio is close to unity and drops off on either side. The drop is greater when the Cu/ Group III ratio exceeds unity. If this were to happen, the devices should have become worse as we move towards the In side. But, it was seen that the V_{oc}'s increased towards the In side. The currents did not follow any particular trend with respect to the metal ratio and were about the same as the previous run.

430 55%	450 57%	450 56%	440 57%	430 53%
430 51%	430 49%	440 56%	440 53%	430 54%
460 59%	430 48%	450 53%	430 50%	420 50%
460 63%	450 60%	450 60%	440 56%	420 53%
450 60%	460 61%	410 43%	450 58%	400 47%

Figure 4.23: Voc and FF Distribution for 1.0μm Thick CIGS with More Indium – C027

4.5.4 Effect of Sodium

As mentioned in chapter 3, the amount of Sodium from the Soda lime glass substrate that enters the CIGS layer also affects the device performance. The amount of Sodium entering the CIGS layer is found to be inversely proportional to the thickness of the Mo back contact. From previous work done related to this issue, it was found that the device

performance varied with respect to the Mo thickness as shown in figure 4.24. As can be seen, the devices show opposite trends for V_{oc}'s and J_{sc}'s. The V_{oc}'s decrease with increase in Mo thickness whereas the Jsc's increase. This compensation effect caused the efficiency to be pinned at a certain level without allowing further improvement. This is because, as the Mo thickness is reduced, more Sodium reaches the CIGS.

It was suspected that this could very well be the cause of what we were observing. Since the thickness of the CIGS layer is now reduced in half, the amount of sodium would be more than that in the standard device. This is equivalent to varying the thickness of Mo in the standard devices.

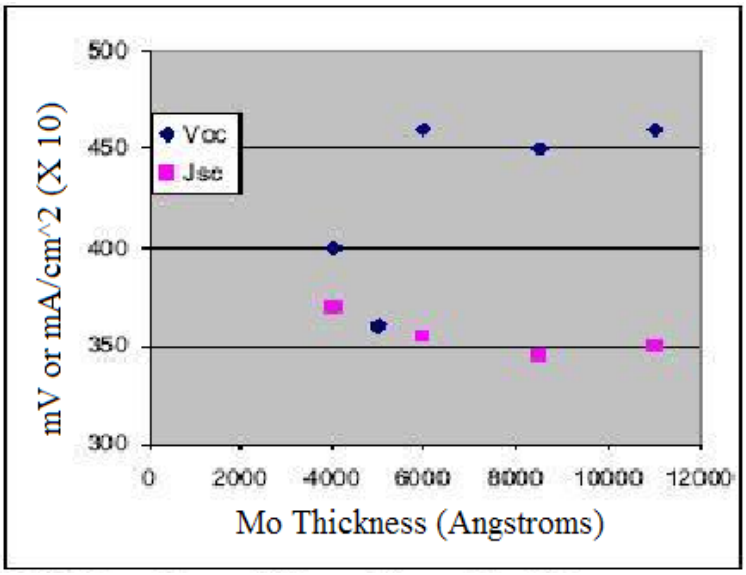

Figure 4.24: Variation in Device Performance with Respect to Mo Thickness

Hence, in order to reduce the amount of Sodium entering the CIGS, the thickness of the Mo back contact was increased from 1.0µm to 1.5µm in run C028. The V_{oc} and FF profile for these devices are shown in figure 4.25. As it can be seen, increasing the thickness of Mo has resulted in uniform performance throughout the substrate. The performance of devices towards the In side have also increased significantly.

470 63%	460 57%	460 60%	450 56%	390 55%
450 60%	450 58%	450 56%	450 58%	450 59%
360 31%	450 55%	440 52%	440 50%	450 59%
450 58%	430 50%	440 52%	450 59%	450 63%
420 41%	450 60%	450 56%	440 60%	440 62%

Figure 4.25: Voc and FF Distribution for 1.0μm Thick CIGS with Thick Mo – C028

This could be because, as the amount of Sodium is reduced, the effect of oxidation reduces and the formation of In_{Cu} antisite defects is reduced, thereby causing increase in V_{oc}'s, especially towards the In side.

Although the performance was better in terms of V_{oc}'s and FF', the J_{sc}'s were still limited to 29 mA/cm^2. This is consistent with the data of figure 4.24 and implies that Sodium is not at a higher level in thin devices. Though the performance of devices was uniform, it did not improve the performance by a whole lot. There are other ways by which the performance can be made uniform without increasing the Mo thickness and that was not of primary concern here. Since increasing the Mo thickness did not serve the purpose of increasing the currents, it was decided to use the standard Mo thickness for future experiments.

4.5.5 Effect of Selenization Time

The effect of Selenization time on device performance was also studied for the 1.0μm devices. In all the previous experiments, the Selenization time was 12 minutes. One

experiment was done where the CIGS thickness was 1.0μm and the Selenization time was increased to 22 minutes. The V_{oc} profile for these devices (C029) is shown in figure 4.26. It can be seen that there is not much of a difference in performance compared to the standard devices in the region away from the Se source. But the devices closest to the Se source, show significant reduction in V_{oc}'s and FF's. This suggests that there is more than required Se which leads to poor performance. It can also be seen that the increase in Selenization time has not affected the device performance since the devices away from the Se source still show good performance. The performance of the devices worsens as we move towards the more Se region, which may be due to the formation of Cu_xSe_y. This is characteristic of the devices fabricated in this chamber because the walls of the chamber are coated with lots of Se which starts to evaporate as the temperature in the chamber increases.

470 60%	470 61%	420 52%	360 41%	360 50%
450 57%	370 47%	410 49%	390 45%	290 35%
470 56%	460 53%	370 35%	440 50%	400 50%
420 45%	400 42%	400 41%	440 47%	290 31%
410 46%	420 45%	420 45%	430 47%	390 43%

Figure 4.26: Voc and FF Distribution for 1.0μm Thick CIGS and Long Selenization Time

The Jsc's were better on these devices near the Cu end. A maximum Jsc of 30.5 mA/cm^2 was obtained from this run. The spectral response of Device 1 which gave the highest current is shown in figure 4.27.

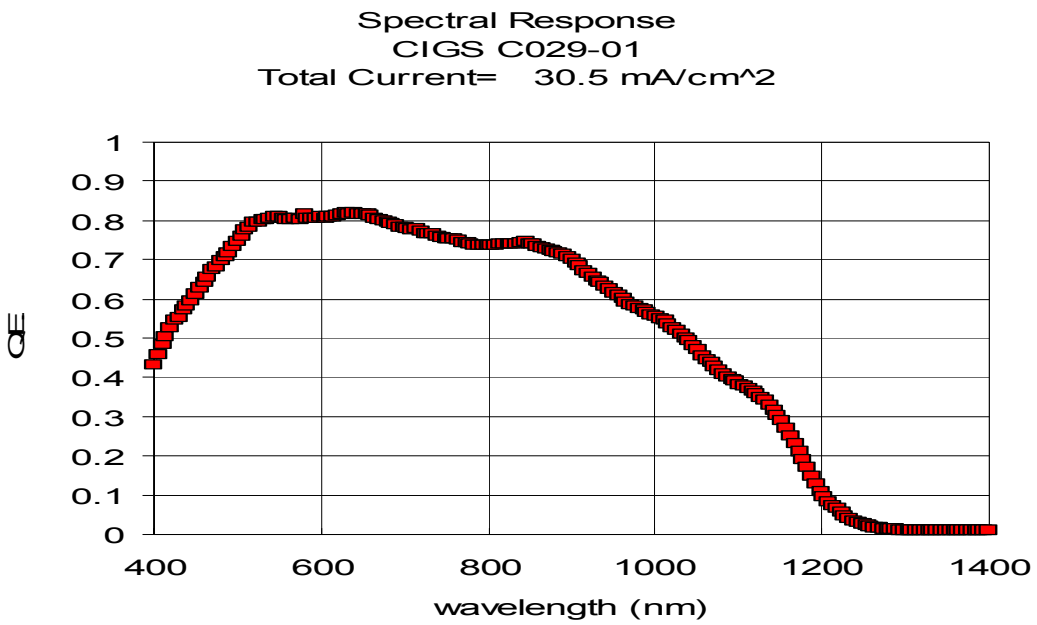

Figure 4.27: Typical Spectral Response of Devices in Run C029

4.5.6 0.65µm Thick CIGS Layers

The devices showed good performance even when the absorber layer thickness was reduced by half. The major loss was in terms of current which dropped by 2-3 mA/cm^2. Hence it was decided to reduce the thickness even further. Devices with 0.65µm thick CIGS layers were fabricated. Initially, devices were fabricated by reducing the deposition time and Selenization time in proportion to the thickness. C030 was the run where the CIGS thickness was 0.65µm and the Selenization time was 8 minutes. The V_{oc} and FF profile for C030 is shown in figure 4.28. It can be seen that the V_{oc}'s are very low and so are the fill factors. The QE spectrum of this device showed in figure 4.29 shows that the band-gap has increased even more.

The thickness of the absorber layer has been reduced by a factor of 3 compared to the standard. This would put the space-charge region very close to the back contact. When the CIGS thickness is reduced, an increased number of electron-hole pairs will be

generated close to the back contact. Most of these electron-hole pairs may recombine before they can be collected because of significant back contact recombination.

170 38%	x	230 33%	300 46%	260 44%
280 44%	x	240 46%	240 31%	320 51%
240 41%	220 41%	210 42%	240 43%	270 45%
270 46%	320 49%	280 47%	270 43%	280 47%
320 50%	300 49%	300 47%	260 45%	230 45%

Figure 4.28: Voc and FF Distribution for 0.65µm Thick CIGS Devices from Run C030

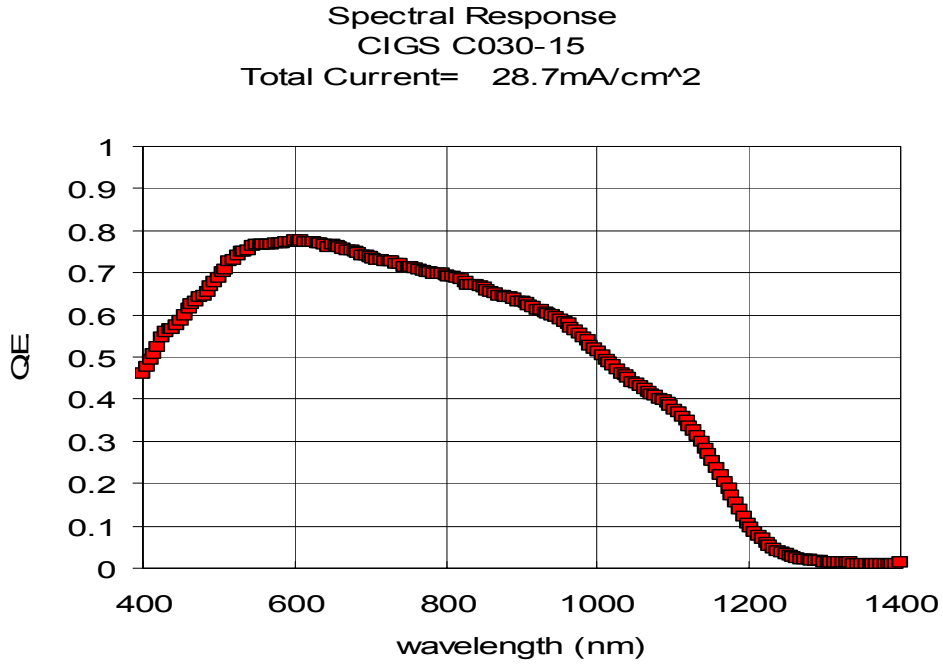

Figure 4.29: Typical Spectral Response of Devices in Run C030

It is likely that too much Gallium enters the space-charge layer and much of it is not bonded properly. These defects are highly likely near the interface. This could be one of the causes for low V_{oc}'s. Also, the QE spectrum as shown in figure 4.31, where it is compared with the standard, shows that there is an overall downward shift in the entire spectrum with somewhat higher loss in the red, causing a reduction in J_{sc}'s.

The devices fabricated with the thinnest absorber layer thickness also showed a drastic reduction in the width of the space-charge region. From C-V measurements, it was seen that the depletion width was only around 400-500 Å for these devices. Most of the electron-hole pairs will now be generated outside the depletion region and these carriers need to diffuse, so that the electric filed separates them. The I-V curves as shown in figure 4.30 show that the devices are shunted in light. The QE spectrum measured at zero bias shows that the J_{sc}'s are around 28 mA/cm^2. But, as forward bias is applied to the device, the already narrow depletion region reduces further. This would require the light generated electron-hole pairs to diffuse even more, for the electric filed to have an effect on them. And in this process, they may recombine before they can be collected which is why the currents reduce as the forward bias increases. Since the depletion width is too small, there could be significant tunneling recombination in the junction region that causes shunting, resulting in low V_{oc}'s [2]. This would also reduce the J_{sc}'s.

It could also be the effect of poor film quality as the thickness is reduced. Lundberg et al., [2] have found that the thin CIGS films have smaller grains and hence high grain boundary recombination which could also be the reason for low V_{oc}'s. Shunting can also be caused as the layer is made thinner, if the roughness of the film is of the same order as the film thickness. This would lead to non uniform coverage of the surface by CdS and ZnO which also result in shunting.

In the standard process, the Se flux is maintained at an average of 18 Å/s which is at least three times the amount needed for stoichiometric CIGS formation. This is because the sticking coefficient of Se at high temperatures is very low. Another reason for the high Se

flux during Selenization is to protect the surface of the CIGS film. By having excess Se pressure, any back evaporation of In from the substrate is prevented. However, since the Selenization time is also reduced in proportion to the thickness, the time for which the substrate stays at high temperatures is also reduced. Hence, it was decided to reduce the Se flux also during Selenization in C031. However, standard Se flux was maintained during deposition of the precursors. The devices fabricated with these conditions showed improved performance, but the performance was spotty i.e. non-uniform. The V_{oc}'s and FF's of C031 are shown in figure 4.32.

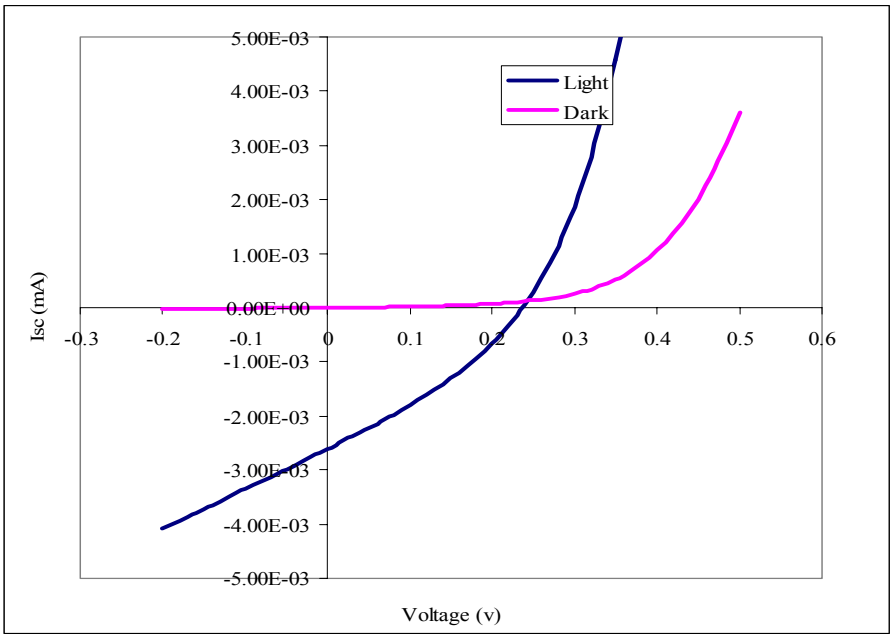

Figure 4.30: IV Curve of a 0.65µm Thick CIGS Device (C030-18)

Devices with 0.65µm thick CIGS layers were fabricated with the longer Selenization times also. It was found that longer Selenization times always proved bad for device performances irrespective of whether the Se flux during Selenization was high or low. Devices were also fabricated with much lower Se flux of 5 Å/s during Selenization.

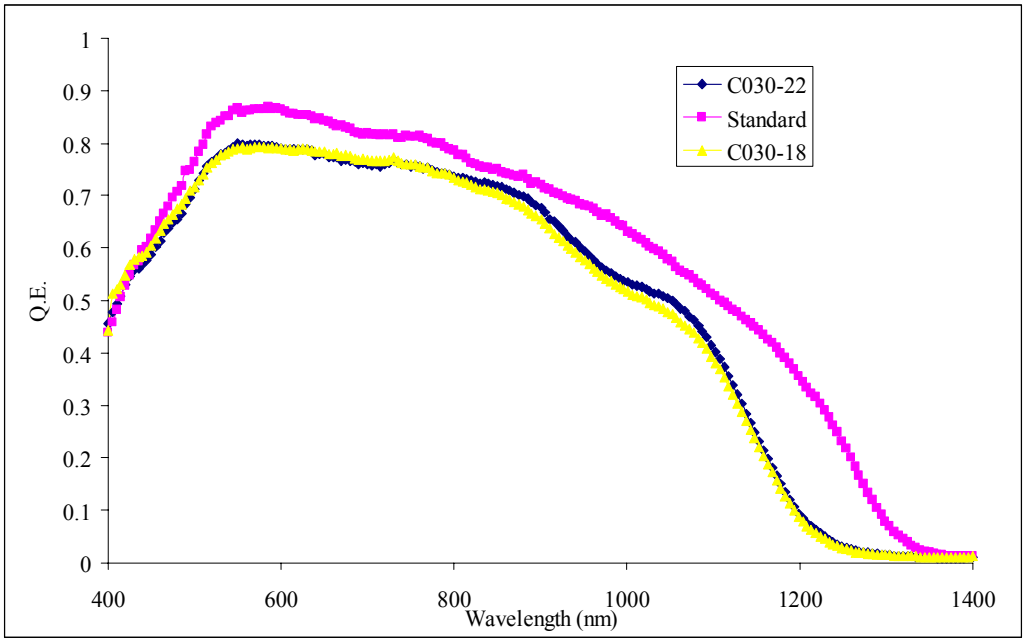

Figure 4.31: Spectral Responses of Standard and 0.65µm Thick CIGS Devices

160 29%	x	330 33%	350 43%	340 41%
430 63%	410 59%	400 54%	350 49%	410 59%
410 55%	320 51%	280 49%	370 49%	340 48%
370 53%	350 51%	400 54%	370 50%	270 41%
380 44%	400 50%	390 50%	350 50%	290 45%

Figure 4.32: Voc and FF Distribution for 0.65µm Thick CIGS Devices from Run C031

4.6 Stability of "Thin" CIGS Solar Cells

Devices with different CIGS layer thicknesses were tested for stability after a few weeks. It was found that the devices fabricated with standard (2µm), 1.5µm, 1.0µm thick CIGS layers showed similar performance. There were little or no changes in the V_{oc}'s and Fill Factors of these devices.

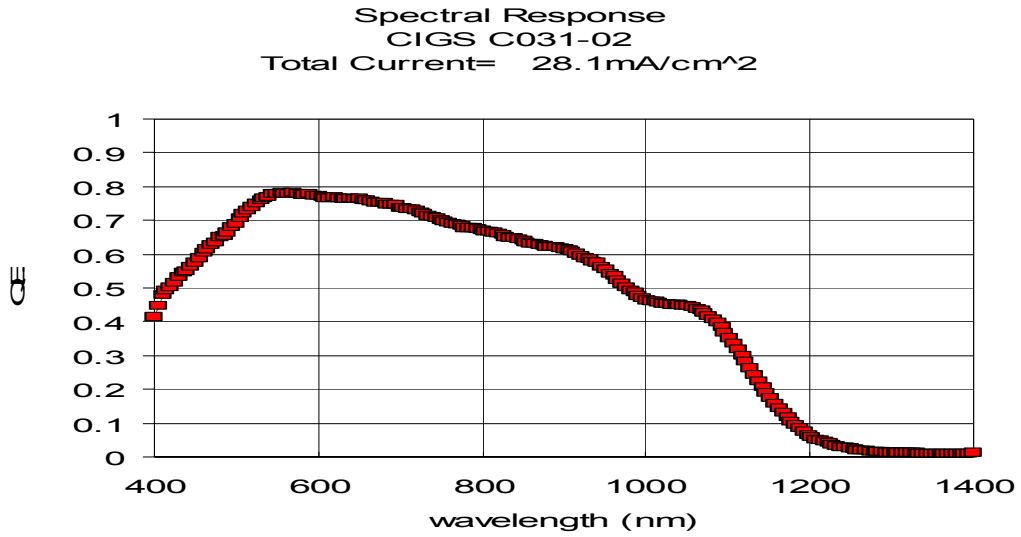

Figure 4.33: Typical Spectral Response of Devices in Run C031

On the other hand, major changes were observed for devices fabricated with 0.65µm thick CIGS layers. The devices fabricated with longer Selenization times had very poor initial performance. When measured after the sample was kept in the lab for a few weeks exposed to atmosphere, the devices showed slight improvement in V_{oc}'s, although the V_{oc}'s were only around 100-150 mV which is very less compared to our standard value. While these devices showed improvement, C031, the device that initially showed good performance degraded. The V_{oc}'s reduced to 200-250 mV when measured after a few weeks. It could be an effect of oxidation that is dominant at thickness levels which leads to an overall leveling in performance.

It was found that the device performance was always much lower than the standard. It was clear that we have fallen off the edge by reducing the thickness to 0.65µm.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS

Work done in this study can be grouped into three main categories. In the initial stages of this research, Zinc Oxide was developed as a front contact for CIGS solar cells. In the second stage, the effects of heat treatments at different stages of processing on the performance of devices were analyzed. In the final stage, the effect of absorber layer thickness on device performance was studied, and the thickness of the CIGS layer was successfully reduced to 1μm.

Bi-layer Zinc Oxide – The Transparent Conducting Oxide (TCO) Front Contact for CIGS based solar cells were developed and optimized. It was found during the course of this research that the Zinc Oxide as a layer and its interfaces were important for optimum device performance. Different methods of deposition were employed before obtaining the best performances. To start with, the intrinsic layer was sputtered using a pure Zinc Oxide target and the n-type layer was sputtered from an Al doped ZnO target. Initially, when only one gun was used to deposit both the intrinsic and Al-Doped layer, it was found that a vacuum break in between and its consequence, heating the substrate twice was found to be detrimental on device performance. It was then decided to use two separate guns to deposit the layers. Experiments carried out with this configuration showed that the position of the substrate with respect to the guns played an important role in device performance. It was found that, device performances were poor when the substrates were placed directly above the gun. It was concluded that the atomic/molecular bombardment by the high energy ions during sputtering, cause damage to the underlying layers thereby hurting device performance. Hence the substrates were moved in between the guns to avoid the bombardment and this improved the performances and this had a

positive effect on device performance. The effect of Oxygen partial pressure during i-ZnO deposition was varied and its effect on device performance was studied. The thickness of the intrinsic layer was also varied. Best performances were obtained for an i-ZnO that was 250 Å thick and sputtered with 0.1 mTorr Oxygen.

In the next step, both the intrinsic and doped layers were deposited from an Al doped ZnO target. Excess Oxygen pressure was used to achieve intrinsic behavior in the films deposited from the doped target. The effect of Oxygen pressure and the i-ZnO layer thickness was studied with this method also. Devices with currents of 37 mA/cm^2 were fabricated. But the Voc's on these devices were low around 370 mV. On the other hand, devices with Voc's of 450 mV were fabricated, but the currents on these devices were limited to 32 mA/cm^2. Clearly, compromise had to be made to achieve optimum values for both currents and voltages. With 0.4 mTorr Oxygen pressure and i-ZnO thickness of 350Å, open circuit voltages of 440 mV and short circuit current densities of 34 mA/cm^2 were obtained.

Heat treatment experiments were carried out on the devices at different stages of processing and also on completed devices. The maximum effect of annealing was on devices with high Cu/ Group III metal ratio. In all the cases, there was a drop in Voc, but the maximum drop was when the device was annealed right after CdS deposition in vacuum. This effect was diminished when the device was annealed in air. It is suspected that the air ambient acts as a barrier layer to the losses. It was found that there was drop in currents also. The primary cause for the loss in currents was the i-ZnO layer, although there were some contributions from the CdS layer. It was found that the unfavorable interfaces were the main factor for reduction in current. It was found that if the CdS layer was protected by the i-ZnO layer, it will not deteriorate.

The main reason for the drop in V_{oc} in the high Cu/ Group III region was found to be the thin layer of top Copper that is deposited during Selenization. Though it is deposited when the substrate is at a high temperature, it has less time to react and hence it is

expected that not all of this Cu is bonded and some of this may move and react unfavorably with post-deposition annealing. It is expected that this Copper could fill metal vacancies in the CdS and i-ZnO layers which would alter the location of Fermi levels in these films and hence lower the effective contact energy. This could explain the drop in V_{oc}. Although the loss in Jsc's could be explained by unfavorable interfaces, more experiments need to be done in order to confirm this.

Devices with CIGS layers thinner than the standard thickness values were fabricated. The thickness of the CIGS layer in the standard devices is 2μm. The thickness of this layer was reduced to 1.5μm. It was found that the V_{oc}'s were higher than that of the standard devices. However, there was some loss in J_{sc}'s. The main reason for this drop was an overall drop in the QE spectrum which is suggestive of the interface.

The thickness of the CIGS layer was reduced to 1μm in the next experiment. The V_{oc}'s were significantly higher than the standard devices, the maximum being 470 mV. The J_{sc}'s dropped even more than the 1.5μm devices. It was seen that there was no more contribution from the interface, which caused the loss in J_{sc}'s. The loss in current was primarily due to the increase in band-gap of the devices. Perhaps, the increase in band-gap indicates that the extra Ga that might have reached the interface, bonded instead. In order to compensate for the extra Ga, which causes the increase in band-gap, devices with more Indium were fabricated. This would cause the Cu/ group III ratio to be less than unity and the effect would be more pronounced towards the In side. It is known that best device performances are obtained when the ratio is close to unity and drops off on either side. If this were to apply, the device performance should have reduced towards the In side. But, it was found that the devices rather got better towards the In side. It is not clear why this is the case and more experiments are needed to understand the phenomenon. Also, the band-gap of the devices did not change form the increased value. In fact, all the devices fabricated with this thickness i.e. 1μm had a larger band-gap than the thicker devices. Devices were also fabricated on thicker Mo layers to understand the effect of Sodium on the device performance at this thickness. However, no significant change was

observed when the Mo thickness was increased to 1.5µm form the standard 1µm. Best device performances were obtained when the Selenization time was 22 minutes. The J_{sc}'s were around 30 mA/cm^2 and V_{oc}'s were around 470 mV.

The thickness was reduced further down to 0.65µm. The initial performance of these devices was considerable, although less when compared to the standard values. There was also a further increase in band-gap of the devices. The data from all the experiments showed that the increase in band-gap was because of the following effect. It is known that Ga tends to accumulate towards the back contact. When the thickness of the CIGS layer is reduced, the space-charge region is moved more towards the back contact which causes more Ga to enter the space-charge region. This causes the increase in band-gap. It was found that when the thickness of the CIGS layer was reduced, there was some reduction in the width of the space-charge region. However it was still large enough for the effect of Ga incorporation to be observed. But, when the thickness was reduced to 0.65µm, device performances were affected to a great extent. The V_{oc}'s and J_{sc}'s were significantly lower. The space-charge region was very narrow extending only a few hundred Angstroms. As the thickness is reduced by a factor of 3 compared to the standard, there could be significant back contact recombination. The devices were electrically shunted when the thickness was reduced to 0.65µm. Also, at this thickness, there could be too much Ga entering the space-charge layer and much of it is not bonded properly which affects the V_{oc}'s. The IV curves of these devices show significant collection problems also. The J_{sc}'s also reduced due to the increase in band-gap of the devices and unfavorable interface effects. Hence it was concluded that thickness of 0.65µm affects the performance of the devices to a large extent.

To understand the reason for the loss in currents, devices with CIGS layers thicker than the standard were fabricated. The maximum currents were around 32 mA/cm^2 for these devices. This is close to the standard devices, but on the lower end. The V_{oc}'s were also lower than the standard by 20-30 mV. The V_{oc} increases as the thickness of the absorber is reduced, but the Jsc's reduce as the thickness is reduced. Both these trends were

observed to apply over a range of thickness values and dropped on either side. Hence there is a limit to which the thickness can be reduced.

It was found that the CIGS/ CdS and CdS/ ZnO interfaces are very important for the optimum performance of the devices. The conductivity of the interface layers also affects the performance. An important factor contributing to the interfaces is thought to be the thin layer of Top Copper. More experiments have to be carried out to understand the effect of the thickness of top copper on device performance, especially when the absorber layer thickness is reduced.

In this work, the thickness of the CIGS layer was successfully reduced to 1μm. The thickness of the absorber layer in these devices has been reduced by half, and plausible performance was achieved. Devices with V_{oc}'s as high as 470 mV, Jsc's of 30 mA/cm^2 and Fill Factors of 0.61 were fabricated. Though the thickness is reduced by a factor of 2, the device performances were still close to the standard performance values. It has been found by other research groups that, by creating what is called a Back Surface Field, typically realized by depositing a thin layer of CGS on Mo before CIGS, could improve the performance of the devices with extremely thin absorber layers. However, this is significantly different from what has been done here and hence, can have other effects also.

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