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Growth of 3C-SiC on (111)Si using Hot-Wall Chemical Vapor Deposition

by

Christopher Locke

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Engineering Science
Department of Electrical Engineering
College of Engineering
University of South Florida

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Keywords: silicon carbide, heteroepitaxy, crystal defects, chemical vapor deposition, polysilicon

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Growth of 3C-SiC on (111)Si using Hot-Wall Chemical Vapor Deposition

Christopher Locke

ABSTRACT

The heteroepitaxial growth of cubic silicon carbide (3C-SiC) on (111) silicon (Si) substrates, via a horizontal hot-wall chemical vapor deposition (CVD) reactor, has been achieved. Growth was conducted using a two step process: first the Si substrate surface is converted to SiC via a carbonization process and second the growth of 3C-SiC is performed on the initial carbonized layer. During carbonization, the surface of the Si is converted to 3C-SiC, which helps to minimize the stress in the growing crystal. Propane (C_3H_8) and silane (SiH_4), diluted in hydrogen (H_2), were used as the carbon and silicon source, respectively. A deposition rate of approximately 10 μm/h was established during the initial process at a temperature of ~1380 °C. The optimized process produced films with X-ray rocking curve full-width at half-maximum (FWHM) values of 219 arcsec, which is significantly better than any other published results in the literature. Once this process was developed a lower temperature process was developed at a slower growth rate of ~2 μm/h at 1225 °C. The crystal quality was inferior at the reduced temperature but this new process allows for the growth of 3C-SiC(111) films on oxide release layers for MEMS applications. In addition, for electronic device applications, a lower

temperature process reduces the generation of defects caused by the nearly 8 % mismatch in the coefficient of thermal expansion (CTE) between 3C-SiC and Si. Finally a new process using a poly-Si seed layer deposited on an oxide-coated Si wafer was used to form 3C-SiC films for MEMS applications. The results indicated initially that the films may even be monocrystalline (based on X-ray evaluation) but later analysis performed using TEM indicated they were highly-ordered polycrystalline films.

The grown 3C-SiC films were analyzed using a variety of characterization techniques. The thickness of the films was assessed through Fourier Transform infrared (FTIR) spectroscopy, and confirmed (in the case of growth on poly-Si seed layers) by cross-section scanning electron microscopy (SEM). The SEM cross-sections were also used to investigate the 3C-SiC/oxide interface. The surface morphology of the films was inspected via Nomarsky interference optical microscopy, atomic force microscopy (AFM), and SEM. The crystalline quality of the films was determined through X-ray diffraction (XRD).

CHAPTER 1: INTRODUCTION

1.1 Silicon Carbide Overview

Silicon carbide (SiC) is a wide-bandgap semiconductor material exhibiting mechanical and electrical properties suitable for fabricating devices for use in high-temperature and corrosive environments, high-power switching applications, high mechanical wear conditions, and possibly *in vivo* bio-sensors. Unlike silicon-based electronics, which can only withstand temperatures up to 250 °C, SiC-based devices can operate at temperatures up to 650 °C (Shenai 1989).

Silicon carbide can exist in many different crystal structures depending on growth conditions, a phenomenon called polytypism. Polytypism is a special case of polymorphism, in which the crystal structures between two polymorphs differ only in the way identical, two-dimensional layers of close-packed layers are stacked. In the case of SiC, polytypes vary by the different stacking sequences of the tetragonally-bonded Si-C subunits, with more than 200 polytypes known to exist (Foll 2006). However, an overwhelming majority of electronic materials research is concerned with only 3 of these polytypes : 4H-SiC, 6H-SiC, and 3C-SiC. The 4H, 6H,and 3C designation, called the Ramsdell notation, is the most wide-spread method of identifying polytypes (Foll 2006). The number-letter prefix designates the quantity of close-packed Si-C layers required for each unit cell and whether the polytype is a hexagonal (H), cubic (C), or rhombohedral

(R) crystal system. For example, 4H-SiC indicates a hexagonal crystal system comprised of a repetitive, uniquely-ordered stacking sequence of four Si-C subunit layers.

The hexagonal close-packed structure is a main reason for the high stability of the hexagonal SiC polytypes. The 4H-SiC polytype has the highest stability due to the alternating cubic and hexagonal layers (Park, et al. 1994). 6H-SiC has a low, anisotropic electron mobility, while 4H-SiC has a much higher electron mobility and is less anisotropic, i.e. less directionally dependent (Casady and Johnson 1996). Thus 4H-SiC is, at present, the most commonly used polytype for electronic devices (Saddow and Agarwal 2004).

Unlike the more commonly studied 6H-SiC and 4H-SiC polytypes, 3C-SiC has the ability to be heteroepitaxially grown on Si, allowing for the growth of SiC on large area substrates. Si wafers are inexpensive and are currently manufactured as large as 12 inches in diameter. 3C-SiC could be epitaxially grown on large-area Si wafers to produce seeds for bulk growth. Currently, only bulk SiC is available in the 4H and 6H polytype with boule sizes capable of producing a maximum 4 inch size wafer at a cost of nearly $2000-$2500 per wafer (Cree Inc. 2009). Futhermore, bulk SiC grown by physical vapor transport contains screw dislocation densities near 50-200 cm^{-2} that can penetrate into the epitaxial layer during growth and lead to device failure. Because of the cubic crystal structure of 3C-SiC, these screw dislocations are energetically unfavorable and do not in occur in 3C heteroepitaxy.

Unfortunately, the heteroepitaxial growth of 3C-SiC on Si is exacerbated by a 20% lattice mismatch and 8% coefficient of thermal expansion (CTE) between Si and 3C-SiC (refer to Table 1.1), which leads to in-plane stresses in the film. Often the atomic bonds along these crystal planes will break and reform to relieve film stress, leaving behind

dangling bonds which are referred to as misfit dislocations (Smith 1995). Further information on crystallographic defects and the methods of reducing and eliminating them can be found in section 2.2. Another disadvantage of heteroepitaxy is the 8% difference in thermal expansion coefficients between 3C-SiC and Si. These are a few of the material growth-related issues that must be addressed before 3C-SiC can be realistically considered as a replacement for Si based electronic devices.

High-temperature device applications are not generally possible using Si due to its narrow bandgap of 1.12 eV. At elevated temperatures, the thermal generation of electron-hole pairs exceeds the number of dopant-provided free carriers, leading to device failure (Zetterling 2002) The thermal generation of electron-hole pairs is much lower in SiC than in Si due to its wider energy bandgap (3.2 eV at room temperature for the 4H-SiC polytype). The difference in the intrinsic carrier concentration, n_i, between Si and SiC, is 19 orders of magnitude (i.e., 10^{19}), which enables higher temperature applications using SiC. As seen in Table 1.1, the bandgap values for SiC are more twice that of Si with the resulting values of intrinsic carrier concentration being several orders of magnitude lower. The intrinsic carrier concentration is proportional to the decaying exponential of the bandgap value. As a result, n_i is substantially lower for SiC than Si.

Table 1.1 Properties of commonly used SiC polytypes compared with Si. (Casady and Johnson 1996) (Harris 1995).

Property	4H-SiC	6H-SiC	3C-SiC	Si
Energy bandgap at 300K (eV)	3.20	3.00	2.29	1.12
Intrinsic Carrier Concentration at 300K	$5x10^{-9}$	$1.6x10^{-6}$	$1.5x10^{-1}$	$1x10^{10}$
Critical breakdown electric field	2.2	2.5	2.12	0.25
Saturated electron drift velocity (x 10^{7}	2.0	2.0	2.5	1.0
Thermal conductivity (W/cm-K)	4.9	4.9	3.2	1.5
Electron mobility (cm^2/V-s)	1000	600	800	1450
Hole mobility (cm^2/V-s)	115	100	40	470
Thermal Conductivity (W cm^{-1} K^{-1})	3.7	3.6	3.2	1.49
Lattice constant (a, c in Å)	a=3.0730 c=10.053	a=3.0806 c=15.1173	a=4.3596	a=5.43095
Elastic coefficient* (GPa) *calculated	C_{44}=600	C_{11}=500 C_{12}=92 C_{44}=168	C_{11}=352 C_{12}=120 C_{44}=233	C_{11}=167 C_{12}=65 C_{44}=80

The dissipation of heat in a high-power device is critical to the reliability of that device (Powell and Rowland 2002). When the material is heated, the physical properties often change. For example, the carrier mobility decreases with increasing temperature and the intrinsic carrier concentration increases, which may cause the device to fail (Saddow and Agarwal 2004). Since the thermal conductivity of SiC is greater than three times that of Si, the heat can flow more readily from hot spots in the SiC-based device to the package compared to Si and other semiconductors (Masri 2002).

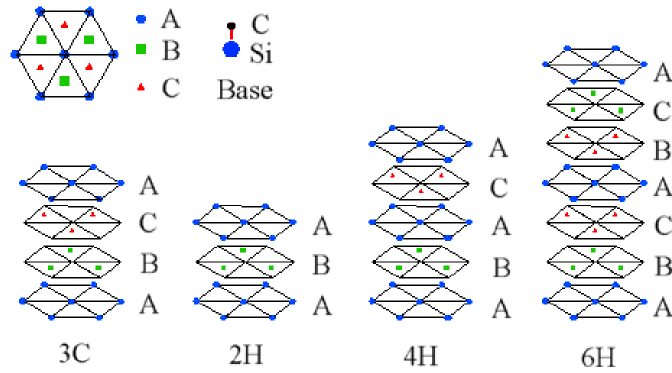


Figure 1.1 Four examples of SiC polytype stacking sequences. Each point represents a lattice point on which the Si-C basis is attached. Each layer is the close packed plane of the crystal system and is differentiated by "A", "B", or "C", which is determined by the relation of each layer's lattice point positions to the interstitial spaces of the other layers (Saddow and Agarwal 2004).

The 'A', 'B', and 'C' labels in Figure 1.1 denote the position of the lattice points, a collection of periodic points in space, on which the Si-C subunits are located. As seen in Figure 1.1, 4H-SiC has a stacking sequence of ABCB, or 4 layers, therefore the designation is 4H. This structure has an equal number of cubic and hexagonal lattice sites. The 6H-SiC structure has 6 stacking layers before the sequence repeats ABCACB, and, finally, 3C-SiC is a continuation of the ABC stacking sequence which has purely cubic symmetry. Due to differences in stacking sequence, the electrical, mechanical and optical properties vary for each polytype of SiC, as shown in Table 1.1.

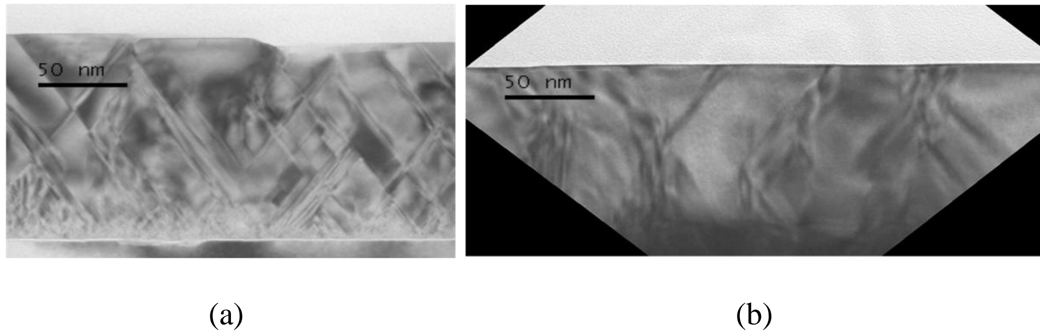
1.2 Motivation for 3C-SiC Growth on (111)Si Substrates

Silicon wafers oriented in the <100> direction are often the substrate of choice to grow 3C-SiC due to its wide-spread availability, it's resilience to mechanical bowing and fracturing from in-plane substrate/film stress, and the ability to produce good quality epitaxial films. However, the surface morphology of 3C-SiC grown on (100)Si substrates

is subject to a mosaic pattern of terraces bounded by {111} planes forming sloped sides. These are believed to be the result of stacking faults, micro-twins, and anti-phase boundaries (APBs) propagating along the four equivalent {111} planes and terminating on the surface of the crystal. As a result, the three-dimensional topography generated on the surface of the epitaxial layer can lead to device fabrication difficulties.

3C-SiC grown on <111> oriented Si substrates, on the other hand, are prone to wafer bow, fracturing, and film delamination. As long as the films are thinner than ~2µm, these maladies can be minimized. However, XTEM and plan view TEM analysis of thin 3C-SiC films grown on (111)Si indicates that the films have significantly fewer stacking faults than corresponding 3C-SiC films grown on (100)Si substrates. The surface morphology of (111)3C-SiC is very smooth, devoid of the mesa-like features seen on (100)3C-SiC (Figure 1.2). This could be a result of the defects common to epitaxial 3C-SiC growth, i.e. stacking faults and twins, which tend to form along the {111} planes, developing parallel to the growth plane. Preliminary hardness measurements performed by A. Volinsky in the Department of Mechanical Engineering via nanoindentation with a Berkovich tip indicate the possibility that (111)3C-SiC films may be 50% harder than (100)3C-SiC films of similar thickness. The (111) surface of 3C-SiC is similar in atomic arrangement to 4H-SiC which has been used recently to form graphene layers. Graphene is a very high conductivity film that is being researched as a next-generation electronic device and has been formed on the basal planes of 4H and 6H-SiC either through silicon sublimation or the deposition of thin layers of carbon (Fanton, Robinson and Weil 2009). The hexagonal configuration of carbon in these planes is

believed to serve as a good template for the formation of sp^2 bonds between C atoms (Fanton, Robinson and Weil 2009). The (111) surface of heteroepitaxially grown 3C-SiC also displays low surface roughness needed to produce large graphene crystals and high electron mobility which can be impeded by strain and graphene crystal misorientation (Fanton, Robinson and Weil 2009).



(a) (b)

Figure 1.2 Cross-section TEM data of 3C-SiC grown on (a) (100)Si and (b) (111)Si. Note the more flat surface morphology and lower defect density of the 3C-SiC(111) film. TEM image courtesy of C. Buongiorno, IMM-CNR, Catania, Sicily (IT).

The SiC Group at the University of South Florida has been investigating the optimization of the new process of growing thin-film 3C-SiC on a polycrystalline Si (poly-Si) seed layer CVD-deposited on a CVD-deposited SiO_2/ Si (111) stack. The CVD deposited polycrystalline Si seed layer appears to exhibit a highly textured grain structure, in other words, the polycrystalline grains are oriented in a preferred direction. The texturing of the polycrystalline Si layer is very sensitive to the deposition temperature. It is reported that the films are deposited favoring the <110> orientation and, once annealed, tend to arrange in the <111> orientation (Parr and Gardiner 2001). Growing the 3C-SiC via the poly-Si seed layer on an oxide release layer will provide a

versatile substrate for the fabrication of free-standing, highly-crystalline 3C-SiC MEMS structures with low residual stress.

1.3 3C-SiC CVD Heteroepitaxy on (100)Si Substrates

Epitaxy is the growth of a thin layer on a crystal substrate in which the substrate is a template for the growth. Heteroepitaxy is the growth of an epitaxial layer on a seed crystal of a different type. Cubic SiC may be heteroepitaxially grown on Si substrates.Since the growth of single crystal, large-area, bulk 3C-SiC crystals has not been demonstrated heteroepitaxy is needed to grow 3C-SiC crystals. However, the near 20% lattice mismatch between Si and SiC leads to an epitaxial film that is highly defective and therefore not suitable for electronic devices. This is generally because interfacial defects propagate into the 3C-SiC device layer and result in high leakage currents in 3C-SiC/Si devices. Indeed, the issues impeding the growth of high quality, monocrystalline 3C-SiC/Si have proven to be so difficult to overcome that many groups have abandoned 3C-SiC/Si. In this thesis, we aim to use novel patterned substrates to mitigate and/or eliminate these defects with the goal of developing device-quality 3C-SiC/Si layers.

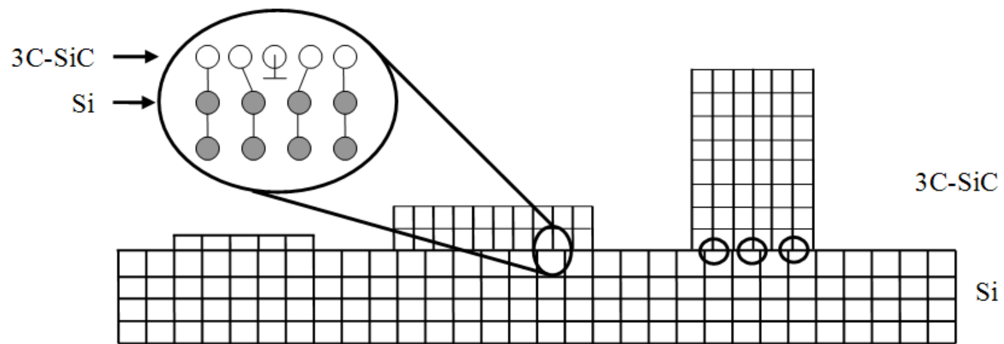


Figure 1.3 Illustration of the affect of lattice mismatch in heteroepitaxy. The ⊥ symbol denotes the location of a missing row of atoms which is known as a line defect. Note the stretched and compressed covalent bonds at the interface resulting from the lattice mismatch between the two crystals.

As seen in the figure, there is a strain in the epilayer from an attempt by the epilayer ($a_{3C\text{-}SiC}$ = 4.3596Å) to accommodate the substrate's lattice constant (a_{Si} = 5.43095Å) (Harris 1995). The attempt to accommodate the mismatch not only produces defects, but these defects in the epitaxial layer have a mosaic morphology in the case of the 3C-SiC/Si system. While a carbonization step is normally employed which converts the Si surface to SiC and acts as a buffer layer to reduce this stress, this does not completely accommodate the mismatch. With this buffer layer, there are still a fair amount of dislocations which must be reduced if 3C-SiC is to be realized for fabrication.

One of the most successful methods to grow 3C-SiC is by chemical vapor deposition (CVD). The standard precursor chemistry typically used is the silane-propane-hydrogen gas system. Although extensive work has been performed for decades since the early 1980's, there is still a lack of good quality 3C-SiC on Si epitaxial material. While

growth rates up to 40 μm/h on undulant Si (100) substrates by cold-wall CVD have been reported to produce SiC substrates with near bulk quality, defects originating from the undulant substrate persist (Nagasawa, Yagi and Kawahara 2002). More relevant for device manufacturing were studies performed using hot-wall CVD, which resulted in growth rates up to 50 μm/h (Reyes, spring MRS 2006).

1.4 Summary of Organization of Thesis

SiC demonstrates roboust electrical, chemical, and mechanical performance suitable for use in harsh environments where Si-based devices would fail. Unfortunately, the chemical inertness is a double-edged sword; a desirable property for device application becomes a hinderance for the processing of SiC films. Coupled with the inherent problems of heteroepitaxial growth, new techniques to reduce or eliminate these issues must be investigated if SiC is to be realized as the preferred fabrication material for harsh environment devices. Chapter 2 will discuss the principles of CVD growth and hardware since chemical vapor deposition is the primary means of growing cubic SiC. An overview of crystal defects that are commonly found in the heteroepitaxial growth of 3C-SiC on Si will then be presented. The development of a low temperature heteroepitaxial process for growth of 3C-SiC films with reduced residual stress and a brief discussion of the characterization techniques to analyze the films will follow in Chapter 3. In Chapter 4, the benefit of using compliant substrates for heteroepitaxy will be discussed, focusing primarily on 3C-SiC growth on the poly-Si/ SiO_2/ (111)Si compliant stack. Finally, future research exploring 3C-SiC growth on a variety of novel

compliant substrates and the characterization techniques used to quantify the residual stress present in the films will be presented in Chapter 5.

CHAPTER 2: HOT-WALL CHEMICAL VAPOR DEPOSITION

2.1 Overview of CVD

Chemical vapor deposition (CVD) is a technique in which a solid film is formed onto a surface by a chemical reaction emanating from vapor phase precursors. The chemical reactions generally undergo activation by ohmic heating, RF induction heating, plasma, or light. It is a technique often employed for the uniform growth of high quality thin films. The common types of CVD techniques are 1) Organometallic Vapor Phase Epitaxy (OMVPE) 2) Plasma Enhanced Chemical Vapor Deposition (PECVD) 3) Photo CVD 4) Low Pressure CVD and 5) Atmospheric Pressure CVD. Chemical vapor deposition involves a series of sequential steps beginning with the vapor phase and progressing through a series of quasi steady-state reactions which culminate in the development of a sold film. The progression from vapor phase to film growth can be summarized by the following sequence of events. First, the gaseous reactants diffuse through the boundary layer to the surface. Second, the reactants adsorb on the surface and then usually undergo some surface migration to reach a reaction site (i.e., dangling chemical bond). Third, the reactants undergo a chemical reaction which may be catalyzed by the surface. Fourth, the reaction by-products undergo desorption from the surface. Fifth, the reaction by-products diffuse through the boundary layer, enter the gas stream and are exhausted out of the reactor. Finally, the condensed product is

incorporated into the structure of the developing film. The process is summarized in Figure 2.1 below.

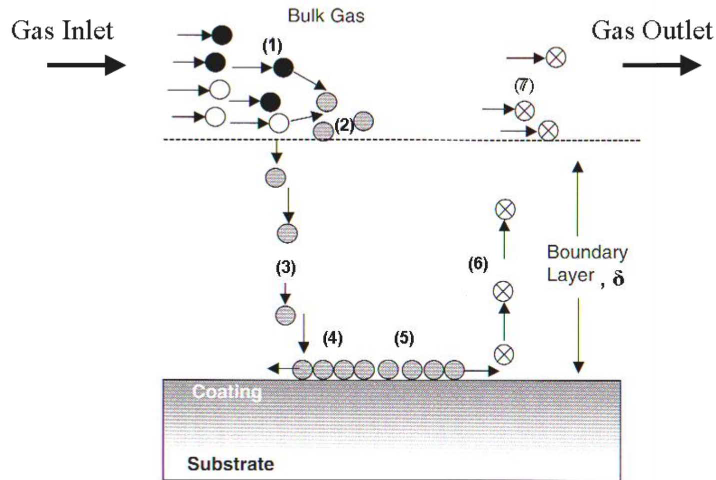


Figure 2.1 Schematic diagram of mechanistic steps which occur during the CVD process. (1) Gas inlet, (2) dissociation of reactants, (3) diffusion of reactants to the surface, (4) adsorption of reactants to the surface, (5) heterogeneous surface reaction, (6) desorption of by-products, (7) diffusion of by-products back into the bulk gas. (Park and Sudarshan 2001)

Although many rate-limiting steps are known to exist, the deposition rate of CVD processes is primarily governed by mass transport and surface kinetics. These two rate limiting steps can be controlled by several process parameters. The temperature and pressure of the reaction environment greatly impact the deposition process. The pressure controls the thickness of the boundary layer and, as a result, affects the rate of the reactant and product diffusion (Sivaram 1995). At low pressures, the boundary layer is thinner, which minimizes the diffusion time across the region. This is known as a transport-limited CVD regime; where the rate of deposition is limited by the diffusion of reactants to the surface and is less sensitive to temperature (Sivaram 1995). If the temperature is low, then an oversupply of reactants is created due to the molecules

reacting slowly (Sivaram 1995). If the temperature is high, then the surface reactions take place quickly and the reaction rate is limited by the diffusion of molecules. The growth regime (transport-limited or surface reaction-limited) is determined by the slowest process (diffusion or chemical reaction) (Smith 1995). Figure 2.2 illustrates how both the temperature and pressure during CVD affects the growth rate.

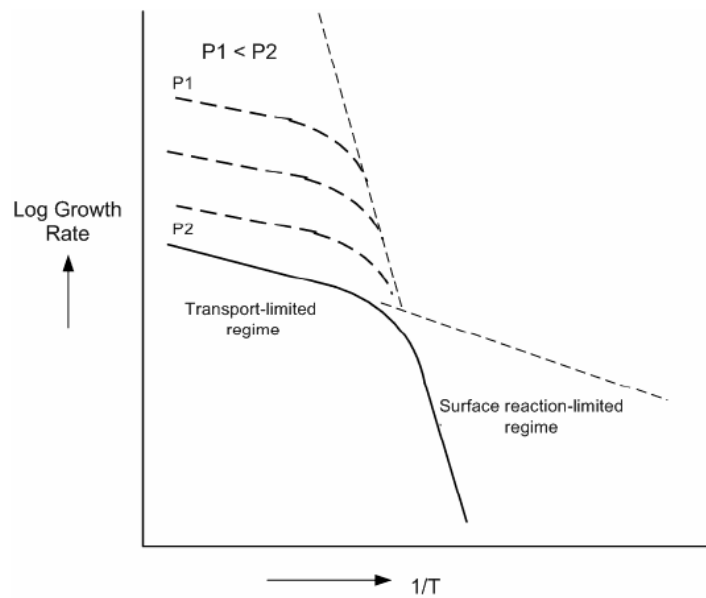
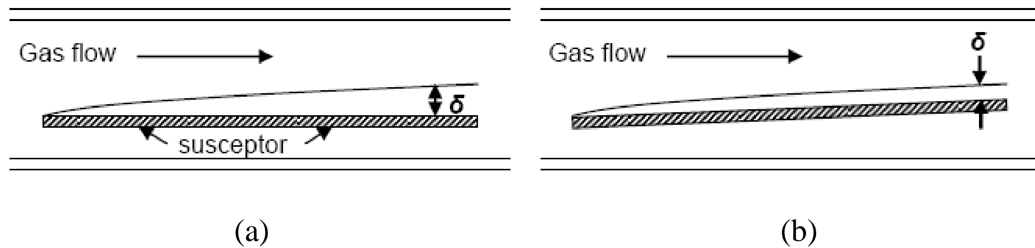


Figure 2.2 Dependence of process temperature and pressure on growth rate via CVD. (Smith 1995).

Another important process parameter that influences reaction rate is gas velocity. The CVD process involves the transport of precursor gases through the use of a carrier gas, which usually flows in a laminar manner although occasionally has some turbulence (Park and Sudarshan 2001). When a fluid flows over a stationary surface, a thin layer of fluid immediately above the surface is stationary. This is known as the boundary layer and is inversely proportional to the gas velocity and directly proportional to the fluid

viscosity and pressure. In a horizontal CVD reactor design, the boundary layer increases along the direction of the carrier gas flow, which leads to an exponential decrease in the deposition. Tilting the susceptor increases the gas velocity by continuously decreasing cross-sectional area and thus reduces the thickness of the boundary layer along the flow direction (Rossi 1988). Figure 2.3 illustrates these principles.



(a) (b)

Figure 2.3 Illustration of the boundary layer, δ, in a horizontal reactor with: (a) flat susceptor design, and (b) tilted susceptor design. (Pierson 1999)

2.1.1 Early Stage of Thin Film Growth

The initial stages of film growth are characterized by three major phenomena which occurs independent of the type of film growth technique. The material must first condense out of the vapor phase and nucleate on a substrate. The reactant species impinging on the surface is attracted to the substrate by the London dispersion forces of the substrate atoms. The probability that an impinging atom will be adsorbed onto the surface is related to a quantity called the sticking coefficient, which is the ratio of the amount of material condensed on the surface to the total amount of impinging atoms, see Figure 2.1 (Sivaram, S 1995). Once an atom is adsorbed onto the surface it must overcome a surface binding energy, Q_{desorb}, in order to leave the surface. Given the

vibrational frequency, ν, of the adsorbed atom, the length of time, τ_s, that an atom stays on the surface is expressed by,

$$\tau_s = (1/\nu)*\exp(Q_{desorb}/kT) \qquad (2.1)$$

When Q_{desob} is large in comparison to kT, the adsorbed atom will spend a long time on the surface, so the chance of the atom being incorporated on the surface is high (Sivaram, S 1995). When the energy of the surface atoms is on the order of kT, then the adsorbed atom will have a high probability of being desorbed. Once incorporated onto the surface, the condensed atoms or molecules tend to aggregate and form small clusters on the surface of the substrate, a process called nucleation. These small clusters are in a constant free energy struggle between the releasing free energy when forming a cluster and having to pay energy cost when forming a surface interface between two distinct phases. Small clusters are unstable if the energy released from the formation of its volume cannot sustain the creation of its surface. Once the clusters have reached a critical size, any addition of molecules to the cluster releases energy instead of costing energy and nucleation growth can be sustained. Then the randomly formed nucleation sites reach a saturation density and undergo island coalescence via the diffusion and continuing capture of adatoms. This saturation point occurs when the internuclear distances are on the order of the mean surface diffusion length. As the islands grow, they assimilate subcritical nuclei and coalesce with other islands, forming a connected network. Eventually, the steady-state growth above the first layer occurs. However, CVD processes add an additional step to the film growth process; a chemical reaction among the surface-adsorbed reactants occurs at the gas-substrate interface. Whereas

simple condensation is always exothermic, a majority of CVD reactions are endothermic which means they must usually wait until they interact with the heated substrate. Another important feature of the CVD process that complicates this general growth sequence is that the intrinsic impurities, in the form of reaction products, need to be considered in the vicinity of the film growth (Sivaram, S 1995).

2.1.2 Overview of Heteroepitaxial Defects

Given the nature of heteroepitaxy, i.e. growing a crystalline material on a different crystalline material (substrate), it is nearly impossible to generate a perfect, mono-crystalline film. Other than the introduction of impurities from contamination, the common source of extrinsic crystal defects found in heteroepitaxy stems from a mismatch between the lattice constant and the coefficient of thermal expansion between the substrate and film. These disparities create line defects, such as dislocations, or planar defects as is the case for micro-twins, stacking faults, and grain boundaries.

Dislocations are linear defects resulting from the deviation of atoms from the lattice site positions of the crystalline structure. The disruptions of the atomic arrangement associated with dislocations typically extend through the structure along a line. Dislocations that commonly occur in heteroepitaxy are edge, screw, and misfit.

2.1.2.1 Edge Dislocation

Edge dislocations can be thought of as a disturbance originating from the insertion or removal of a partial plane of atoms from the structure. The region at the end of the

partial plane, where the atomic arrangement maximally deviates from the normal lattice sites, is called the dislocation line. The surrounding region is the dislocation core, which is an area of large strain and dangling bonds that runs alongside the dislocation line. The energy of propagation for an edge dislocation is much lower than the total bond energy of the atoms lying in the propagation plane. This is explained by the fact that an edge dislocation proceeds through a crystal peristaltic fashion. At any given moment, only one bond is broken while the atoms surrounding the dislocation are distorted from their equilibrium positions.

2.1.2.2 Screw Dislocation

Another type of dislocation that is closely related to the edge dislocation, but is not seen in 3C-SiC heteroepitaxy, is the screw dislocation. This dislocation is often thought of as a crystal system which has been subjected to shear stress sufficient enough to overcome the elastic limits of the crystal. The result is the shifting of one side of the crystal relative to the other side by one or more lattice constants. In this case, the dislocation line runs in the direction of the shift. Referencing the atoms located within a plane perpendicular to the dislocation line, if an attempt is made to form a closed path around the dislocation line by connecting the atoms together, a helix will be formed. The once parallel planes of the crystal are now joined by a helical path; this is why this type of dislocation is referred as a screw dislocation.

2.1.2.3 Misfit Dislocation

In the case of heteroepitaxy dislocations, called misfit dislocations, form at the interface of two crystals with different lattice constants. In an attempt to minimize the interatomic bonding strain induced by the lattice mismatch, the atomic planes of the thin film will be distorted at the interface and will no longer be equally spaced. The roughly equidistant points along the interface where the lattice deviations are the greatest correspond to the misfit dislocations. If the heteroepitaxial film has a coefficient of thermal expansion different than the substrate, then when temperature changes occur, usually during post-growth cooling, misfit dislocations occur in order to relieve in-plane stress present near the film-substrate interface.

2.1.2.4 Planar Defects

Planar defects correspond to disturbances of the crystal structure resulting from the two dimensional deviation of atoms from their corresponding lattice sites. Planar defects commonly found in heteroepitaxial films are stacking faults (SF), twins, antiphase boundaries (APB), and double position boundaries (DPB).

Stacking faults occur when a mistake occurs in the stacking sequence of the planes of atoms along certain directions. If planes of densely-packed spheres (atoms) are to be stacked on each other, one finds that there are two sets of interstitial spaces to place the next densely-packed plane. As a result, it is possible to lay three planes in succession without the co-alignment of interplanar atoms. In a perfect crystalline structure, a stacking sequence will eventually repeat in a periodic fashion. The face-centered cubic

(FCC) structure is created when the stacking sequence repeats as ABCABC…and the hexagonal close packed (HCP) structure is created from the sequence ABABAB… In the case of the zinc blende structure of 3C-SiC, it is not unusual to see stacking errors occur in the stacking of the {111} planes since the nearest-neighbor bonding is not affected by stacking faults. In fact, the energy associated with stacking faults is very low when compared to other planar defects since the defect is only due to the nearest-neighbor arrangement and not disturbances of the crystal structure. This mistake may arise during the film growth or when plastic deformation has occurred to the film. Figure 2.4 shows a plan-view TEM micrograph of the stacking faults present in a 3C-SiC film grown heteroepitaxially on (100)Si.

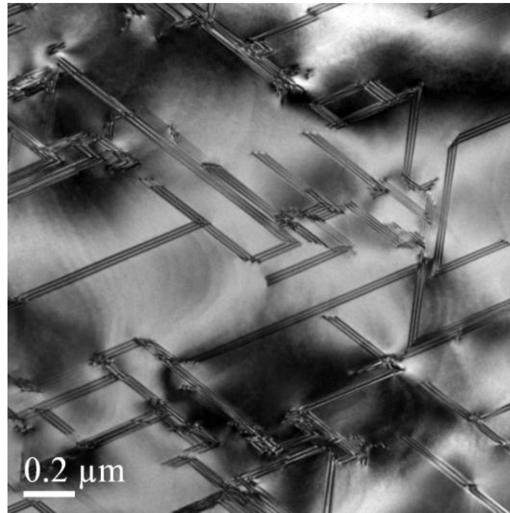


Figure 2.4 Stacking faults revealed via PV-TEM. SF density estimated to be ~ $5x10^4$ cm^{-1}. Data provided by C. Buongiorno, IMM-CNR, Catania, Sicily (IT).

Another type of planar defect resulting from the change of the planar stacking sequence is the mico-twin or simply twin. The distinctive feature of a twin is that the

planar arrangements on opposite sides of the stacking disruption are mirror images of each other. For example, the stacking sequence ABCABCACBACBA…possesses a reflection about the A-plane located at the center of the palindrome. In the diamond or zinc blende structure, twinning occurs mostly about the (111) plane. Twinning causes a change in the crystal orientation. For crystal growth along the <111> direction in the zinc blende structure, the orientation of the crystal planes in the twinned region is along the <$\underline{111}$> or <115> direction. A very smooth surface morphology can result in 3C-SiC heteroepitaxial growth along the <111> direction since the twinning plane is the same as the growth plane. Figure 2.5 (a) shows a schematic reprenstation of a micro-twin while Figure 2.7 shows a plan-view TEM micrograph of an actual microtwin present in a 3C-SiC film grown on (100)Si.

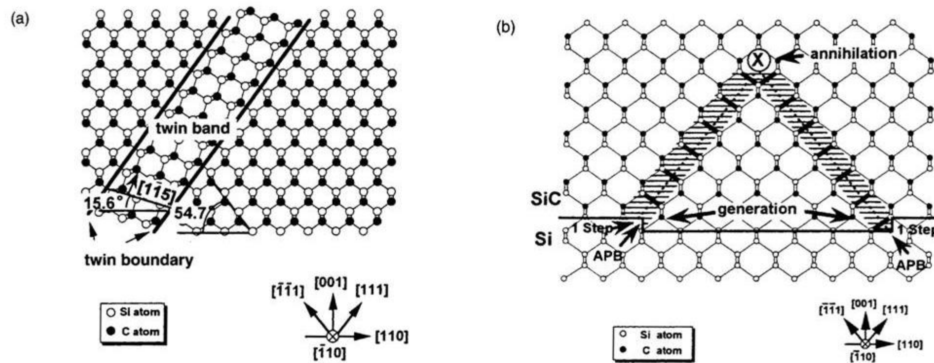


Figure 2.5 Schematic representation of faults in SiC on Si heteroepitaxy. (a) micro-twin defect and (b) antiphase domain boundary (APB) annihilation with film thickness. (Mendez, et al. 2005)

A planar defect that frequently occurs during the growth of (100)3C-SiC on (100)Si substrates is the antiphase boundary (APB). This type of defect is prevalent

during APCVD growth and is significantly reduced at lower growth pressures (Cho and Carter 2001). The APB occurs when two islands having different ordered phase coalesce. In the early stages of the film growth, partial surface steps may cause a relative position shift between the atomic stacking of different islands. In the case of SiC, due to surface roughness of the carbonized Si substrate, some islands of SiC may sit higher relative to others. As the islands grow and coalesce, a Si or C layer of one island may bond with another Si or C atom of another island forming a Si-Si or C-C bond as illustrated in Figure 2.6. These boundaries tend to propagate along the {111} planes (Ishida, Takahashi and Okumura 2003). However, the etching experiments of Li and Giling have shown evidence that APBs can propagate along the {110} plane (Ishida, Takahashi and Okumura 2003).

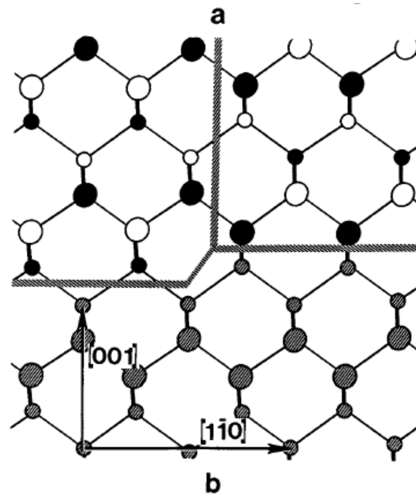


Figure 2.6 Geometrical consideration of the formation of an APB when SiC is grown on (100)Si substrate with an atomic step. Note the bonding of Si-Si and C-C atoms. (Cho and Carter 2001)

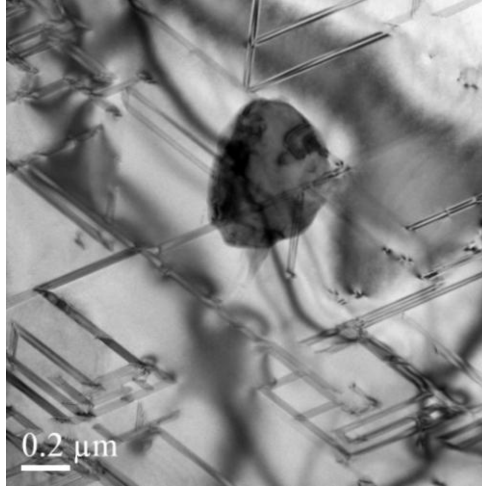


Figure 2.7 Micro-twinned crystal defect observed with plan-view TEM (PV-TEM). Data courtesy of C. Buongiorno, IMM-CNR, Catania, IT.

The double position boundary (DPB) is a special case of twinning in which separate domains are rotated about a 180° twin axis and is seen when a FCC type crystal structure is grown in the (111) orientation on a (111) surface (Kong, et al. 1987). This is commonly seen in 3C-SiC films grown on (111)Si. As illustrated in Figure 2.9(a), the (111)Si surface has two equivalent types of sites that the C atoms can locate. As a result, two different nuclei orientations can develop which are rotated 60° relative to each other. When these nuclei coalesce into each other, a DPB is formed. In Figure 2.9(b), the relative shift of the stacking sequence between neighboring domains is shown. The upper case "A" represents the surface of the substrate, while the lower case "a b c…" represents the stacking layers of the epitaxy. One can see that every third layer offers the opportunity to form a perfect bond across the interface, Si-C, for example, the other planes cannot form this type of bond (Kong, et al. 1987). As a result, the boundary is somewhat disordered and the internal energy is high (Kong, et al. 1987).

Figure 2.8 Example of hetero-defects in (100)3C-SiC from X-TEM. Note the defects along the (111) planes, also threading dislocations and stacking faults. Image courtesy C. Buongiorno, IMM-CNR, Catania, Sicily (IT)

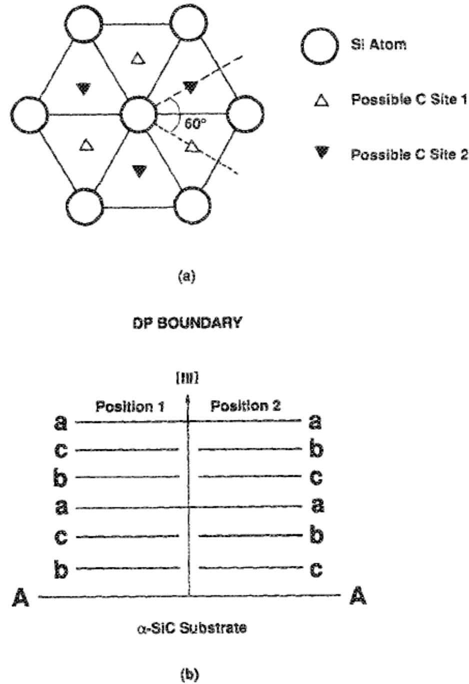


Figure 2.9 Stacking fault generation schematic showing the error in crystal layer formation resulting in a stacking fault defect. (a) top view representation and (b) side view showing the plane stacking sequence (Kong, et al. 1987).

2.2 Hot-Wall 3C-SiC Growth on (100)Si

The 3C-SiC heteroepitaxial process described in this section was developed in several stages from the endeavor of previous students in the USF SiC group. The initial process was developed from the research of Dr. R.L. Meyers-Ward during her thesis work (Myers 2003). This process was then adapted for the incorporation of halide chemistry to the CVD process during the respective dissertation and thesis work of M. Reyes (Reyes 2008) and S. Harvey (Harvey 2006). The 3C-SiC heteroepitaxial process was altered for use in a newly constructed hot-wall CVD reactor, MF2, from the thesis work of C.L. Frewin (Frewin 2007).

A low-pressure, horizontal, hot-wall CVD reactor was used to carry out the deposition experiments on n-type (100)Si substrates. The substrates were diced into 8 mm x 10 mm die which were RCA cleaned and immersed in a dilute 1:20 hydrofluoric acid (HF) solution to remove contaminants and the native oxide prior the hetero-epitaxial deposition. The traditional dual precursor chemistry of propane (C_3H_8) and silane (SiH_4) were used with a palladium cell purified hydrogen (H_2) carrier gas.

The growth schedule consisted of two main steps: (i) low pressure carbonization of the Si substrate and (ii) low pressure 3C-SiC epitaxial layer growth. The sample temperature was ramped in a H_2/C_3H_8 atmosphere, $x_{propane} = 16x10^{-3}$, the propane mole fraction, from room temperature to 1135˚C, at which it was held constant for two minutes to carbonize the Si surface. After carbonization, SiH_4 was introduced at a mole fraction, $x_{silane} = 1x10^{-3}$ and gradually increased to $x_{silane} = 7.5x10^{-3}$ while the temperature was ramped at a rate of ~35°C/ min to 1380˚C for growth. As the temperature was ramped, the process pressure was then lowered from 400 Torr to 100 Torr and the C_3H_8 was gradually decreased from $x_{propane} = 16x10^{-3}$ to $x_{propane} = 0.22x10^{-3}$. Once at the growth plateau of the process schedule, a Si/C ratio of 0.9 was maintained during growth. This procedure resulted in a repeatable 3C-SiC growth process, yielding growth rates up to 10 μm/h and specular surface morphology. This served as the "baseline" process for the development of the high temperature and low temperature 3C-SiC growth processes on (111)Si substrates.

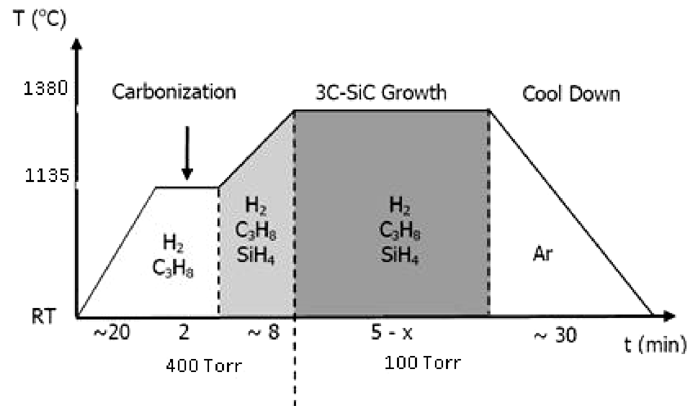


Figure 2.10 Process schedule for the growth of 3C-SiC on Si via heteroepitaxy.

Optical Microscopy with a maximum magnification of 500X was used to qualitatively analyze the film surface morphology and interface void density after growth. Fourier Transform Infrared (FTIR) Spectroscopy was used for film thickness determination. The surface morphology and structural quality were characterized by Atomic Force Microscopy (AFM) and X-ray Diffraction (XRD).

2.3 Hot-Wall 3C-SiC Baseline Growth Process on (111)Si

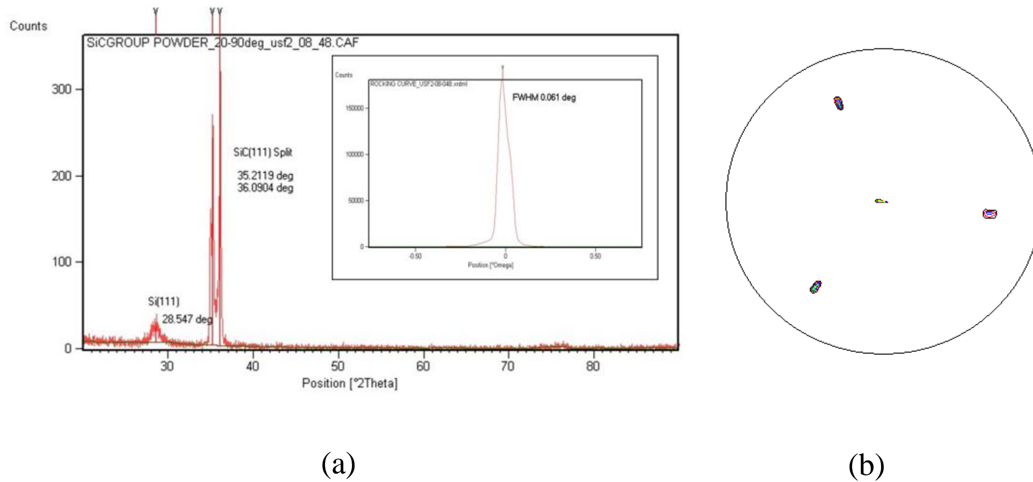
As previously discussed in Chapter 1, the as-grown 3C-SiC films on Si films suffer from a large amount of defects caused by the 20% lattice mismatch between Si and 3C-SiC which results in a rough mesa-like growth structure (Ishida, Takahashi and Okumura 2003). In particular the surface morphology of 3C-SiC grown on (001) oriented Si is highly irregular thus making device processing difficult. Fortunately, growth on (111) oriented Si results in a much smoother morphology with nearly flat surface topology achieved with our process. This provided the motivation to develop and optimize a 3C-SiC growth process on (111)Si based on the 3C-SiC/ (100) Si growth

schedule described previously for possible use in advanced electronic device and MEMS applications.

A single-side polished 50 mm (111)Si wafer was RCA cleaned and loaded into a hot-wall SiC CVD reactor for growth, details of which may be found in the literature (Kern and Poutinen 1970). The 3C-SiC process was performed in two stages, namely carbonization followed by growth. During carbonization, a C_3H_8 mole fraction of $1.6x10^{-3}$ was achieved by using a flow of propane (C_3H_8) and hydrogen (H_2) through the reactor at 16 standard cubic centimeters per minute (sccm) and 10 standard liters per minute (slm), respectively, was established while the temperature was ramped to 1135°C at a process pressure of 400 Torr. Once the temperature stabilized at 1135°C, the wafer was held under a steady-state condition of gas flow, temperature, and pressure for 2 minutes. This allowed the conversion of the Si wafer surface to a 3C-SiC buffer layer. After the 2 minute carbonization plateau was finished, the growth phase began. Silane (SiH_4) was then introduced into the gas stream at x_{silane}=$1.0x10^{-3}$ and was slowly increased in a step-wise fashion to x_{silane}=$5.5x10^{-3}$ while the C_3H_8 mole fraction was decreased from x_{silane}=$1.6x10^{-3}$ to $0.14x10^{-3}$. During this transition, the temperature was ramped from 1135°C to 1380°C over a 15 minute period and the process pressure reduced to 100 Torr and the H_2 flow increased from 10 slm to 40 slm at 1315°C. Once the growth temperature of 1380°C was reached, a Si/C ratio of 1.2 was maintained while the wafer was once again held under steady-state gas flow, temperature and pressure.

Figure 2.11(a) shows the X-ray diffraction rocking curve of the 3C-SiC(111) peak with a full-width at half maximum (FWHM) value of 219 arcsec. This is a very

interesting result given that the film thickness was only approximately 2 μm, thus indicating that the grown film is of very high quality compared with published literature values. Based on this result x-ray polar figure mapping was performed and it was observed that the micro twin content was below the detection limit of the technique, as shown in Figure 2.11(b). Pole figures were recorded on a D5005 Bruker diffractometer equipped with an Eulerian cradle using Cu-Kα radiation with the source operating at 40 kV and 30 mA. The pole figures were then recorded by rotating the samples along the ω-, χ- and φ-axes with details of this technique reported by Anzalone et al. (Anzalone, et al. 2008). The crystallographic orientation of the (111) 3C-SiC planes was recorded at $2\theta \approx 35.59°$ for the XRD pole figure analysis. Figure 2.10(b) shows the presence of four strong peaks, three at χ=70,5° and one at χ=0°, corresponding to the typical <111> 3C-SiC plane orientations. No other peaks were visible, and, in particular, spots associated with micro-twin defects were not observed.



(a) (b)

Figure 2.11 3C-SiC(111) film characterization data via X-ray diffraction showing (a) θ-2θ powder diffraction scan (inset ω-scan rocking curve) and (b) the corresponding polar figure map. The film diffraction was solely along the (111) direction with a rocking curve FWHM of 219″ (film thickness ~2 μm). The polar figure indicates an absence of micro-twins as confirmed by TEM (Fig. 2.11). Pole figure mapping courtesy of R. Anzalone, Università di Catania, Catania, Sicily (IT)

Based on the X-ray data, the next step in the analysis of the grown (111)3C-SiC film was naturally TEM analysis. Plan view TEM analysis is a very powerful technique for the detection and eventual quantification of defects in the SiC film such as stacking faults and micro-twins. In order to assess the stacking fault density, some bright-field on-axis images were acquired, and a count of the stacking fault density performed. The data indicates a concentration of stacking faults ~5.2×10^4 cm^{-1}. This value is obtained by measuring the length of stacking faults on a wide area of about 20 μm^2. Such a SF density is expected for the film thickness we studied. By going towards thicker films, the SF density will decrease up to a saturation plateau. Figure 2.12(a) shows one of the corresponding [100] on-axis plan view-TEM images where a low density of stacking faults is visible. Along the [100] direction the detection of micro-twins is not very easy,

either from the images or from the diffraction pattern, where the presence of extra spots is expected. For the detection of twin defects we have to tilt the sample by 18° in order to align the electron beam with the [114] crystal direction. The relative diffraction pattern is very sensitive to the presence of twins, because of the superimposition of the (110) diffraction pattern derived from the twinned crystals. In the Fig. 2.12(b) is shown the (114) diffraction pattern of a relatively large area of the film. The extra spots due to the twinned crystals are completely absent, and only the spots due to the stacking faults intensity elongation are present, as confirmation of the very low micro-twin concentration in this film.

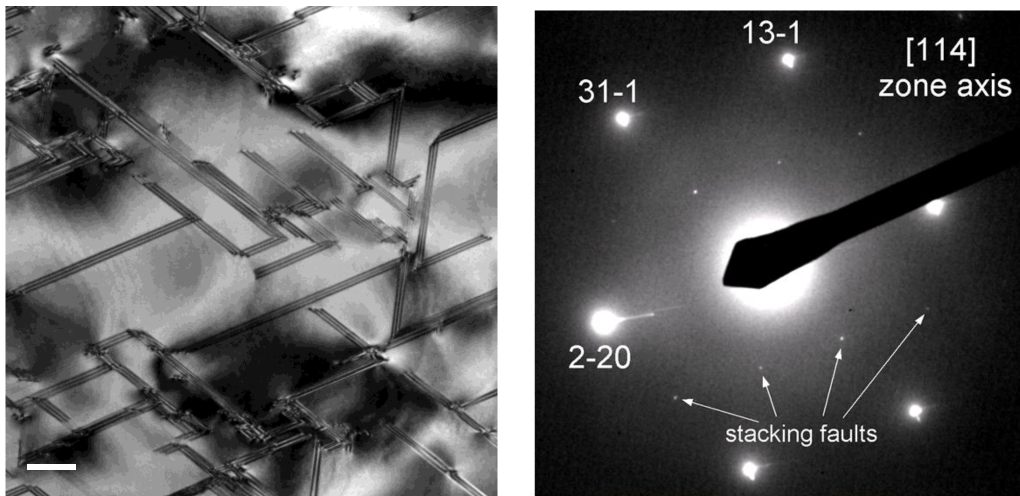
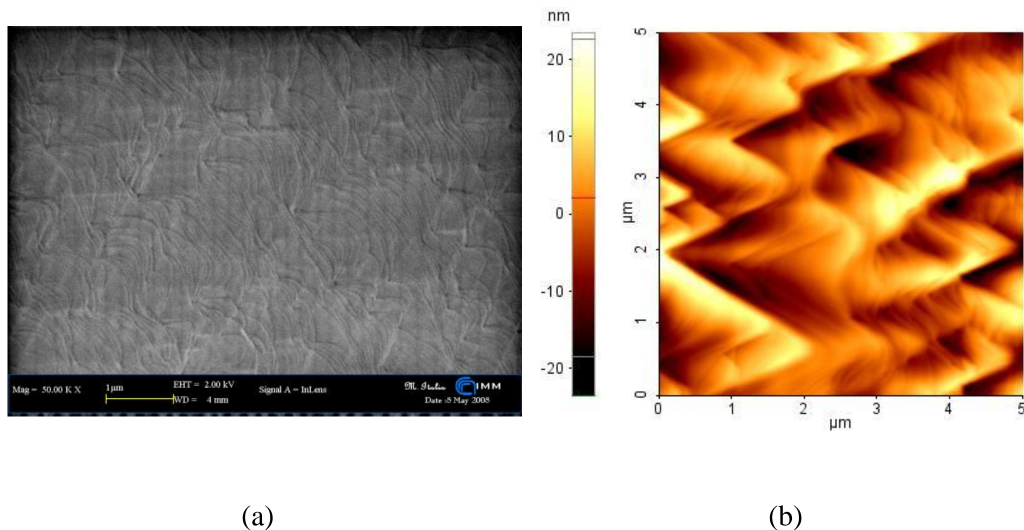


Figure 2.12 3C-SiC(111) film characterization by TEM via (a) (100) on-axis plan-view bright-field micrograph and (b) [114] zone axis diffraction pattern. The presence of micro-twins was not detected, even in the [114] zone axis confirming the x-ray polar figure observations of Fig. 2.10. Data courtesy of C. Buongiorno, IMM-CNR, Catania, IT

What was curious in the TEM micrographs were linear features (not shown) which appeared to be atomic steps. Therefore SEM and AFM analysis was performed on these samples which confirmed that these are indeed originating from steps on the

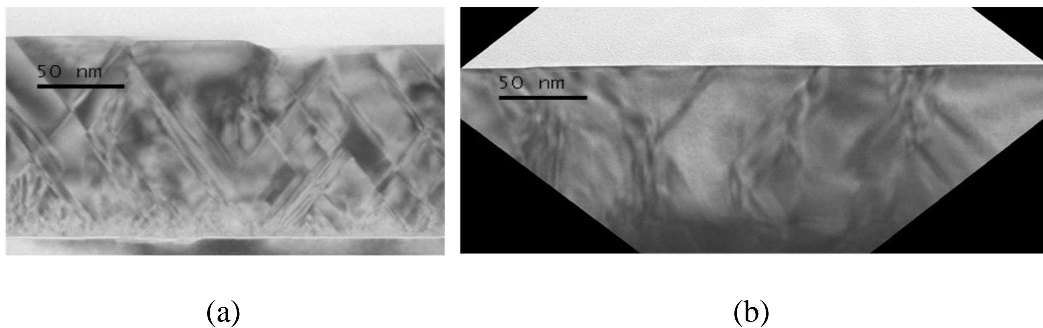
surface. Morphological analysis via plan-view SEM and AFM are shown in Figure 2.13. In both cases triangular step morphology was observed, consisting of single unit cell and multiple (macro) steps indicative of step bunching. While the (111)Si substrate is nominally on-axis (i.e., miscut 0° from the <111>) there is generally a slight misorientation in the starting substrates. The nature of the step morphology indicates that the misorientation is along the <11-2> based on the work of Camarda et al. (Camardo, Magna and LaVia 2009). Based on the work of Coletti (Coletti, et al. 2007), these steps can be rearranged to improve the atomic order of the surface. Indeed this has also been performed on this surface in our CVD reactor and is reported by Frewin et al. (Frewin, Coletti, et al. 2009).



(a) (b)

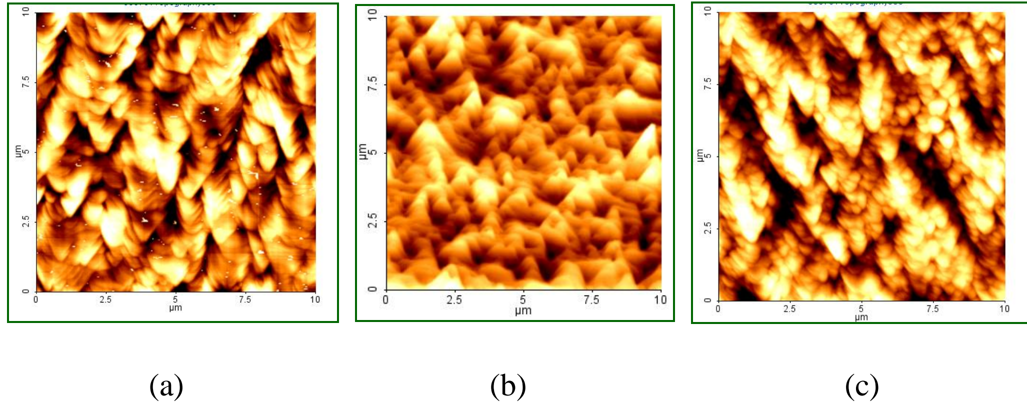
Figure 2.13 3C-SiC(111) film characterization by (a) plan-view SEM and (b) AFM analysis. Note the triangular shaped steps which consist of single atomic steps as well as macro steps due to step bunching. Substrate orientation ~0° but observed step structure indicates a slight misorientation in the <110> direction. SEM image courtesy of M. Italia, IMM-CNR, Catania, IT.

Additional analysis was performed on similarly grown films to assess their mechanical properties for MEMS applications. In fact these films were compared to (100)3C-SiC on Si films grown with a similar process (Reyes, Shishkin, et al. 2007) and the mechanical properties were found to be exceptional, as reported by Reddy et al. (Reddy, et al. 2007) and also Locke et al. (Locke, et al. 2008). The measured hardness was around > 50 GPa with an Elastic Modulus of >500 GPa compared with values for Si of 12 and 175, respectively, which is even higher than values measured for (100)3C-SiC.



(a) (b)

Figure 2.14 Cross-section TEM data of 3C-SiC grown on (a) (100)Si and (b) (111)Si. Note the more flat surface morphology and lower defect density of the 3C-SiC(111) film. Data courtesy of C. Buongiorno and A. Severino, IMM-CNR, Catania, IT



(a) (b) (c)

Figure 2.15 10µm x 10µm AFM scans of (111)3C-SiC/ (111)Si deposited at 1380°C illustrating the impact of pressure on film quality. (a) 100 Torr, (b) 200 Torr, (c) 400 Torr. Note the increasing grain size as the growth pressure decreases. All films ~1.2µm thick and grown under same temperature and precursor concentration.

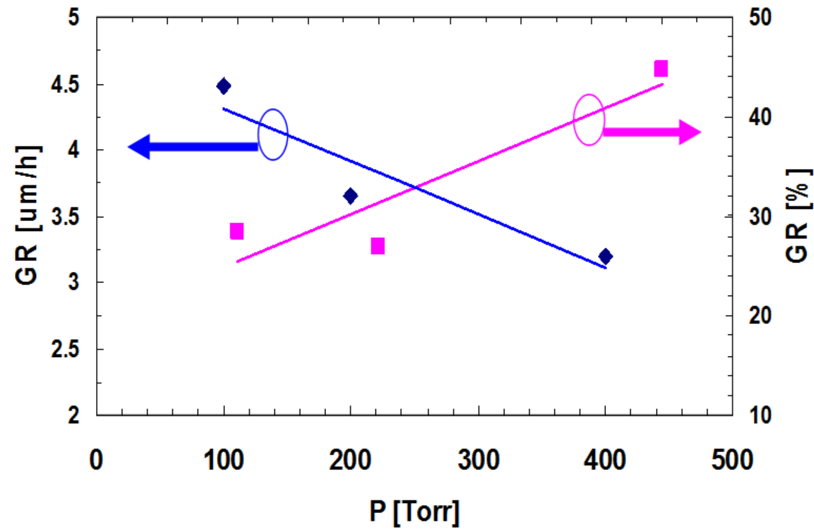


Figure 2.16 The impact of reactor pressure on the growth rate (GR [µm/h]) and (111)3C-SiC film thickness gradient (GR[%]). 50mm (111)Si wafer substrate. Reduced pressure improves thickness uniformity and increases deposition rate as expected (See Section 2.1). The trend lines are to aid the eye only and do not infer linear relationships.

2.4 CVD Reactor Hardware

The CVD reactor used for this research was the horizontal hot-wall reactor shown in Figure 2.16, which was designed and built by the SiC Group at the University of South Florida. The reactor chamber wall is a fused quartz tube supported by water-cooled electropolished stainless steel endplates. The gases are regulated via mass-flow controllers (MFC) and flow into the head plate (left side of Figure 2.16) by ¼″ 316L stainless steel gas lines. A round diffuser plate consisting of several small, evenly-spaced holes disperse the gases and establish laminar flow. The gases are funneled from the diffuser plate by a quartz inlet tube to the hot zone of the reactor. The hot zone consists of a SiC-coated graphite susceptor surrounded by graphite foam. The susceptor provides a means of converting electromagnetic energy from the RF induction coils to thermal energy so the necessary CVD reaction can occur at the substrate surface. The ceiling of the susceptor was designed with a gradual taper so that the height of the upstream portion is higher than the downstream portion of the susceptor. The taper causes an increase of the gas velocity as it moves through the susceptor and, as a result, decreases the thickness of the boundary layer. This improves the film uniformity across the wafer. The graphite foam provides a physical means of supporting the susceptor and insulating the susceptor which reduces thermal gradients due to radiative and conductive losses in the susceptor. The water-cooled copper coil surrounding the reactor in Figure 2.16 heats the reactor hot-zone by radio frequency (RF) induction. A 50 kW/ 10 kHz solid state RF generator, manufactured by Mesta Electronics Inc., is capable of inductively heating the susceptor to temperatures near 2000°C. The temperature of the hot zone is monitored by an optical

pyrometer, which measures temperature by monitoring the susceptor's black body emission. The pyrometer is aimed at a small hole in the susceptor which has been bored to a depth near the growth zone, so that an accurate temperature measurement at the growth zone can be obtained. The temperature and gas flow is regulated by feeding the data back to the RF generator and MFCs, respectively, by a computer interface written in LabView™. The CVD reactor is currently configured to flow propane (C_3H_8) and silane (SiH_4) which serve as the SiC precursor gases, nitrogen (N_2) for n-type doping, and argon (Ar) or hydrogen (H_2) as the carrier or annealing gas. The reactor also has the capability to use hydrogen chloride (HCl) or methyl chloride (CH_3Cl) to add chlorine to the reactor chemistry. The H_2 gas is purified via a palladium cell and the Ar is purified by a catalytic purifier. An Edwards DP-40 dry pump and throttle valve regulates the CVD chamber pressure.

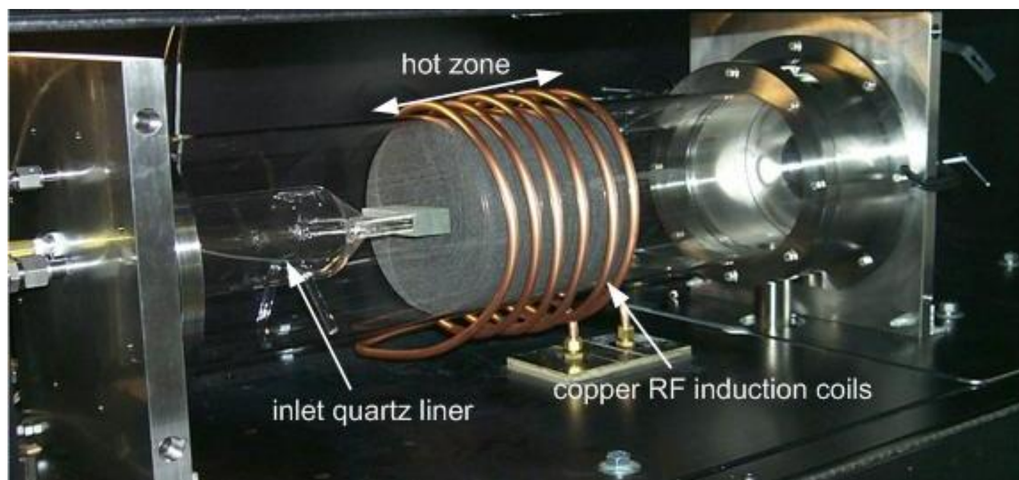


Figure 2.17 Photograph of the MF2 CVD horizontal reactor at USF. MF2 was used for the growth of all films reported in this thesis and is dedicated solely for 3C-SiC on Si growth and processing.

2.5 Summary

Chemical vapor deposition is a widely-used technique to produce uniform high quality epitaxial films. Several variations of chemical vapor deposition exist, but are essentially governed by the mechanisms of mass transfer and surface reaction kinetics. The reactants are mixed in a carrier gas, frequently H_2 or Ar, and delivered to the reaction chamber of the CVD reactor. The reactants then diffuse across a boundary layer, adsorb onto the surface and undergo chemical reactions. Many parameters must be considered in order to successfully grow an epitaxial layer. Temperature and pressure are the most influential variables. Pressure regulates the boundary layer thickness, the lower the pressure the thinner the boundary layer and the reactants and reaction products can diffuse rapidly. Temperature regulates the surface kinetics, at higher temperatures the surface reactions can occur faster and increase the deposition rate.

The early stages of thin film growth can be generalized for all deposition process in the following sequence. First, the condensation and nucleation of species from the gas phase must occur. Second, diffusion-controlled island coalesce into a connected network structure. Last, steady state growth of the film occurs. CVD processes deviate from this generalization because reactions must occur at the surface of the substrate. Heteroepitaxy, by its very nature, is prone to crystal defects. In 3C-SiC growth, defects such as edge dislocations, stacking faults, twins, misfits, and sometimes APBs are a result of film stress from the mismatch of the lattice parameter and coefficient of thermal expansion. Double position boundaries are a result of two possible locations on a (111) oriented face for the stacking of atoms to occur. These defects must be minimized

through reactor design considerations, gas chemistry, and careful process parameter modification.

CHAPTER 3: LOW TEMPERATURE PROCESS DEVELOPMENT

The growth of 3C-SiC on Si substrates has been traditionally been performed at temperatures just below the melting temperature of Si (i.e., 1410 °C). The reason for this is twofold. First the highest-quality epitaxial layers have been formed at these temperatures and second the growth rate is a strong function of growth temperature. Indeed growth performed on bulk 3C-SiC substrates provided by the Hoya company in our laboratory were optimum at a temperature of 1550 °C (Saddow, Shishkin and Myers 2008). However, one of the main applications of 3C-SiC on Si films is the formation of highly robust MEMS structures, and for this technology to be truly practical there is a need for an oxide release layer. Therefore, the formation of 3C-SiC on an oxide release layer would be highly beneficial, but this is only possible at reduced growth temperatures. This chapter outlines research performed during this thesis work to develop a low-temperature growth process that maintains film quality with an acceptable growth rate of ~2 µm/h.

3.1 Motivation for Reducing Process Temperature

From an economic viewpoint, the faster growth rate of the high temperature 3C-SiC heteroepitaxial process would make its incorporation into SiC device fabrication desirable. However, the extreme temperatures severely limit the selection of materials to

be incorporated into a fabrication process prior to the 3C-SiC deposition mainly to refractory-type materials. Otherwise, device structural integrity may be lost or undesirable diffusion into the surrounding area may lead to device failure. For example, metals such as Au and Al, frequently used in device fabrication, have melting points far below 1380°C and silicon dioxide, having a glass transition temperature near 1200°C, exhibits plastic flow at the temperatures used for high temperature 3C-SiC growth as described in Chapter 2. Another issue arises from the 8% coefficient of thermal expansion (CTE) mismatch between 3C-SiC and Si. When the 3C-SiC hetero-epitaxial film cools from the high growth temperature to ambient room temperature, thermal stress develops at the 3C-SiC/ Si interface putting the 3C-SiC film under tension and inciting stress-relieving mechanisms, such as wafer bow, to emerge. The greater the ΔT between the growth temperature and the cooled 3C-SiC/ Si wafer, the greater the bow. Excessive wafer bow can complicate subsequent processing of the wafer, induce the deformation of free-standing structures, or cause catastrophic substrate fracture or film delamination. Another stress-relieving mechanism is the formation of a planar crystal defects such as glide twins and stacking faults.

When these temperature-related issues are considered, the development of a low-temperature 3C-SiC hetero-epitaxial process appears to be a necessity if 3C-SiC film growth is to be incorporated with other fabrication processes, especially for MEMS applications.

3.1.1 Film Buckling from CTE Mismatch

As previously discussed, the residual stress found in heteroepitaxy, specifically 3C-SiC growth on Si, comes from two primary sources, the lattice parameter mismatch and the different thermal expansion coefficients. Figure 3.1 illustrates the temperature dependence of the thermal expansion coefficients between 3C-SiC and Si. Since ~1380°C is the typical growth temperature used for 3C-SiC growth, the chart clearly shows that CTE will contribute significantly to the residual stress present in the film after growth.

Vacancies and interstitial atoms at the grain boundaries can provide a stress relieving mechanism as the crystalline layers grow. From Figure 3.2, it can be seen that the stress as a function of thickness decreases as the film thickness increases due to defects in the lattice. As the growth continues, eventually the effects of lattice mismatch are minimized via defect formation so that the stress in the film decreases with film thickness. The point at which this defect generation/stress relief occurs is known as the critical thickness, t_c, and is important for determining the maximum thickness that may be grown before significant crystallographic defects are formed.

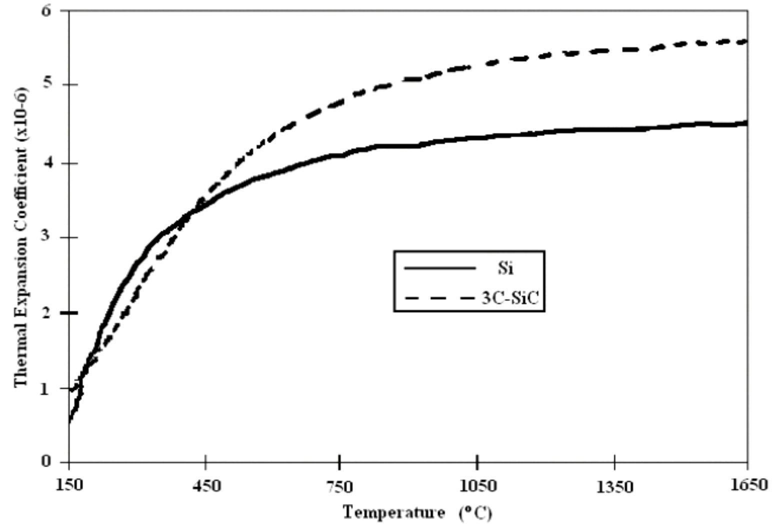


Figure 3.1 Graph of the thermal coefficient of thermal expansion (CTE) between 3C-SiC and Si. The mismatch is 8% at room temperature (Weeber and Wang 1996).

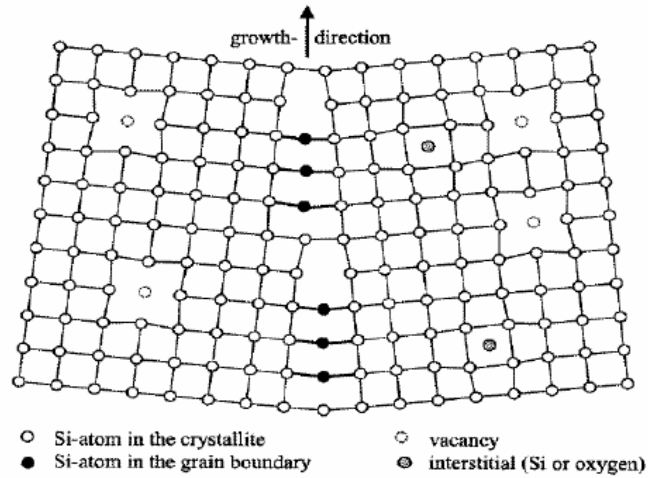


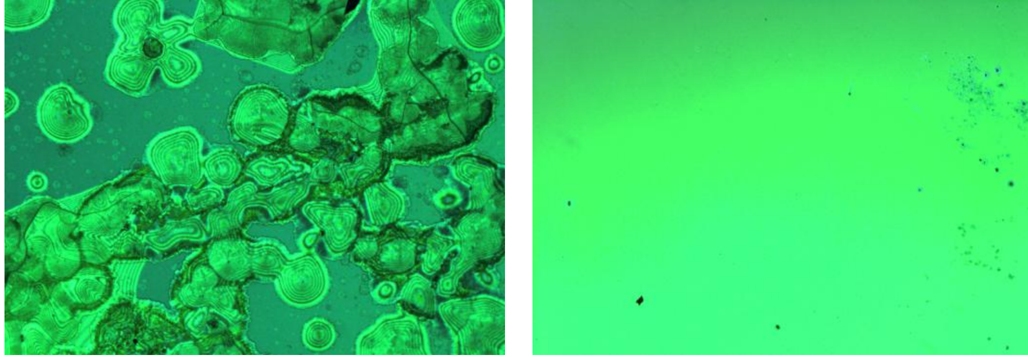
Figure 3.2 Defect generation in crystals caused by interstitial atoms and vacancies in the lattice.

3.1.2 Growth on Oxide-Coated SiliconWafers

Oxide-coated Si wafers provide a promising substrate for the growth of SiC owing to its potential advantage in film strain relaxation and the facilitation of SiC micromachining. The high temperatures required for the growth of single-crystal 3C-SiC described in Chapter 2 soften the SiO_2 layer, allowing relief of the stress caused by the 20% lattice mismatch, and suppress the formation of voids caused by Si evaporation at the 3C-SiC/Si interface (Huang, et al. 2005). The softening of the SiO_2 occurs at approximately 1160°C (Nassau, Levy and Chadwick 1985) and is referred to as the glass transition temperature. When a substrate deforms in response to film stress and allows for a defect-free film to be formed by absorbing all of the stress at the interface, it is called a compliant substrate. By deforming, the substrate allows the strain, which is the physical response to stress, to reside in the substrate instead of the film. Although thick SOI seed layers (>50 nm) have been shown to produce 3C-SiC films that are as defective when compared to 3C-SiC films grown on single-crystal Si substrates, the benefits of the epitaxial growth of 3C-SiC on SOI are realized when 3C-SiC is deposited on a thin (<50 nm) seed layer of Si, which produces excellent quality 3C-SiC. However, a major drawback of using SOI in the production of 3C-SiC devices is the fact that SOI requires expensive ion implantation and chemical-mechanical planarization (CMP) processing. These processes add to the overall production cost of the device, and many MEMS devices do not require single-crystal SiC material for proper functionality. A cost-efficient, easily produced wafer stack consisting of polysilicon (p-Si) deposited on a SiO_2/ Si substrate could replace the SOI substrate if poly-SiC is desired as a material for

the MEMS application. As mentioned in Chapter 2, deposition techniques depend on condensation from the gas phase followed by the nucleation of conglomerates. This tends to form an inhomogeneous network structure in the early stages of film growth, which means that complete coverage of the substrate has not occurred. These uncovered areas are referred to as “pinholes” in thin film terminology. When SiO_2 is heated beyond the glass transition temperature, its viscosity is reduced and it can flow through these pinholes. Figure 3.3 illustrates the results of the underlying SiO_2 flowing through the pinholes at the typical temperatures (1380°C) used for 3C-SiC growth on Si.

SiO_2 has been traditionally used as an etch-stop for Si processing involving DRIE/RIE (S. Federico 2003). However, the recipes used to etch Si in DRIE/RIE have a similar etch rate with SiC, thereby excluding selectivity and reducing accuracy for the desired structure (Beheim and Evans 2006). With this in mind, SOI substrates provide an excellent media for the creation of freestanding 3C-SiC devices by providing not only an oxide for the etch-stop for DRIE/RIE, but also a single Si crystal seed layer for the heteroepitaxial growth of the 3C-SiC.



(a) (b)

Figure 3.3 Optical micrograph of 3C-SiC growth on a poly-Si seed layer deposited on an oxide-coated (111)Si wafer. (a) The high growth temperature of ~ 1380°C resulted in glass flow of the oxide through pinholes in the poly-Si film. (b) The high growth temperature of ~ 1200°C and did not result in glass flow of the oxide through pinholes in the poly-Si film. This result demonstrates the need to reduce the growth temperature to enable 3C-SiC growth on such a wafer.

3.2 Low Temperature Process Development

Since prior 3C-SiC growth on (111)Si had been conducted using a high temperature growth regime (~1380°C), no low-temperature process had been systematically developed. An established low temperature growth process would exploit the morphologically flat films possible on (111) oriented substrates, but with reduced wafer bow and fracturing associated with (111) oriented heteroepitaxial growth. A low temperature growth process would also be compatible for the growth of 3C-SiC on oxide-coated Si compliant substrates.

3.2.1 Low Temperature Baseline Process

The subsequent 3C-SiC growth was performed as follows. A (111)Si wafer was placed in a horizontal, hot-wall reactor heated by the RF induction of a SiC-coated

graphite susceptor. The wafer was loaded into a molded poly-SiC plate to fix the position of the wafer within the reactor hot zone. This polyplate was then seated into a recess in the susceptor and the chamber was sealed and evacuated of residual gases. The chamber was then filled with palladium-purified hydrogen to a pressure of 400 Torr. The 3C-SiC process developed for this reactor involves two main process stages, namely the carbonization and growth stages (Reyes, Shishkin, et al. 2007). The pressure for the carbonization process was 400 Torr, and growth pressure was 100 Torr based on the high temperature process. The standard gases used for 3C-SiC growth are: palladium-purified hydrogen, H_2, which is used as the transport gas; propane (C_3H_8), which is the carbon precursor; and a 10% silane (SiH_4) premixed in 90% hydrogen ballast(H_2), which is the silicon precursor.

The carbonization stage occurred while the sample temperature was ramped to 1135°C at a rate of ~35 °C/min. Throughout the ramp a flow of 16 sccm of C_3H_8 was maintained with a mass flow controller (MFC), and the H_2 carrier gas flow was maintained at 10 slm. Once the carbonization temperature was reached, the temperature was maintained for 2 min to allow conversion of the (111)Si surface into 3C-SiC. After carbonization and creation of the 3C-SiC template layer, the temperature was ramped a second time at a rate of 35°C/min to the growth temperature of 1200°C. During this ramp, we determined that it is advantageous to decrease the flow of C_3H_8 while simultaneously introducing and increasing the flow of 10%SiH_4/ 90%H_2 in a step-wise manner. At the growth temperature the input gas silicon to carbon ratio, Si/C, for the growth stage was 1.2. H_2 flow was maintained at 10 slm until 30°C before the ramp was

completed, where it was increased to 40 slm, and the pressure was reduced from 400 Torr to 100 Torr. The temperature and gas flows were then held constant, allowing the continued epitaxial growth of 3C-SiC on the carbonized (111)Si. Figure 3.4 graphically summarizes the baseline low temperature process.

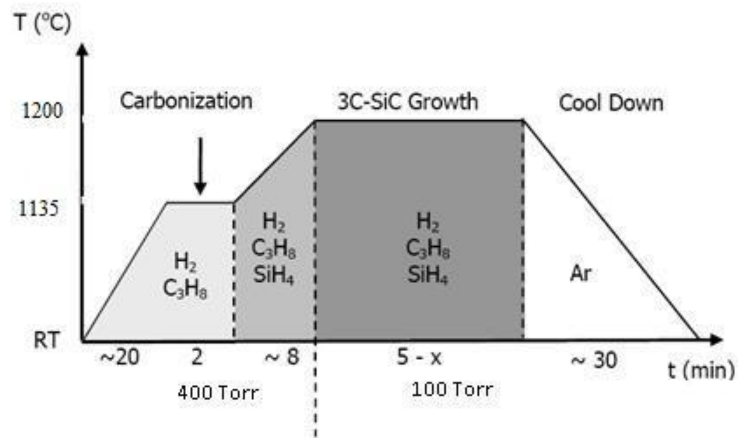


Figure 3.4 Initial baseline low temperature CVD growth process schedule.

The initial test dies yielded a hazy surface over the standard test polyplate, a sintered silicon carbide plate which holds the 8 x 10mm silicon dies in a consistent location in the reactor hot zone.

A series of experiments were conducted in order to obtain a uniform specular film deposition within the growth zone. As briefly discussed in Chapter 2, several parameters govern the film deposition when using chemical vapor deposition. In order to develop an optimized process only one growth parameter was changed at a time while all others are held constant. Sometimes this can be difficult to achieve if a multitude of experiments are conducted, since the process of film deposition itself alters the reactor condition. The

first series of experiments involved decreasing the molar concentration of SiH_4 since it was reasoned that C_3H_8 would not crack as effectively at the lower growth temperature, thus resulting in a Si saturated gas composition. The time of film growth was set at 20 minutes for all tests since thin polycrystalline films are difficult to discern from thin monocrystalline films in the early stages of growth. In a series of four experiments, the Si/C ratio was varied in increments of 0.2 from 1.4 to 0.8, the C_3H_8 molar concentration was held constant while the 10% SiH_4/ 90% H_2 flux was varied. The best result was obtained for a Si/C ratio of 1.2, although the film was visually hazy in appearance, it demonstrated the least haziness and had the largest grain sizes of the four samples when viewed at 500X magnification using an optical microscope. The next series of experiments involved decreasing the precursor concentration in the H_2 carrier gas. The initial precursor molar fraction values for dilution of 5.5 sccm of C_3H_8 and 200 sccm of 10% SiH_4/ 90% H_2 in 40slm H_2 were $x_{silane}= 0.5x10^{-3}$ and $x_{propane}= 0.139x10^{-3}$. The total precursor concentration was reduced so that the flow rate for propane was 3 sccm. This resulted in molar fractions of $x_{silane}= 0.027x10^{-3}$ and $x_{propane}= 0.075x10^{-3}$. The resulting film morphology was clear and colorful, which indicated very thin film growth. The same experiment was run for 40 minutes to realize a thicker film for a more reliable quality assessment. The resulting 40 minute film growth was hazy and displayed a very granular morphology when viewed using 200X magnification optical microscopy. The SiC deposits on the polyplate revealed an important detail about the deposition pattern occurring in the hot zone of the reactor; it appeared that the optimum deposition was occurring downstream from the position of the test dies. The The H_2 carrier gas flow was

then reduced in 5slm increments from 40 slm to 20 slm while maintaining a constant precursor mole fraction. The best deposition occurred at a 25 slm H_2flow rate. A growth run was performed to assess the deposition rate. A 1 hour growth duration produced a 1.4μm thick 3C-SiC film. A series of experiments were planned to increase the deposition rate and improve film quality via modification of the Si/C ratio and precursor concentration.

3.2.2 Optimized Low Temperature Process

Once the low temperature baseline process had produced heteroepitaxial films with a clear, specular morphology, the optimum Si/C ratio needed to be determined for the new growth process. Although it was determined that the best morphology occurred at a Si/C=1.2 during the establishment of the low temperature baseline process, the position of the growth zone was moved upstream via carrier gas flow adjustment (reduced flow in this case). As the reactants travel through the hot zone, the Si/C ratio of the gas is constantly shifting in favor of a carbon rich atmosphere. This is believed to be the result of the Si supplied by SiH_4 being unavailable for surface reactions due to the formation of Si clusters in the gas stream (Vorob'ev, et al. 2000). Again, a series of film growths were conducted by varying only the Si/C ratio in 0.1 increments ranging from 1.2 to 0.9 while all other growth parameters were held constant. The samples were visually inspected under an optical microscope and it was determined that a Si/C=1.1 displayed the smoothest surface morphology with the fewest inclusions. Although visual inspection of the film provides only a qualitative assessment of film quality, surface

morphology is frequently related to crystal defects and this approach is a valuable tool when simplicity and immediate feedback is required.

An increase in the deposition rate was the focus on the next set of experiments. The current growth schedule involved diluting 3 sccm of C_3H_8 and 99 sccm of 10%SiH_4/ 90% H_2 in 25 slm of H_2 carrier gas while under 100Torr of pressure at 1200°C. The precursor concentration was increased to $x_{propane}= 0.16x10^{-3}$ and x_{silane}= C_3H_8= 4 sccm and 10%SiH_4/ 90%H_2=120 sccm diluted in 25 slm of H_2, maintaining the Si/C ratio at 1.1. The flow rate of C_3H_8 and 10% SiH_4/ 90% H_2 was increased to 4.0 sccm and 120 sccm, respectively. The resulting film was hazy and exhibited a granular morphology under optical microscope inspection. A growth run using a flow rate of C_3H_8=3.5 sccm and SiH_4= 115 sccm also demonstrated degraded film quality. The process pressure was further reduced from 100 to 75 Torr, the lowest obtainable pressure for the low temperature growth condition in the MF2 reactor. The pressure was decreased in an attempt to increase the amount of available reacting Si species by decreasing the tendency to form Si clusters. Computer modeling and experiments suggest that the deposition rate is sensitive to the available Si bonding sites (Vorob'ev, et al. 2000). LeChatelier's Principle states that a dynamic equilibrium opposes changes to a system. Although this does not explain why the change happens, it serves as a tool to assess the reaction of a system subjected to various process changes. Given the following reactions,

$$A+B \rightarrow C$$

$$A+B \leftarrow C$$

LeChatelier's Principle states that a decrease in the pressure of a system favors the reaction direction that increases the number of particles in the system. By decreasing the pressure, Si clusters should tend to dissociate, maintaining all other variables unchanged from the 100 Torr growth schedule. The resulting film grown at 3 sccm of C_3H_8, 99 sccm of 10% SiH_4/ 90% H_2 diluted in 25 slm H_2carrier gas under 75 Torr yielded improved film morphology. Attempts to increase the precursor molar concentration resulted in degraded film morphology.

A growth run on an RCA cleaned, quartered 50mm (111) Si wafer was performed to assess the film deposition rate. A forty-five minute 3C-SiC deposition experiment was conducted and measurements via FTIR yielded a growth rate that increased from 1.4µm/h to 1.9µm/h. The process conditions results in a clear, specular film. The film morphology was assessed using optical microscopy and atomic force microscopy. However, the bowed substrate revealed the presence of residual film stress. No fractures could be seen visually with the unaided eye, but under 200X, small cracks could be seen. A subsequent growth experiment was performed on an RCA cleaned, 50 mm (111)Si wafer using the optimized low temperature/ low pressure growth process. The duration of the growth plateau was 90 minutes and yielded a 2.84µm thick film. The wafer was noticeably bowed and fractures could be seen with the unaided eye across the wafer surface. The cracks formed a triangular pattern along the <110> directions on the wafer.

The low-temperature (111)3C-SiC process was then applied at increased growth temperatures up to 1380°C. The plot of the natural logarithm of the growth rate versus the inverse of the deposition temperature is illustrated in Figure 3.5. Comparing this

result to Figure 2.15 in Section 2.4., it suggests that the CVD reaction was in the mass transfer limited regime for the low temperature growth process, since the deposition rate was influenced by a pressure change from 100 Torr to 75 Torr.

Atomic force microscopy (AFM) scans were performed to ascertain the surface morphology of the 3C-SiC films. X-ray diffractometery (XRD) was performed on the 3C-SiC film to verify the film orientation and crystalline quality.

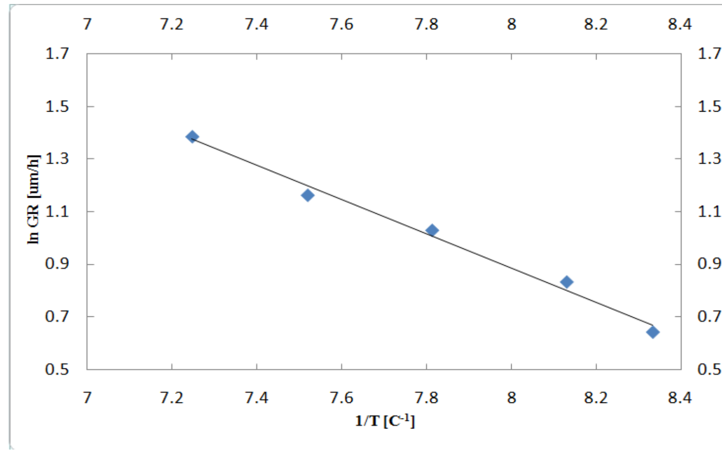
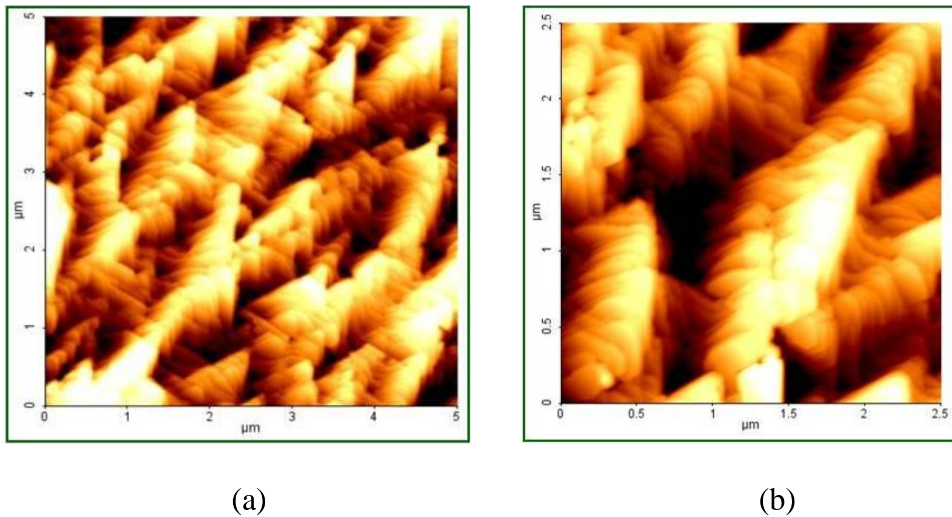


Figure 3.5 Plot of the deposition rate versus inverse temperature using the optimized low-temperature/ low pressure growth process at various growth temperatures.

3.2.2.1 AFM Analysis

A PSI-100XE AFM manufactured by Parker Scientific Instruments Inc. was used to quantify the film morphology. The AFM is a scanning probe instrument that uses a reflective cantilever/probe tip and laser feedback system to image surface topology. As the tip passes across the surface, the cantilever is deflected and the change of the laser-signal is recorded by a position sensitive detector (PSD). The position deviations are

processed via computer software and a topographical representation of the surface is created. This particular imaging mode is called contact mode. Another AFM measurement technique called non-contact mode uses a vibrating cantilever that is placed in close proximity to the sample in order to image the surface. As the tip experiences variations in the Van der Waals force, the resonant frequency of the tip changes. This technique was used to image the (111)3C-SiC surface shown in Figure 3.6. The characteristic 60° triangular-shaped grains of a (111)-oriented surface are readily apparent. This triangular feature is a result of the (111) oriented Si substrate not having a perfectly oriented surface, but is slightly miscut in the <110> direction. The directions parallel to the triangle edges point in the <110> direction as predicted by Camarda et al. (Camardo, Magna and LaVia 2009). The surface is very well-ordered although slightly step-bunched. The surface roughness value, Rq, for this film was 5.06 nm RMS.

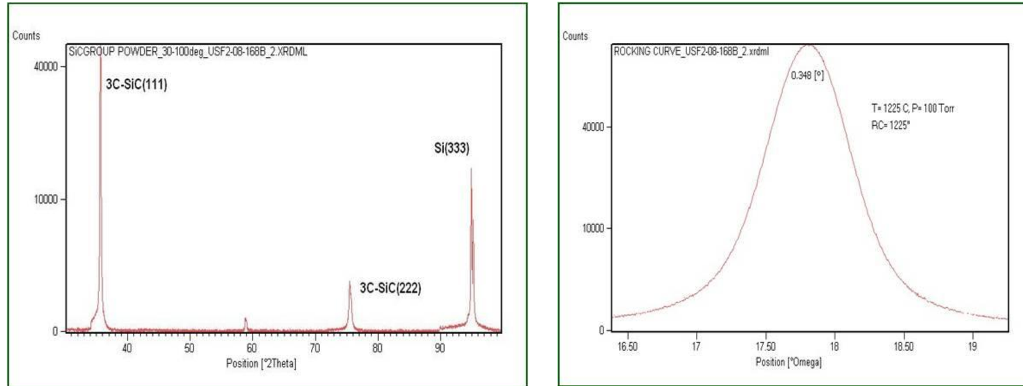


(a) (b)

Figure 3.6 AFM scans of growth run USF2-08-168B grown at a temperature and pressure of 1200°C, 75 Torr. The Rq= 5.06nm for the 10µm x 10µm scan.

3.2.2.2 XRD Analysis

A Philips X'Pert Panalytical XRD operating at the Cu Kα x-ray line was used to analyze the crystallinity of the 3C-SiC film deposited on the 50 mm (111)Si wafer. In XRD, reflected x-rays are used to determine the lattice spacing of the crystallographic planes by means of Bragg's Law. A θ-2θ, frequently referred to as a Powder scan, sweeps the detector and x-ray source through a range of angles so that the normal of the film surface bisects the incident and reflected path. The θ-2θ scan yields information about crystal orientation. The ω rocking curve scan maintains a constant θ value and "rocks" the sample in the ω direction. By performing the rocking curve scan, a relative assessment of the crystal quality from the full-width at half maximum value (FWHM) of the measured curve can be obtained. Figure 3.7(a) is a powder scan measurement from the 90 minute growth experiment. The strongest peak occurs at 35.7° which belongs to the (111)3C-SiC reflection. Another peak from 3C-SiC appearing at 75.5°corresponds to the (222) plane. Additional peaks at 69° and 95° are from the {111}Si planes due to the x-rays penetrating into the (111)Si substrate. No other 3C-SiC peaks appear in the diffractogram, confirming the deposited film is epitaxial and oriented in the [111] direction and is monocrystalline. The rocking curve measurement shown in Figure 3.7(b) was taken from the (111)3C-SiC peak at 35.7° and had a FWHM= 0.35°, which indicates a mildly defective monocrystalline film.



(a) (b)

Figure 3.7 XRD scans of USF2-08-168B. (a) θ-2θ scan reveals the that a monocrystalline (111)3C-SiC film is present (b) Rocking curve measurement of the (111)3C-SiC peak at 35.7° reveals a FWHM value of 0.348°, indicating the presence of crystal defects. Film thickness was~2.8μm

3.3 Summary

A stable low temperature 3C-SiC heteroepitaxial process with a 2μm/h deposition rate has been developed. First a baseline process was developed based on high temperature growth schedule for the growth of 3C-SiC on (111)Si substrates. The baseline process yielded specular films with a 1.4μm/h growth rate. Experiments modifying the Si/C ratio, precursor concentration and pressure were performed to optimize the baseline process. With the optimized process, the deposition rate was increased to 2μm/h and a monocrystalline film exhibiting a highly-ordered surface was produced.

CHAPTER 4: GROWTH OF 3C-SIC ON POLY-SI SEED LAYERS

Micro-electrical-mechanical systems (MEMS) are used for numerous applications from automobile airbag sensors to combustion control, sensors and medical diagnostics such as DNA assays, just to name a few. These MEMS applications have been supported by Si MEMS, which can be readily made using micromachining techniques developed for the microelectronics industry. One of the powerful fabrication approaches for Si MEMS is the use of poly-Si, the MEMS structural material, deposited on oxide release layers. These release layers are activated simply by placing the sample in HF which dissolves the oxide and thus leaves a free-standing poly-Si structure supported over the substrate surface.

One of the drawbacks of Si MEMS is the fact that Si, while a very durable and easy to machine, is not suitable for harsh environments due to the lack of material resilience at elevated temperatures and when exposed to harsh chemicals and radiation. SiC is a natural material for such harsh-environment sensors, and since SiC can be micromachined using similar processes to Si, much work has been done to develop SiC-based MEMS. While the cubic form of SiC can be deposited directly on Si, and the 3C-SiC layer patterned using reactive ion etching (RIE), the only way to release the 3C-SiC layer is wet KOH etching of the underlying Si. The resulting material is often rough due to Si residue from the etch which can diminish device performance in addition to adding

cost to the device manufacture (KOH etching can take more than an hour in most cases). Being able to employ oxide release layer strategies to SiC-based MEMS clearly would be a major step forward in SiC-MEMS technology, but in order to achieve this goal two things must happen. First, a low temperature 3C-SiC on Si growth process must be developed, which was reported in Chapter 3. Second, a poly-Si (or single-crystal but very thin) layer must be deposited on top of the oxide release layer to allow for the formation of the 3C-SiC film. In this chapter research to realize exactly this point is discussed where we have demonstrated a high-quality poly-3C-SiC on oxide film process that is suitable for subsequent MEMS manufacture which will be the subject of future work as outlined in the following chapter.

4.1 Introduction

The growth of highly oriented 3C-SiC formed directly on an oxide release layer, composed of a 20-nm-thick poly-Si seed layer and a 550-nm-thick thermally deposited oxide on a (111)Si substrate, was investigated as an alternative to using SOI substrates for freestanding SiC films for MEMS applications. The resulting SiC film was characterized by x-ray diffraction (XRD) with the x-ray rocking curve of the (111) diffraction peak displaying a FWHM of 0.115º (414″), which was better than that for 3C-SiC films grown directly on (111)Si during the same deposition process. However, the XRD peak amplitude for the 3C-SiC film on the poly-Si seed layer was much less than for the (111)Si control substrate due to slight in-plane misorientations in the film. Surprisingly, the film was solely composed of (111)3C-SiC grains and possessed no 3C-

SiC grains oriented along the <311> and <110> directions which were the original directions of the poly-Si seed layer. With this new process, MEMS structures such as cantilevers and membranes can be easily released leaving behind high-quality 3C-SiC structures. Films were delivered to SRI in Largo, FL and MEMS structures are being fabricated at this time and these results will be published in the future.

4.2 Motivation for 3C-SiC Growth on Oxide Layers

Silicon carbide, SiC, is a semiconductor material that is desirable for many power electronics and MEMS applications due to its wide band gap, mechanical resilience, robust thermal properties, and chemical inertness. However, many of these inherent properties create extreme difficulties when processing MEMS devices with this material. SiC chemical resistance reduces the effectiveness of wet chemical etching and requires the use of dry etching techniques involving reactive ion etching (i.e., DRIE/RIE). Fortunately, cubic silicon carbide, 3C-SiC, is the one polytype of SiC that can be grown heteroepitaxially on Si substrates, and the addition of this Si layer allows for many more processing options in device manufacturing. For example, one can utilize the Si substrate as a sacrificial layer for the creation of freestanding 3C-SiC MEMS structures (Beheim and Evans 2006) (Carter, et al. 2000). However, the recipes used to etch Si in DRIE/RIE have a similar etch rate with SiC, thereby excluding selectivity and reducing accuracy for the desired structure (Beheim and Evans 2006) (McLane and Flemish 1996) (Rosli, Aziz and Hamid 2006). Freestanding SiC MEMS devices using sacrificial Si layers have also encountered difficulties during device fabrication resulting from unetched Si preventing

the complete release of the structure (Beheim and Evans 2006) (Carter, et al. 2000). Silicon dioxide, SiO_2, has been traditionally used as an etch-stop in Si processing involving DRIE/RIE, and can be easily removed by wet chemistry processes to allow for the full release of freestanding structures (Federico, et al. 2003). With this in mind, silicon-on-insulator, SOI, substrates provide an excellent media for the creation of freestanding SiC devices by providing not only an oxide for the etch-stop for DRIE/RIE, but also a Si crystal seed layer for the heteroepitaxial growth of the 3C-SiC (Shimizu, Ishikawa and Shibata 2000) (Myers, Saddow, et al. 2004).

SOI provides some additional benefits for the growth of 3C-SiC as shown in previous studies (Shimizu, Ishikawa and Shibata 2000) (Myers, Saddow, et al. 2004). The high temperatures required for the growth of single-crystal 3C-SiC soften the SiO_2 layer, allow dispersion of stress caused by the ~20% lattice mismatch between SiC and Si, and suppress the formation of voids caused by Si evaporation at the 3C-SiC/ Si interface (Carter, et al. 2000). Although thick SOI seed layers (>50 nm) have been shown to produce 3C-SiC films that are of comparable quality when compared to 3C-SiC films grown on single-crystal Si substrates, the benefits of the epitaxial growth of 3C-SiC on SOI are realized when 3C-SiC is deposited on a thin (<50 nm) seed layer of Si, which produces excellent quality 3C-SiC (Shimizu, Ishikawa and Shibata 2000) (Myers, Saddow, et al. 2004). However, a major drawback of using SOI in the production of 3C-SiC devices is the fact that it requires extensive processing techniques (Shimizu, Ishikawa and Shibata 2000) (Myers, Saddow, et al. 2004). These processes add to the overall production cost of the device. In addition many MEMS devices do not require

single-crystal SiC material for proper functionality. A cost-efficient, easily produced wafer stack consisting of poly-Si/ SiO_2/ Si layers could replace the SOI substrate if poly-SiC is desired as a material for MEMS applications.

4.3 Deposition of Poly-Si Layer on SiO_2/ (111)Si

For our experiments we replaced the expensive SOI wafer with a stack of poly-Si/ SiO_2/ (111)Si, where the poly-Si serves as the seed layer for the growth of poly-SiC. The results of the growth were surprising because, instead of producing a layer of poly-SiC, the resulting growth was 3C-SiC that was highly oriented in the <111> direction, and contained no grains in the <110> direction, which was the favored orientation of the poly-Si grains. Substrate preparation for the growth experiments was as follows. A (111)Si wafer was RCA cleaned, followed by the CVD deposition of 5500 Å of silicon dioxide. After oxidation, a 50-nm-thick film of poly-Si was deposited by LPCVD at a temperature of 610°C and a pressure of 300 mTorr (Harbeke, et al. 1984). This process was chosen from the various poly-Si recipes for many reasons. The first is that a compressive stress is produced between the resulting poly-Si film and the oxide layer, which should help bring the Si crystal lattice into greater compliance with the 3C-SiC crystal lattice (Yang, et al. 2000). A secondary reason for the growth of poly-Si at this temperature is that it generates large columnar Si grains textured mainly in the <110> direction with a minor presence of grains textured in the <111> and <311> directions (Harbeke, et al. 1984). The resulting thin poly-Si film was characterized by both AFM and XRD to ascertain the starting growth surface properties. The AFM, performed on a

PSIA XE-100 microscope, shows a surface with grains of average area on the order of 5.5 nm^2, having an average surface roughness of 0.49 nm rms, but also indicated the presence of pinholes in the surface. The XRD measurements were performed on a Philips Panalytical X'pert Diffractometer operating at the Cu K-α line, and the measurements indicated alignment of the poly-Si grains in the <110>, <111>, and <311> directions, as was expected from the literature (Harbeke, et al. 1984) (Yang, et al. 2000). The pinholes created difficulties during the deposition of 3C-SiC by creating a pathway for softened oxide material to flow onto the growth surface thus destroying the 3C-SiC film morphology. Therefore, the temperature for growth was reduced from temperatures developed by M. Reyes, et al. to eliminate this problem, resulting in the maximum growth temperature for 3C-SiC on the film stack of 1200°C.

4.4 3C-SiC Growth on Poly-Si/ SiO_2/ (111)Si Stack

The finalized growth process is as follows. The poly-Si/ SiO_2/ (111)Si wafer stack was placed in a horizontal, hot-wall reactor heated by the RF induction of a SiC-coated graphite susceptor. The wafer was loaded into a molded poly-SiC plate to fix the position of the wafer within the reactor hot zone. This poly-SiC plate was then seated into a recess in the susceptor and the chamber was sealed and evacuated of residual gases. The chamber was then filled with palladium-purified hydrogen to a pressure of 400 Torr. The 3C-SiC process developed for this reactor involves two main process stages, namely the carbonization and growth stages (Reyes, Shishkin, et al., Development of a high-growth rate 3C-SiC on Si CVD process 2006). The pressure for the carbonization

process was 400 Torr, and growth pressure was 100 Torr. The standard gases used for 3C-SiC growth are: palladium-purified hydrogen, H_2, which is used as the transport gas; propane (C_3H_8), which is the carbon precursor; and a 10% silane (SiH_4) premixed in hydrogen, which is the silicon precursor.

The carbonization stage occurred while the sample temperature was ramped to 1135°C at a rate of ~ 35°C/min. Throughout the ramp, a 2.38×10^{-3} C mole fraction was maintained. Once the carbonization temperature was reached, the temperature was maintained for 2 min to allow for conversion of the poly-Si surface into 3C-SiC. After carbonization and the creation of the 3C-SiC template layer, the temperature was ramped a second time at a rate of 35°C/min to the growth temperature of 1200°C. During this ramp, we determined that it is advantageous to slowly decrease the flow of C_3H_8 while simultaneously introducing and increasing the flow of SiH_4. H_2 flow was maintained at 10 slm until 30°C before the ramp was completed, where it was increased to 25 slm, and the pressure was reduced from 400 Torr to 100 Torr. At the growth temperature the silicon to carbon ratio, Si/C, for the growth stage was 0.94, with a 3.94×10^{-4} C mole fraction and a 3.71×10^{-4} Si mole fraction. The temperature and gas flows were then held constant, allowing for the continued epitaxial growth of 3C-SiC on the carbonized poly-Si buffer layer. The reactor had no wafer rotation, so the process parameters produced a growth rate of 3.0 µm/h at the upstream-side of the wafer and 2.5 µm/h at the downstream-side of the wafer due to precursor depletion. This rate, measured using an Accent QS-1200 FTIR system to determine film thickness, was also verified on samples

of 3C-SiC grown on single-crystal Si oriented in the <100> and <111> directions using identical process conditions as reported above.

4.4.1 AFM Analysis

AFM surface analysis was used to characterize the film morphology as shown in Figure 4.1. The growth of SiC on the poly-Si/ SiO_2/ (111)Si substrate was compared with 3C-SiC grown directly on (100) and (111)Si substrates. The morphology of the surface of the 3C-SiC on the poly-Si stack was similar to that of the 3C-SiC grown on Si (111), showing growth of ordered triangular island grains of similar size. The AFM micrograph of 3C-SiC grown on Si (100) has smaller, rounded, and more disassociated island growth with a large distribution in grain size. A cross-section SEM micrograph displays the growth of 3C-SiC on the poly-Si stack near the downstream sector of the wafer shown in Figure 4.2. This cross-section SEM, performed on a Hitachi 4800 microscope, shows that the thickness of the 3C-SiC film grown for 30 min on the poly-Si stack was ~1.3 μm, verifying the growth rate as measured by FTIR. An important aspect of this growth process is that the oxide remained perfectly intact and was unaffected during the growth of the 3C-SiC.

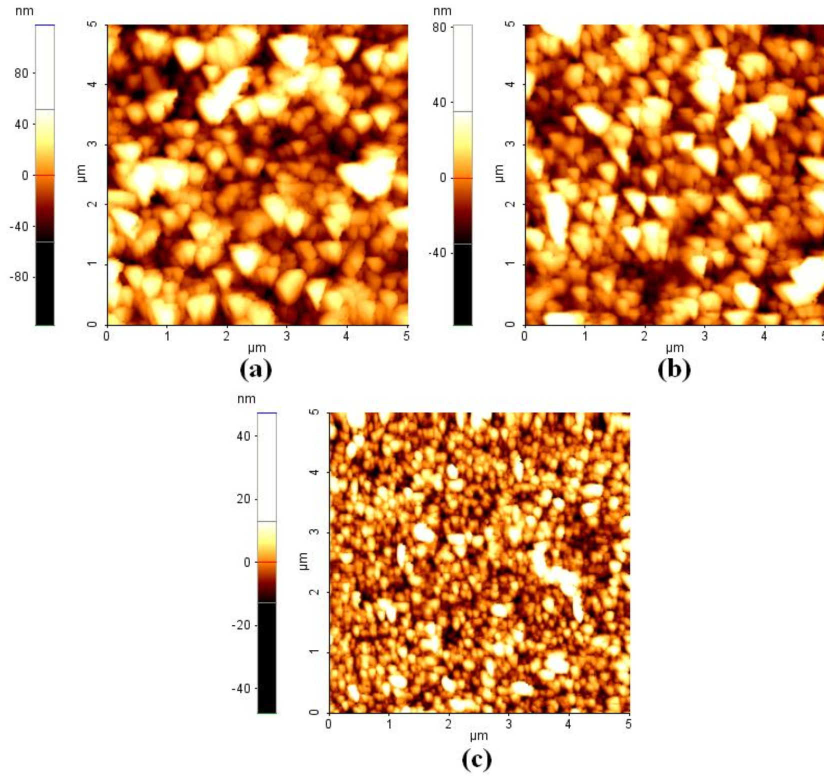


Figure 4.1 AFM micrographs of the surfaces of the SiC deposition grown on (a) poly-Si/ SiO_2/ (111)Si, (b) (111)Si, and (c) (100)Si. The 5µm x 5µm images were collected in contact mode using a SiN tip. The respective z resolution and r_q values are (a)-78nm to 81.4nm, r_q=17.9nm, (b) -117.3nm to 118.4nm, r_q= 26.5nm, and (c) -47.7nm to 47.5nm, r_q=6.57nm.

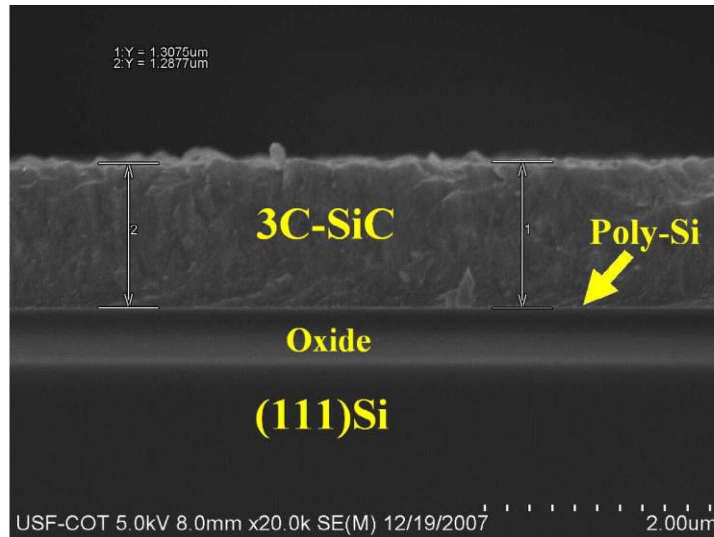


Figure 4.2 Cross-section SEM micrograph of a 3C-SiC film grown on the poly-Si/ SiO_2/ (111)Si compliant stack. The 3C-SiC grown has a thickness of ~1.3µm and the SiO_2 layer is ~0.55µm thick. The poly-Si layer was estimated to be ~20nm. Note that the SiC/ SiO_2 interface is undamaged.

4.4.2 XRD Analysis

Figure 4.3 shows the XRD θ-2θ diffraction spectra and high-resolution rocking curves performed on the 3C-SiC films for determination of the crystal orientation and quality of the 3C-SiC layer. For the 3C-SiC film grown on the poly-Si/ SiO_2/ (111)Si stack a very strong peak was observed at 35.6º while a weaker peak at ~71.8º is due to reflections from the (111)3C-SiC and (311)3C-SiC planes, respectively. It is also evident that there are no SiC reflections originating from the <110> direction, which were the main grain orientations present in the poly-Si seed layer. A comparison of the relative peak intensities suggests a preference for grain alignment in the <111> direction, while very few grains appear to be aligned along the <311> direction. The 3C-SiC films grown on (111)Si and (100)Si show dominant peaks at 35.6° and 41.4°, respectively.

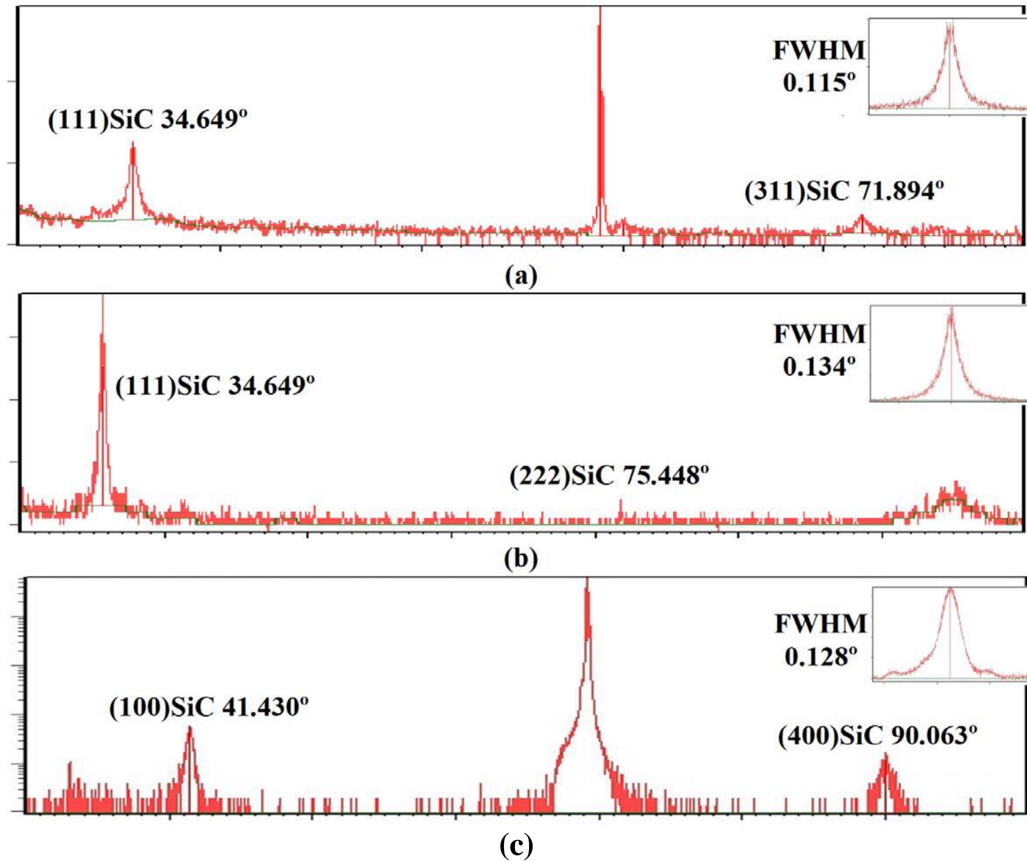


Figure 4.3 XRD θ-2θ diffraction surveys for the 3C-SiC films grown on (a) poly-Si/ SiO_2/ (111)Si, (b) (111)Si, and (c) (100)Si substrates. The XRD θ-2θ scans show that (a) and (b) possess a primary peak at 35.6°, and (c) possesses a primary peak at 41.4°. Insets: rocking curves for each of the 3C-SiC films taken at their respective primary Bragg peaks. The FWHM values are 0.115° (414″), 0.134° (482″), and 0.128° (460″), respectively.

The rocking curves were taken at the primary Bragg peak for each the 3C-SiC epitaxial films. The insets displayed in Figure 4.3 show the results of the rocking curves obtained for each substrate type. The rocking curve for the 3C-SiC films on poly-Si/ SiO_2/ (111)Si substrate displayed a FWHM of 0.115º (414″), the 3C-SiC on (111)Si was 0.134º (482″), and the 3C-SiC on (100)Si displayed FWHM value of the 41.4° peak of 0.128º (460″). The correlation of the FWHM values from the growth performed on poly-

Si/ SiO_2 / (111)Si versus the growth performed on single-crystal Si appears to suggest that all films have relatively comparable crystallinity. This correlation proves to be very interesting because the growth of the 3C-SiC film on the poly-Si/ SiO_2 / (111)Si stack began on a poly-Si seed layer with multiple orientations, and when compared to 3C-SiC films by Carter, et al. (Carter, et al. 2000) grown on SOI of similar Si seed and oxide layer thicknesses (50 nm and 0.5 μm, respectively), the reported FWHM value was 0.20° (720″), which is almost double the FWHM of the 3C-SiC grown on the poly-Si seed reported in this work.

Speculation suggests that the result of the weak amplitude from the Bragg reflections seen in the θ-2θ diffraction scan and the relatively narrow FWHM measurement from the rocking curves indicate a highly-ordered polycrystalline 3C-SiC layer in which the crystallites are misaligned relative to each other but all appear to be of the <111> direction. While the <111> direction of the 3C-SiC planes of the various grains are still approximately parallel to one another, producing a relatively narrow rocking curve, the (111) planes rotated about the <111> direction would produce a weak amplitude count in the θ-2θ survey.

4.5 Summary

In summary, a well ordered polycrystalline 3C-SiC film with grains predominantly along the <111> direction has been successfully grown on a poly-Si/SiO_2/ (111)Si wafer and the process results verified multiple times. This process was developed to create an easy to release 3C-SiC layer for use in MEMS applications and, therefore,

will be useful for MEMS applications that will benefit from 3C-SiC structures. The cost-effectiveness and relative ease for the deposition of both oxide and poly-Si make this process superior to the methods used to fabricate SOI substrates, and the oxide layer provides more device processing options than 3C-SiC grown directly on single crystal Si. Fortuitously, the resulting 3C-SiC films were highly ordered in the <111> direction and their quality assessed using AFM, SEM, and XRD analysis. The quality of the ordered 3C-SiC grown on the poly-Si stack is comparable to that of 3C-SiC grown on a single crystal Si, and much better than that of 3C-SiC grown on conventional SOI as reported in literature.

CHAPTER 5: SUMMARY AND FUTURE WORKS

5.1 Summary

A low temperature heteroepitaxial process has been developed and characterized for the growth of 3C-SiC on 50mm (111)Si substrates. A "baseline" high temperature process was first developed from a previously established 3C-SiC on (100)Si high temperature growth process. From this baseline process, a low temperature baseline process was developed and optimized and then applied to 3C-SiC growth on a poly-Si/ SiO_2/ (111)Si compliant substrate stack.

The initial base line for 3C-SiC deposition was achieved using a two-step growth process, carbonization of the Si substrates proceeded with a growth plateau. The substrate was first heated from room temperature to 1135°C in a mixture of a H_2/C_3H_8 (10 slm/16 sccm) at 400 Torr. Once at 1135°C, the substrate was maintained at this temperature for two minutes to carbonize the surface. The temperature was then increased from 1135°C to 1380°C. During this temperature ramp, the H_2 flow was increased to 40 slm and the pressure was reduced from 400 Torr to 100 Torr. The SiH_4 was introduced into the gas mixture at 10sccm and increased at intervals to the final flow rate of 220sccm. Meanwhile, the propane was simultaneously decreased at intervals to 6 sccm. The resulting film was specular and demonstrated low crystal defects as measured via XRD and TEM analysis.

The high temperature baseline process was then adapted for low temperature growth. The carbonization occurred at 1135°C while 10 slm of H_2 and 16 sccm of C_3H_8 flowed through the reactor. The carbonization process lasted for a two minute duration. The temperature was ramped from 1135°C to 1200°C. It was discovered after several low temperature optimization experiments that a lower flow rate of the H_2 carrier was required than the high temperature growth process. During the temperature ramp from the carbonization plateau to the growth plateau, a H_2 flow rate of 25 slm was implemented. In order to increase the deposition rate at the lower temperature, the growth pressure needed to be decreased to 75 Torr, the minimum chamber pressure possible for the MF2 CVD reactor. Under the optimized conditions, the deposition rate improved from 1.4µm/h to 1.9µm/h with the transparent film exhibiting a smooth, specular morphology.

Finally, the optimized low temperature process was used to deposit 3C-SiC on an oxide compliant substrate. Compliant substrates should soften at the deposition temperature and allow the strain inherent to heteroepitaxy to reside in the substrate thus ensuring a high-quality film is formed. Deposition experiments on the poly-Si/ SiO_2/ (111)Si stacks and various orientations of crystalline Si substrates were performed in tandem. Initial measurements using XRD revealed crystal quality that rivaled or exceeded the films deposited on the crystalline Si substrates. Further investigation using TEM and AFM analysis revealed that the films deposited on the compliant substrate stack were highly-textured polycrystalline silicon carbide which seems to be ideal for MEMS applications which we intend to exploit in the near future.

5.2 Future Works

A cost-effective growth process capable of producing nearly defect-free SiC will need to be developed in order for silicon carbide to be considered a commercially viable material for electronic and MEMS applications. Unfortunately, (111) oriented 3C-SiC films grown directly on crystalline Si substrates are plagued by stress-related issues, such as film deformation, commonly referred to as wafer bow, and fracturing, that overwhelm any benefits.. Several techniques have been investigated to overcome the mismatch issues associated with SiC heteroepitaxial growth, but compliant substrates offer the most promising approach for the realization of devices formed on mismatched heteroepitaxial materials (Ayers 2008). A wide variety of compliance methods have been developed over the years where a majority of the methods involve a thin film serving as a crystal seed template layer for epitaxial growth that decouples the thicker substrate from the epitaxy (Ayers 2008). The benefit of using an oxide-based compliant substrate is that the oxide can be easily etched away thus it serves double duty as a MEMS release layer. This would be invaluable for the advancement of the SiC-based MEMS and bio-MEMS vision of the SiC Group at the University of South Florida.

5.2.1 3C-SiC Growth on SOI Substrates

As previously discussed, oxide-based compliant substrates offer a stress-relaxation mechanism and the benefit of an etch-stop release layer. The work done on the poly-Si/ SiO_2/ Si compliance stack offers many avenues to explore. While the benefit of using a CVD deposited poly-seed layer is that it can be deposited using readily accessible

tools, producing the very thin films necessary for compliancy but potentially leaving "pinholes" within the seed-layer. A viable solution to overcome this issue is to grow thicker CVD deposited Si films and follow with dry oxidation and HF etching of the Si layer. The low oxidation rate of dry oxidation would offer better control of the seed layer thickness. The poly-Si/ SiO_2/ Si stack produces highly-oriented polycrystalline 3C-SiC, but a monocrystalline template is needed to produce highly crystalline 3C-SiC. Initial work in the SiC Group at USF involving the growth of 3C-SiC on SOI via cold-wall CVD that was conducted by Dr. R. L. Myers-Ward while working with silicon bonded wafers produced by Dr. Karl Hobart of NRL and work involving a Si/ poly-SiC SOI substrate was performed by S. Harvey via hot-wall CVD using the MF1 reactor (Harvey 2006). The compliancy of the oxide layer could be supplemented with the incorporation of various dopants into the silicon over layer (SOL) of the SOI substrate to create a buffer layer to deposit 3C-SiC. $Si_xGe_{(1-x)}$ alloys have already been incorporated into the SOL of SOI substrates and have demonstrated improved epitaxial film quality when compared to non-compliant substrates (Ayers 2008). What was lacking during the previous work on SOI substrates in our group was a high-quality, low-temperature 3C-SiC on Si growth process and now that this process has been developed as part of this work perhaps it is time to revisit SOI as a means to form high-quality films for electronic device applications.

5.2.2 Residual Stress Characterization

The fundamental issue regarding heteroepitaxial growth, or any film growth for that matter, is the degree of in-plane film stress and how the film responds to that stress. Characterization the 3C-SiC film stress is going to be necessary in order to quantify and evaluate the effectiveness of 3C-SiC growth on future compliant substrates. It is only recently that tools have become readily available at USF to make the necessary measurements. A recently established collaboration with Dr. A. Volinsky in the mechanical engineering department has provided us with new characterization opportunities. Nanoindentation can provide important data regarding film hardness and fracture toughness. Several tools are available for wafer/film deformation analysis from which film stress can be extracted via the modified Stoney's equation. While deformation analysis provides valuable stress-related data, it tends to be sensitive and assumptions made in the derivation of the modified Stoney's equation can produce large errors. Other techniques will need to be incorporated in order to supplement this data. Micro Raman Spectroscopy and XRD analysis can prove useful for quantifying in-plane film strain/ stress of highly-textured 3C-SiC films by measuring the peak-shifts in stressed films; however XRD can be very sensitive to measurement error if the peaks are located at 2θ greater than 90°. Incorporation of these stress analysis techniques into the current characterization protocol of the SiC Group at USF will provide enhanced feedback for continued improvement of the 3C-SiC heteroepitaxy process.

5.2.3 MEMS Fabrication

Perhaps the most obvious future work task emanating from this thesis research is to take the materials developed and form high-quality MEMS structures, either for mechanical MEMS or bio-MEMS applications. Given the thrust of the USF SiC group into the bioengineering arena, this work would support a whole host of research on-going in the group and thus allow for critical mass to be achieved, which is difficult to do in a university research group that is not located within a research center. Three tasks are recommended in this area. 1) micro-machine 3C-SiC on (100)Si films and compare stress values to realized structure bow so as to correlate and correct stress measurement analysis and modified Stoney's equation methods discussed in the previous section. 2) grow additional poly-3C-SiC on oxide films, micro-machine them and compare the structure bow with pre-release mechanical stress measurements to see how well they correlate. And finally 3) re-start 3C-SiC on SOI substrate research, both for MEMS applications as well as realizing high-quality 3C-SiC films for electronic applications. If these 3 tasks are pursued there is a high probability that breakthroughs in 3C-SiC on Si technology can be made so that this polytype of SiC, the so called 'dark horse' of SiC, can take its place as the preferred polytype due to its lower cost of epi growth and possibility for realization on large-area, inexpensive Si substrates. To achieve this goal clearly more work needs to be done but the ground work has been laid in this thesis research as well as others around the world and there is hope that this dream may become a reality in the near future.

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