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Design and Fabrication of Multi – Dimensional RF MEMS Variable Capacitors

by

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A thesis submitted in partial fulfillment
of the requirements for the degree of
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Department of Electrical Engineering
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TABLE OF CONTENTS

LIST OF TABLE iii

LIST OF FIGURES v

ABSTRACT x

CHAPTER 1 INTRODUCTION 1
- 1.1 Overview 1
- 1.2 Thesis Organization 3
- 1.3 Contributions 4

CHAPTER 2 BACKGROUND STUDY 5
- 2.1 Introduction 5
- 2.2 Micromachining Techniques 5
  - 2.2.1 Bulk Micromachining 6
  - 2.2.2 Surface Micromachining 6
  - 2.2.3 LIGA 6
- 2.3 MEMS Actuation 7
  - 2.3.1 Thermal Actuation 7
  - 2.3.2 Piezoelectric and Magnetic Actuation 7
  - 2.3.3 Electrostatic Actuation 7
- 2.4 Study of MEMS Tunable Capacitors for RF Application 8
  - 2.4.1 MEMS Tunable Capacitors Utilizing Thermal Actuation Principle 9
  - 2.4.2 MEMS Tunable Capacitors Utilizing Zipper Actuation Principle 10
  - 2.4.3 MEMS Tunable Capacitors Utilizing Electrostatic Actuation Principle 10
- 2.5 Summary 11

CHAPTER 3 DESIGN TECHNIQUE 12
- 3.1 Introduction 12
- 3.2 Design of Multi-Dimensional RF MEMS Variable Capacitors 12
  - 3.2.1 CPW Transmission Line Design 13
  - 3.2.2 TRL Calibration Standards Design 13
  - 3.2.3 Capacitor Design 14
  - 3.2.4 Cantilever Beam Design 15
- 3.3 Capacitor Simulation 17
- 3.4 Summary 21

CHAPTER 4 FABRICATION TECHNIQUE 22
4.1 Introduction 22
4.2 Silicon Substrate Characteristics 23
4.3 Process Flow 23
4.3.1 Pattern First Metal (CPW) 23
4.3.2 Silicon Monoxide Deposition 25
4.3.3 Pedestal Gold Electroplating 25
4.3.4 Beam Formation and Final Release 25
4.3.5 Release Process 26
4.4 Problems in Fabrication Technique 26
4.4.1 Shorting of Electrodes 26
4.4.2 Membrane Release Failure 27
4.4.3 Stiction 27
4.5 Summary 28

CHAPTER 5 MEASUREMENTS AND MODELING 29
5.1 Introduction 29
5.2 TRL Calibration Technique 29
5.3 Measurement Setup 34
5.4 Equivalent Circuit Modeling 35
5.5 Quality Factor Measurements 41
5.6 Summary 43

CHAPTER 6 STUDY ON ANODIC BONDING TECHNIQUES 44
6.1 Introduction 44
6.2 Anodic Bonding 44
6.3 Improved Anodic Bonding Technique 45
6.4 Procedure for Anodic Bonding Process 47
6.4.1 Silicon Wafer Cleaning 47
6.4.2 Glass Cleaning 47
6.4.3 Experimental Procedure 48
6.5 Summary 48

CHAPTER 7 CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK 49
7.1 Conclusion 49
7.2 Recommendations for Future Work 50

REFERENCES 51

APPENDICES 55
Appendix A: Physical Characteristics and the Calculated Actuation Voltage of the Multiple Beam Capacitor Topologies 56
Appendix B: Multi – Dimensional RM MEMS Variable Capacitor with a 1 – Beam Topology 60
Appendix C: Multi – Dimensional RM MEMS Variable Capacitor with a 2 – Beam Topology 66
Appendix D: Multi – Dimensional RM MEMS Variable Capacitor with a 3 – Beam Topology 72

LIST OF TABLES

Table 1.1: Comparison between a RF MEMS Switch and Active Switches Fabricated using Active Component 2

Table 1.2: Typical Performance of the MEMS Varactor Designed with 5 Beams Suspended on a Single Pedestal 4

Table 2.1: Comparison of Switching Speed, Actuation Voltage, and Power Consumption of Various Actuation Mechanisms 8

Table 2.2: Performance Based Comparison of RF MEMS Variable Capacitors by Various Researchers 11

Table 3.1: Physical Characteristics of the Multiple Beam Capacitor Topologies (Beam Topology, Beam Area, Up / Down State Capacitance) 15

Table 3.2: Calculated Actuation Voltage (Equation 3.4) for the Beams Incorporated in the Capacitor Structures 17

Table 3.3: Comparison of the Theoretical Capacitance Value with the EM Simulated Capacitance Value 20

Table 5.1: General Guidelines to Verify the Accuracy of Calibration Procedure 31

Table 5.2: Comparison of the Theoretical Value of the Capacitor (Equation 3.1 and 3.2) with the Extracted Capacitance Value in the Up and Down State (5 – Beam Topology) 36

Table 5.3: Lumped Element Equivalent Circuit Component Values for the One Port MEMS Variable Capacitor in the Up – State and Down – State 37

Table 5.4: Extracted Q Factor at 1GHz Using the Measurement Data and the Model 41

Table 5.5: Performance Based Comparison of RF MEMS Variable Capacitors with Other Researchers 43

Table 6.1: Comparison of Bonding Time for Different Temperatures at 1000 Volts 46

Table A.1: Physical Characteristics of the Multiple Beam Capacitor Topologies (Beam Topology, Beam Area, Up / Down State Capacitance) 56

Table A.2: Calculated Actuation Voltage (Equation 3.4) for the Beams Incorporated in the Capacitor Structures 58

Table B.1: Comparison of the Theoretical Capacitance Value with the EM Simulated Capacitance Value for the 1 – Beam Topology Capacitor 61

Table C.1: Comparison of the Theoretical Capacitance Value with the EM Simulated Capacitance Value for the 2 – Beam Topology Capacitor 67

Table D.1: Comparison of the Theoretical Capacitance Value with the EM Simulated Capacitance Value for the 3 – Beam Topology Capacitor 73

LIST OF FIGURES

Figure 1.1: A Multi Dimensional RF MEMS Variable Capacitor with a Three Beam Topology 2

Figure 2.1: RF MEMS Tunable Capacitor with a Single Beam Topology 9

Figure 3.1: A Three Beam Topology MEMS Variable Capacitor 13

Figure 3.2: Schematic of a 50Ω CPW Transmission Line 13

Figure 3.3: A MEMS Capacitor with a Single Beam Topology in its (a) Up – State (b) Down – State 15

Figure 3.4: Top View of the 5 – Beam Capacitor Topology used in Momentum Simulation 18

Figure 3.5: Theoretical Response (First Order Approximation) of the Capacitance Value of the Five Beam Topology 18

Figure 3.6: EM Simulation Plots of S_{11} Magnitude as a Function of Frequency for a 5 – Beam Topology at Various Beam States 20

Figure 3.7: EM Simulation Plots of S_{11} Phase as a Function of Frequency for a 5 – Beam Topology at Various Beam States 21

Figure 4.1: Process Flow of the Multi Dimensional RF MEMS Variable Capacitors Cross Sectional View (1) CPW / Bottom Electrode Deposition (2) Dielectric Layer Deposition (3) Pedestal Electroplating (4) Top Electrode Deposition (5) Membrane Release (b) Top View (1) CPW / Bottom Electrode Deposition (2) Dielectric Layer Deposition (3) Pedestal Electroplating (4) Top Electrode Deposition and Membrane Release 24

Figure 4.2: Experimental Setup for Gold Electroplating 25

Figure 4.3: Partial Shorting (Indicated by Dotted Line) at the Interface of Edge of the Bottom Electrode and the Dielectric Layer 27

Figure 5.1: Calibration Standards for the TRL Calibration Technique 30

Figure 5.2: Magnitude of S_{21} for the Thru 32

Figure 5.3: Phase of S_{21} for the Thru 32

Figure 5.4: Magnitude of S_{11} for the Thru 33

Figure 5.5: Magnitude of S_{11} for the Delay Line 33

Figure 5.6: Magnitude of S_{11} for the Reflect 34

Figure 5.7: Measurement Setup used for Measuring the One – port MEMS Variable Capacitors 35

Figure 5.8: Lumped Element Equivalent Circuit Model for the One – Port MEMS Variable Capacitor (5 – Beam Topology) 36

Figure 5.9: Comparison of Measured and Theoretical Capacitance as a Function of Voltage (5 – Beam Topology) 38

Figure 5.10: Comparison between the S_{11} Magnitude of the Measured and the Modeled Capacitor (5 – Beam Topology) in the Up – State 39

Figure 5.11: Comparison between the S_{11} Phase of the Measured and the Modeled Capacitor (5 – Beam Topology) in the Up – State 39

Figure 5.12: Comparison between the S_{11} Magnitude of the Measured and the Modeled Capacitor (5 – Beam Topology) in the Down – State 40

Figure 5.13: Comparison between the S_{11} Phase of the Measured and the Modeled Capacitor (5 – Beam Topology) in the Down – State 40

Figure 5.14: Comparison between the Q – Factor of the Measured and the Modeled Capacitor (5 – Beam Topology – Figure 5.8) in the Up – State 42

Figure 5.15: Comparison between the Q – Factor of the Measured and the Modeled Capacitor (5 – Beam Topology – Figure 5.8) in the Down – State 42

Figure 6.1: Schematic Showing the Anodic Bonding Process between Silicon and Glass 45

Figure 6.2: Schematic of the Anodic Bonding Setup 46

Figure 6.3: Schematic of the Improved Anodic Bonding Setup 47

Figure 7.1: Single Beam Topology MEMS Variable Capacitor (a) Suspended Beam (b) Meandered Beam 50

Figure B.1: Top View of the 1 – Beam Capacitor Topology used in Momentum Simulation 60

Figure B.2: EM Simulation of S_{11} Magnitude as a Function of Frequency for a 1 – Beam Topology at Various Beam States 60

Figure B.3: EM Simulation of S_{11} Phase as a Function of Frequency for a 1 – Beam Topology at Various Beam States 62

Figure B.4: Comparison of Measured and Theoretical Capacitance as a Function of Voltage for the 1 – Beam Topology Capacitor 62

Figure B.5: Comparison between the S_{11} Magnitude of the Measured and the Modeled Capacitor (1 – Beam Topology) in the Up – State 62

Figure B.6: Comparison between the S_{11} Phase of the Measured and the Modeled Capacitor (1 – Beam Topology) in the Up – State 63

Figure B.7: Comparison between the S_{11} Magnitude of the Measured and the Modeled Capacitor (1 – Beam Topology) in the Down – State 63

Figure B.8: Comparison between the S_{11} Phase of the Measured and the Modeled Capacitor (1 – Beam Topology) in the Down – State 64

Figure B.9: Comparison between the Q – Factor of the Measured and the Modeled Capacitor (1 – Beam Topology) in the Up – State 64

Figure B.10: Comparison between the Q – Factor of the Measured and the Modeled Capacitor (1 – Beam Topology) in the Down – State 65

Figure C.1: Top View of the 2 – Beam Capacitor Topology used in Momentum Simulation 66

Figure C.2: EM Simulation of S_{11} Magnitude as a Function of Frequency for a 2 – Beam Topology at Various Beam States 66

Figure C.3: EM Simulation of S_{11} Phase as a Function of Frequency for a 2 – Beam Topology at Various Beam States 67

Figure C.4: Comparison of Measured and Theoretical Capacitance as a Function of Voltage for the 2 – Beam Topology Capacitor 68

Figure C.5: Comparison between the S_{11} Magnitude of the Measured and the Modeled Capacitor (2 – Beam Topology) in the Up – State 68

Figure C.6: Comparison between the S_{11} Phase of the Measured and the Modeled Capacitor (2 – Beam Topology) in the Up – State 69

Figure C.7: Comparison between the S_{11} Magnitude of the Measured and the Modeled Capacitor (2 – Beam Topology) in the Down – State 69

Figure C.8: Comparison between the S_{11} Phase of the Measured and the Modeled Capacitor (2 – Beam Topology) in the Down – State 70

Figure C.9: Comparison between the Q – Factor of the Measured and the Modeled Capacitor (2 – Beam Topology) in the Up – State 70

Figure C.10: Comparison between the Q – Factor of the Measured and the Modeled Capacitor (2 – Beam Topology) in the Down – State 71

Figure D.1: Top View of the 3 – Beam Capacitor Topology used in Momentum Simulation 72

Figure D.2: EM Simulation of S_{11} Magnitude as a Function of Frequency for a 3 – Beam Topology at Various Beam States 72

Figure D.3: EM Simulation of S_{11} Phase as a Function of Frequency for a 3 – Beam Topology at Various Beam States 73

Figure D.4: Comparison of Measured and Theoretical Capacitance as a Function of Voltage for the 3 – Beam Topology Capacitor 74

Figure D.5: Comparison between the S_{11} Magnitude of the Measured and the Modeled Capacitor (3 – Beam Topology) in the Up – State 74

Figure D.6: Comparison between the S_{11} Phase of the Measured and the Modeled Capacitor (3 – Beam Topology) in the Up – State 75

Figure D.7: Comparison between the S_{11} Magnitude of the Measured and the Modeled Capacitor (3 – Beam Topology) in the Down – State 75

Figure D.8: Comparison between the S_{11} Phase of the Measured and the Modeled Capacitor (3 – Beam Topology) in the Down – State 76

Figure D.9: Comparison between the Q – Factor of the Measured and the Modeled Capacitor (3 – Beam Topology) in the Up – State 76

Figure D.10: Comparison between the Q – Factor of the Measured and the Modeled Capacitor (3 – Beam Topology) in the Down – State 77

DESIGN AND FABRICATION OF MULTI-DIMENSIONAL RF MEMS VARIABLE CAPACITORS

Hariharasudhan T Kannan

ABSTRACT

In this work, a multi dimensional RF MEMS variable capacitor that utilizes electrostatic actuation is designed and fabricated on a 425µm thick silicon substrate. Electrostatic actuation is preferred over other actuation mechanisms due to low power consumption. The RF MEMS variable capacitor is designed in a CPW topology, with multiple beams supported (1 – 7 beams) on a single pedestal. The varactors are fabricated using surface micromachining techniques. A 1µm thick silicon monoxide (ε_r – 6) is used as a dielectric layer for the varactor. The movable membrane is suspended on a 2.5µm thick electroplated gold pedestal. The capacitance between the membrane and the bottom electrode increases as the bias voltage between the membrane and the bottom electrode is increased, eventually causing the membrane to snap down at the actuation voltage. For the varactors designed herein, the actuation voltage is approximately 30 – 90V.

Full-wave electromagnetic simulations are performed from 1 – 25GHz to accurately predict the frequency response of the varactors. The EM simulations and the measurement results compare favorably. A series RLC equivalent circuit is used to model the varactor and used to extract the parasitics associated with the capacitor by optimizing the model with the measurement results. The measured capacitance ratio is approximately 12:1 with a tuning range from 0.5 – 6pF. Furthermore, the measured S-parameter data is used to extract the unloaded Q of the varactor (at 1GHz) and is found to be 234 in the up state and 27 in the down state.

An improved anodic bonding technique to bond high resistivity Si substrate and low alkali borax glass substrate that finds potential application towards packaging of MEMS varactors is investigated. To facilitate the packaging of the varactors the temperature is maintained at 400°C. The bonding time is approximately 7min at an applied voltage of 1KV.

CHAPTER 1

INTRODUCTION

1.1 Overview

MICROELECTROMECHANICAL systems (MEMS) technology offers an attractive capability for RF systems, particularly in support of switching and tuning functions. MEMS have enabled the performance, reliability and function of devices to be increased while driving down their size and cost at the same time. The technology includes circuit tuning elements (capacitors, inductors), resonators, filters, microphones and switches. These low-loss ultra-miniature and highly integrative RF functions can eventually replace classical RF elements and enable a new generation of RF devices.

The advantages of RF MEMS are found in terms of low loss and good isolation over a large frequency range, low power consumption and low cost. These performance factors have driven investigations into where these devices can be employed in RF systems. Applications where RF MEMS finds use include reconfigurable antenna elements, implementation in phase shifters and RF tuning filters. The near ideal behavior of the RF MEMS devices warrants the use in microwave circuit instead of semiconductor based technology. Table 1.1 shows a comparison between a RF MEMS switch and switch designed using active components. Since MEMS circuits use mechanical movement they have relative low switching speed (>5μs) while switching speed utilizing semiconductor based technology is on the order of 1 – 10ns.

In this work, a one – port multi dimensional RF MEMS variable capacitor that utilizes electrostatic actuation is successfully designed and fabricated on a 425μm thick silicon substrate (ε_r – 11.7). One of the goals of this work is to provide digital type tuning over a frequency range of 1 – 25GHz with a relatively simple varactor design.

Table 2.1: Comparison between a RF MEMS Switch and Active Switches Fabricated using Active Component [1]

Switch Type	Properties			
	Insertion Loss	Isolation	Power Consumption	Switching Speed
PIN/Schottky	0.15dB	45dB	1 – 5mW/device	1 – 5ns
GaAs FET's	1 – 2dB	20dB	1 – 5mW/device	2 – 10ns
HBT/PIN	0.82dB	25dB	1 – 5mW/device	1 – 5ns
Best FET	0.5dB	70dB	5mW	2ns
MEMS	0.06dB	30dB	1uW	>5us

The varactors are designed in a CPW topology, with multiple beams supported on a single pedestal (Figure 1.1). Silicon monoxide (ε_r – 6) is used as the dielectric between the bottom electrode and the cantilever beam. When a DC voltage is applied between the center conductor and the ground plane the electrostatic force pulls the cantilever beam towards the ground, thereby, decreasing the spacing between the electrodes. Using a parallel plate approximation, increase in the capacitance value that is inversely proportional to the electrode spacing is obtained.

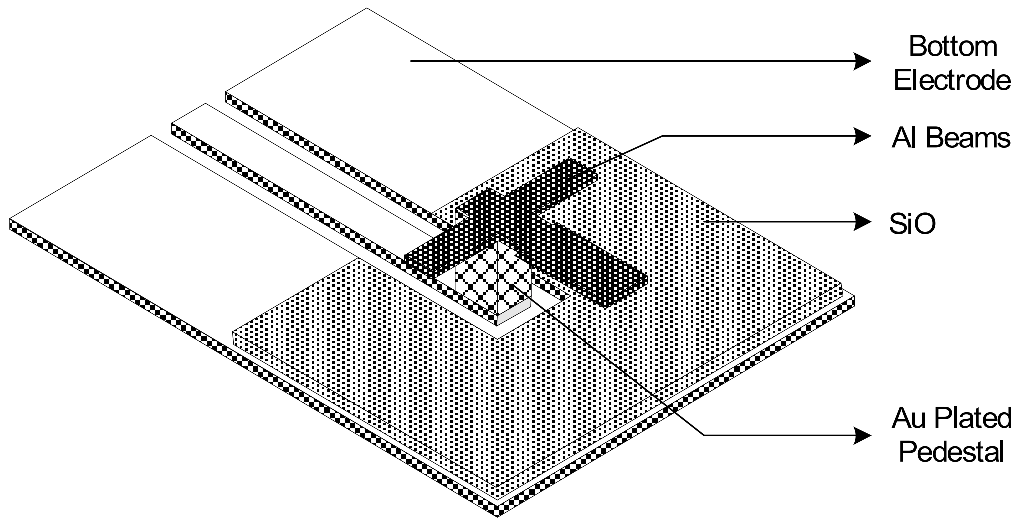

Figure 1.1: A Multi Dimensional RF MEMS Variable Capacitor with a Three Beam Topology

A full wave electromagnetic (EM) simulation is used to analyze the performance of the multi dimensional varactor. The parasitics associated with the design are accurately captured via EM

simulation. A lumped equivalent circuit model is used to extract the capacitance and the parasitics from 1 – 25GHz. The measurement results show good agreement with the simulated results. Furthermore, the unloaded quality (Q) factor of the varactor that is extracted from the measurement result indicates a low loss design for both the up and down states.

1.2 Thesis Organization

The basic micromachining techniques and the different actuation mechanisms used for actuating the MEMS devices are briefly discussed in Chapter 2. The background study of MEMS tunable capacitors for RF applications and a performance based comparison of RF MEMS variable capacitors are briefly described.

The design of the multi dimensional MEMS variable capacitors is presented in Chapter 3. Capacitor design in the up / down state and the design of multiple beam topologies are presented. Capacitor simulations performed using Agilent's ADS Momentum EM field simulator from 1 – 25 GHz for the various states of the beams are presented.

The fabrication process of the multi dimensional MEMS variable capacitors on a silicon substrate is presented in Chapter 4. The release process of the final structures using a CO_2 critical point drying setup and a brief summary of the problems encountered during the fabrication are discussed.

The TRL (thru – reflect – line) calibration technique, used for establishing the reference planes for the 1 – port varactor measurements, is discussed in Chapter 5. The measured and simulated frequency response data is compared in this chapter. With the use of optimization techniques, an equivalent circuit model with the extracted component values for the measured devices is presented. The Q factor of the capacitor extracted in the up and down states from the equivalent circuit model at 1GHz is presented.

An anodic bonding technique used for bonding silicon wafers with glass that can be potentially applied towards the packaging of the MEMS variable capacitors is discussed in Chapter 6. The experimental procedure of the anodic bonding setup and the silicon wafer, glass handling procedure are discussed briefly.

1.3 Contributions

Current issues regarding varactors are; the ability to achieve wide tuning ratios, high tuning range and high Q. The challenge involved herein is to produce high tuning range in a small footprint. The proposed architecture successfully addresses the above factors by incorporating a multi beam topology on a single pedestal. This enables for a high tuning range and high Q operation. The structure is scalable with frequency and can be modified for high frequency applications. Table 1.2 lists pertinent information of a varactor with a 5 – beam topology.

Table 1.2: Typical Performance of the MEMS Varactor Designed with 5 Beams Suspended on a Single Pedestal

5 – Beam Capacitor	Performance
Actuation Voltage	30 – 90V
Tuning Ratio	12:1
Tuning Range	0.5 – 6pF
Size	750µm × 530µm
Q factor	234 (Up state) / 27 (Down State)

CHAPTER 2

BACKGROUND STUDY

2.1 Introduction

MICROELECTROMECHANICAL systems (MEMS) technology offers several advantages for RF systems design. These advantages include the reducing the losses and providing a better linearity [2] when compared with semiconductor based devices. The advantages that are offered by MEMS designs have been implemented in circuit tuning elements (capacitors, inductors), resonators, filters, microphones and switches [3 – 6]. Typical disadvantages associated with an RF MEMS device are the switching speed and packaging the devices [7]. These problems are currently being investigated.

In this chapter, the basic micromachining techniques that include bulk micromachining, surface micromachining and LIGA (lithographe, galvanoformung, abformung) are briefly described. Furthermore, different actuation mechanisms that are typically used in a RF MEMS device are briefly described. Then, a background study of MEMS tunable capacitors for RF applications and a performance based comparison of RF MEMS variable capacitors by other researchers are discussed.

2.2 Micromachining Techniques

Micromachining is the underlying foundation of MEMS fabrication, and a key factor for MEMS processes. In general, micromachining is such a process that selectively etches away parts of the silicon (or other substrate) wafer or adds new structural layers to form the mechanical and electromechanical devices [8 – 11]. The motivation for micromachining the MEMS devices is that it allows miniaturization and parallel processing, which leads to inexpensive fabrication in large quantities. This coupled with thin film deposition and etching techniques is used to create complex structures that can be used to fabricate high performance RF MEMS devices. A brief summary of the typical micromachining techniques used in RF MEMS is discussed below.

2.2.1 Bulk Micromachining

Bulk micromachining is a technique used to realize micromechanical structures within the bulk of a single crystal silicon wafer by selectively etching wafer material [8, 9, and 12]. The selective removal of significant amounts of silicon from a substrate can be used to form three dimensional mechanical structures such as membranes, trench holes, cantilevers, bridges [13]. The crystal planes (54.7° for 100 Si substrate) in Si is used to realize the machined structures, therefore, structures with small footprints are difficult to realize (this is also the case with other substrates).

2.2.2 Surface Micromachining

Unlike bulk micromachining, surface micromachining is suitable for fabricating small structures that is typical of a RF MEMS device. Surface micromachining is a technique where in layers are constructed on the silicon surface [8, 9 and 14]. Therefore, the structures that can be built using surface machining are limited by the lithography tools. To build a movable structure a thin layer (typically 1 – 3µm) is deposited on top of silicon or metal where a mechanical structure is desired and this layer is the sacrificial layer [15]. The structural layer, out of which the free standing structures are made, is then deposited on top of the sacrificial layer. Finally, the given mechanical structure is defined by removing the sacrificial layer and releasing the structure layer. Some of the criteria for choosing the sacrificial and the structural layer is the compatibility of both layers to chemical etchants used in the process, material strength and compatibility with thin film deposition techniques.

2.2.3 LIGA

The LIGA[1] process is a technique for fabrication of three dimensional microstructures with high aspect ratios having heights of several hundred micrometers, which is not possible with thin film deposition techniques [16, 17]. LIGA processing in RF system is typically used in fabricating devices that requires high aspect ratio [8, 18]. The disadvantage of LIGA processing is that it requires expensive fabrication tools.

[1] LIGA is an acronym for lithography, electroforming and micromolding (in German, lithographe, galvanoformung, abformung).

2.3 MEMS Actuation

MEMS actuation can be considered as a trigger to perform the desired function. Some of the common actuation mechanisms include electrostatic, thermal, magnetic and piezoelectric. In the following sections a brief introduction on different actuation mechanisms is described.

2.3.1 Thermal Actuation

Thermal actuation has been extensively employed in MEMS. When a heat signal is provided to the device, a deflection is generated by the different thermal expansion between the two materials that is typically used. The amount of deflection is proportional to the material's thermal expansion coefficients. Typical actuation voltage that utilizes thermal actuation is less than 5V [19]. The disadvantage associated with thermal actuation is that it consumes high power (< 200mW) and has low switching speed (~ 300µs) [19].

2.3.2 Piezoelectric and Magnetic Actuation

Devices that use magnetic actuation typically use a ferromagnetic material such as nickel and it is actuated by applying an electromagnetic effect. Magnetic actuation has low switching speed (~ 300µs) and consumes high power (~ 100mW of power).

Piezoelectric actuation is based on inverse piezoelectric effect. When a voltage is applied to an asymmetric crystal lattice, the material deforms in a certain direction providing a large force in the direction of deformation. Unlike other actuation mechanisms, the switching speed is in the order of 50µs and consumes very little power [19].

2.3.3 Electrostatic Actuation

Electrostatic actuation is one of the most popular actuation mechanisms in MEMS applications. This is due to the simplicity in construction and can be integrated with relative ease to a MMIC circuitry [19]. When a voltage is applied between two plates the electrostatic force between the plates is used to actuate the beams. To a first order of approximation, the Young's modulus of the movable membrane, distance between the plates dictates the amount of voltage required to actuate [19, 20]. Other factors such as squeeze film damping and stresses in the beams also play a major role in

determining the actuation voltage. Typically, electrostatic actuation consumes negligible power and current switching speeds is in the order of 10µs [19]. Table 2.1 shows a comparison of switching speed, actuation voltage, and power consumption of the actuation mechanisms described herein [19].

Table 2.1: Comparison of Switching Speed, Actuation Voltage, and Power Consumption of Various Actuation Mechanisms [19]

Actuation Mechanism	Switching Speed (µs)	Actuation Voltage (V)	Power Consumption (mW)
Thermal	300 – 10000	3 – 5	0 – 200
Magnetic	300 – 1000	3 – 5	0 – 100
Piezoelectric	50 – 500	3 – 20	0
Electrostatic	1 – 200	20 – 80	0

2.4 Study of MEMS Tunable Capacitors for RF Application

RF MEMS tunable capacitors with a wide tuning range, high quality factor, and low operation voltage are being fabricated for application in miniaturized RF / microwave communication systems. Although RF MEMS capacitors do not have high switching speed, they have very low insertion loss due to the low resistivity of metal, high isolation due to the physical separation of the electrodes, and excellent linearity [20]. This low loss feature of the RF MEMS capacitors makes them very attractive for use in modern radar and communications system. A performance based comparison of RF MEMS variable capacitors by various authors is discussed below. Figure 2.1 shows a model of the RF MEMS tunable capacitor.

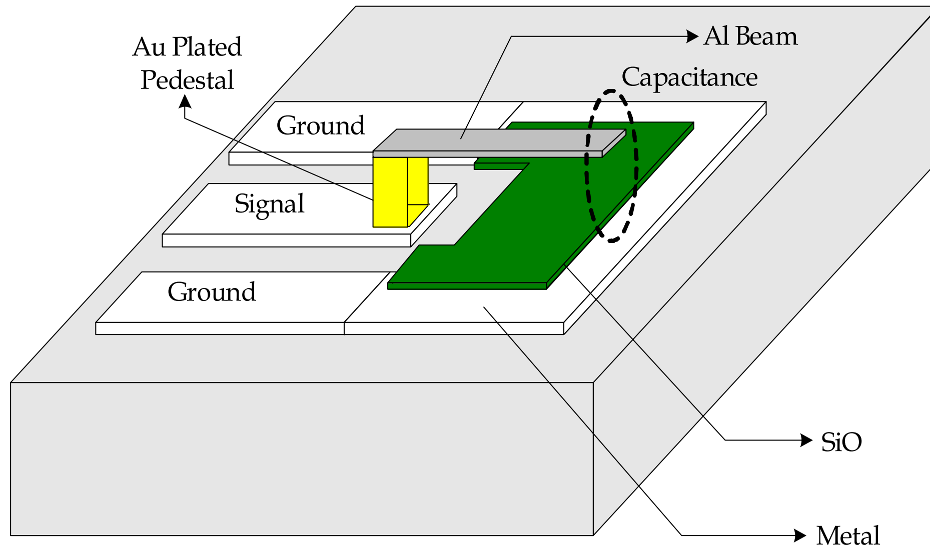

Figure 2.1: RF MEMS Tunable Capacitor with a Single Beam Topology

2.4.1 MEMS Tunable Capacitors Utilizing Thermal Actuation Principle

Huey D. Wu et al. [21] has presented a flip-chip assembly of the MEMS tunable capacitor that utilizes thermal actuation to control the gap of the tunable capacitor from 2 – 0.2µm. A 2-µm air gap is used as the dielectric layer. The capacitance change achieved is 2.6pF for the corresponding gap variation from 2 to 0.2µm. The insertion loss of a polysilicon MEMS capacitor is measured to be -4dB at 40 GHz with a measured resistance of 9.2Ω/□.

Amal Mohamed et al. [22] has presented a MEMS tunable capacitor that utilizes thermal actuation principle. The thermal actuator is designed from a polysilicon layer and a metal layer on top, the deflection produced by this device can move the capacitor plate in ranges of 1µm - 0.2µm with a biased voltage ranges from 1 - 3 volts. The tunable capacitor has high-Q value of 60 at 950MHz.

Zhiping feng et al. [23] has presented a series mounted MEMS tunable capacitor for a CPW configuration utilizing electro thermal actuation for driving the top plate of the parallel plate capacitor. The MEMS structure is bonded on an alumina substrate using flip-chip technology. The air gap is designed to be 2µm. The up – state capacitance increases from 0.3pF to 1.2pF for a maximum bias voltage of 5 volts. The measured Q-factor is 256 at 1GHz for a 0.102pF capacitor and C_{max}/C_{min} ratio of the capacitor is about 4:1.

2.4.2 MEMS Tunable Capacitors Utilizing Zipper Actuation Principle

Gregory et al. [24] has presented a differential multi – fingered MEMS tunable capacitor based on the zipper actuation principle. The capacitor is fabricated in MUMPs polysilicon surface micromachining process. The zero voltage capacitance is 3.1pF and increases by 46% to 4.6pF. The voltage required to achieve the complete tuning is 35V. A CMOS VCO with this capacitor exhibited tuning range of 4.8% with the center frequency of 1.5GHz. The measured Q factor is 6.5 at 1.5GHz.

2.4.3 MEMS Tunable Capacitors Utilizing Electrostatic Actuation Principle

Nils Hoivik et al. [25] has presented a novel design of an electrostatic digitally controllable variable MEMS capacitor constructed using Cronos MUMPS technology and flip-chip technology processing. The capacitor consists of an array of 30 individual plates of equal area, which are connected to the bonding pads by springs of varying widths. This creates a cascading snap-down effect when actuated by electrostatic force. The gap height between the plates is 2μm. The capacitor has a measured Q-factor of 140 at 750MHz, and a tuning ratio of 4:1.

Y.D.Kim et al. [26] has presented a new structure of a RF MEMS voltage tunable capacitor, which have two-movable parallel plates using electrostatic actuation to control the gap of the tunable capacitor. Capacitance of the designed voltage tunable capacitor varies from 1.0pF to 1.48pF as the applied bias voltage is increased from 0.5V to 2.52V.

Jad B. Rizk et al. [27] has presented a digital type RF MEMS switched capacitor where a MEMS shunt bridge is fabricated over a MIM capacitor suitable for 0.5-6 GHz. SiCr is used for the pull down electrode and silicon nitride is used as the dielectric layer. The MEMS bridge height is 1.5μm and the pull down voltage required is 20V. The measured Q-factor is greater than 100 at 1GHz. The capacitance values are ranging from 300fF to 2.25pF rendering varactors with ratios ranging from 3 to 20:1.

Table 2.2: Performance Based Comparison of RF MEMS Variable Capacitors by Various Researchers [21 – 27]

Author	Actuation Mechanism	Actuation Voltage (V)	Capacitance Up State (pF)	Capacitance Down State (pF)	Q-factor
Nils Hoivik et al.	Electrostatic	32	1	4	140 @ 750MHz
Y.D. Kim et al.	Electrostatic	2.52	1	1.48	-
Jad B. rizk et al.	Electrostatic	20	0.12	2.25	90 @ 1GHz
Gregory V. Ionis et al.	Zipper	35	3.2	4.6	6.5 @ 1.5GHz
Huey D.Wu et al.	Thermal	3	0.7	3.5	-
Amal Mohamed et al.	Thermal	3	0.5	2.5	60 @ 950MHz
Zhiping Feng et al.	Thermal	5	0.9	1.7	256 @ 1GHz

2.5 Summary

The basic micromachining techniques and the different actuation mechanisms used for actuating the MEMS devices are briefly described. A background study of MEMS tunable capacitors for RF applications and a performance based comparison of RF MEMS variable capacitors by other researchers are briefly discussed. The choice of actuation mechanism is dependant on the designer. For example, low actuation voltage is achieved if thermal actuation is used; on the contrary the power consumed by the varactor using thermal actuation is considerably high when compared with electrostatic actuation. In this work, electrostatic actuation is preferred over the other actuation mechanisms because of its low power consumption and higher switching speeds.

CHAPTER 3

DESIGN TECHNIQUE

3.1 Introduction

The multi dimensional RF MEMS variable capacitors built in coplanar waveguide (CPW) transmission line configuration have potential advantage at RF and microwave frequencies. The use of CPW transmission lines provides easy integration and a simplified bias scheme since no via holes are required [28, 29]. Furthermore, the lower dispersion loss of components utilizing CPW lines translates directly into a higher quality factor (Q) [9].

The focus of this chapter is the investigation of MEMS variable capacitors in a CPW topology, with multiple beams supported on a single pedestal. The parallel plate capacitor formula is used to calculate the starting values of the capacitor. A full wave EM field simulator (ADS Momentum) is used to accurately predict the behavior of the varactor from 1 – 25GHz.

3.2 Design of Multi-Dimensional RF MEMS Variable Capacitors

A multi dimensional RF MEMS variable capacitor with a three beam topology shown in Figure 3.1 (a single large cantilever beam and two symmetrical cantilever beams) is composed of a bottom electrode and movable metallic membranes (beams) on a single pedestal. The beams are movable in a vertical direction normal to the substrate. The gap between the beams and the bottom electrode can be adjusted electrostatically by applying a tuning voltage, resulting in a change in its capacitance. The electrostatic actuation is preferred over the other actuation mechanisms because of its low power consumption.

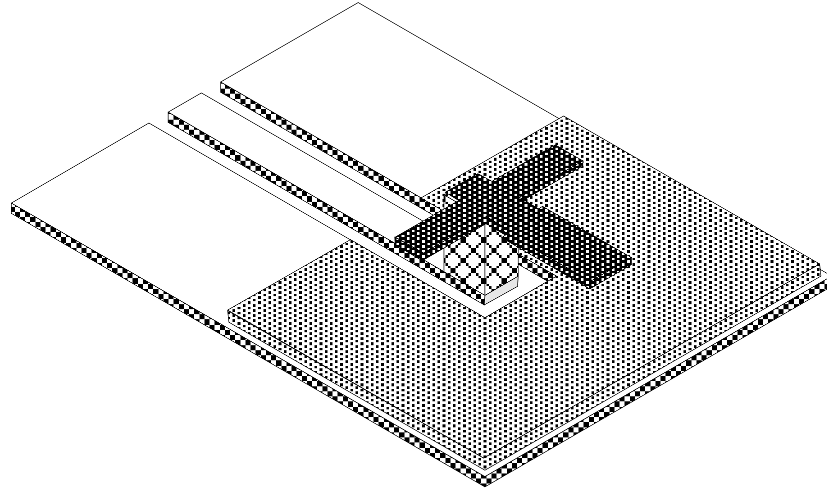

Figure 3.1: A Three Beam Topology MEMS Variable Capacitor

3.2.1 CPW Transmission Line Design

In the designs presented herein, the coplanar waveguide (CPW) transmission line used as the feed line is designed for a 50 Ohm characteristic impedance. Commercial CAD tools such as LINPAR or Line Calc can be used toward this end. In this work, the center conductor width (s) is 120µm and the slot width (w) is 70µm (for a 50Ω line). The ground plane width is chosen to be 500µm.

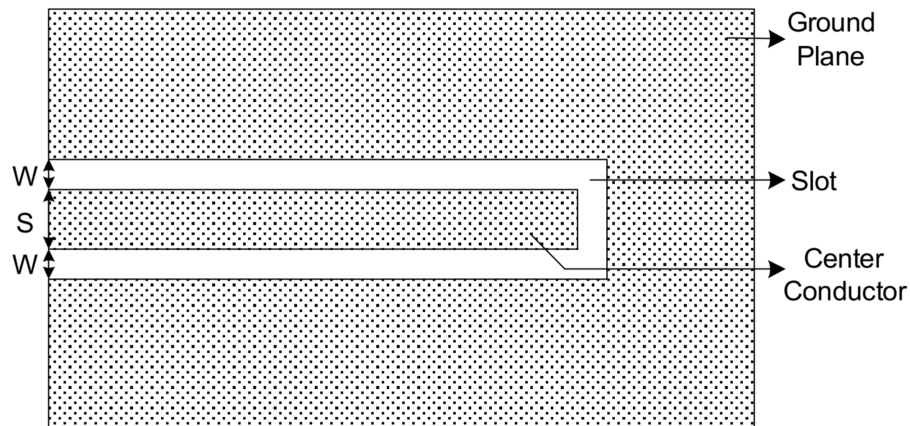

Figure 3.2: Schematic of a 50Ω CPW Transmission Line

3.2.2 TRL Calibration Standards Design

A thru-reflect-line (TRL) calibration technique is used for on-wafer measurements of the capacictors and requires three standards (two 2-port transmission line standards and a reflect standard) [30]. The

length of the thru line is chosen to be 2000μm. The length of the delay line is the total length of the thru line plus the length corresponding to the quarter wave length at a given frequency. Line Calc is used to find the length of the of the delay lines, which are designed at 10, 16 and 26GHz.

3.2.3 Capacitor Design

The capacitors are designed to have a minimum capacitance value in the up state and a high capacitance value in the down state. Figure 3.3 (a) and (b) illustrates a MEMS capacitor with a single beam topology in it's up and down state. The capacitance in the down state can be considered as a metal-insulator-metal capacitor and the value of the capacitance is calculated by the formula given in Equation 3.1 [9, 31 and 32]. This formula is valid to a 1st order approximation as it does not account for the fringing effects.

$$C_{Down} = \frac{\varepsilon_0 \varepsilon_r A}{d} \tag{3.1}$$

Where ε_0 is the electrical permittivity of free space, ε_r is the dielectric constant of silicon monoxide [ε_r – 6], A is the area of the top plate and d is the thickness of the dielectric layer.

The capacitance in the up state can be considered as a parallel plate capacitor with two dielectrics (a) air [ε_{r1} – 1] (b) silicon monoxide [ε_{r2} – 6] and is calculated using the formula given in equation 3.2 [31].

$$C_{Up} = \left[\left[\frac{\varepsilon_0 \varepsilon_{r1} A}{d_1} \right]^{-1} + \left[\frac{\varepsilon_0 \varepsilon_{r2} A}{d_2} \right]^{-1} \right]^{-1} \tag{3.2}$$

Where ε_0 is the electrical permittivity of free space, ε_{r1} is the dielectric constant of air, ε_{r2} is the dielectric constant of silicon monoxide [ε_{r2} – 6], A is the area of the top plate and d_1 is the thickness of air and d_2 is the thickness of silicon monoxide layer. The beam area, beam topology, and up/down capacitance for various beam topologies are listed in Table 3.1 and Table A.1. Figure 3.3 shows the model of the capacitor in its up state (air + SiO as dielectric) and down state (SiO as dielectric). The capacitors are designed to have a high capacitance ratio (C_{Down} / C_{Up}) that is typically greater than 12.

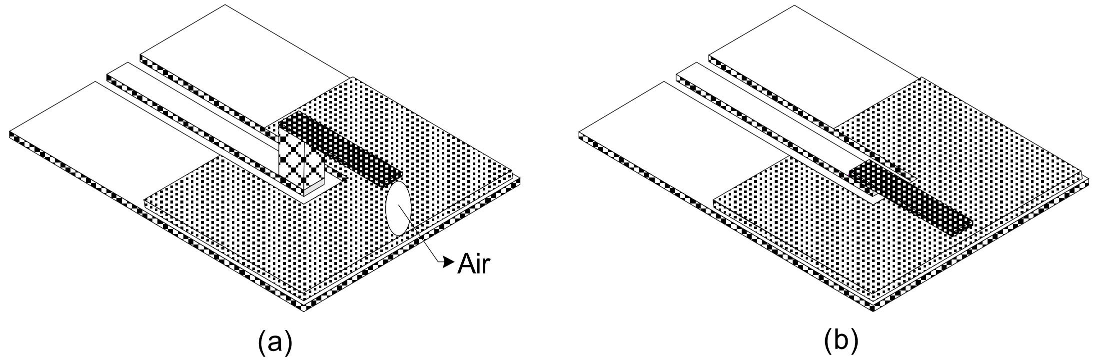

Figure 3.3: A MEMS Capacitor with a Single Beam Topology in its (a) Up – State (b) Down – State

Table 3.1: Physical Characteristics of the Multiple Beam Capacitor Topologies (Beam Topology, Beam Area, Up / Down State Capacitance)

Beam Topology – Structure	Area of the top plate (μm^2)	Up-state capacitance (pF)	Down-state capacitance (pF)
Single Beam – 1c	4.84×10^4	0.161	2.571
Two Beam – 6d	6.45×10^4	0.214	3.426
Two Beam – 8a	1.284×10^5	0.426	6.821
Three Beam – 3c	8.064×10^4	0.286	4.284
Three Beam – 9a	1.769×10^5	0.587	9.398
Four Beam – 5b	9.69×10^4	0.322	5.148
Four Beam – 10d	1.878×10^5	0.624	9.977
Five Beam – 5a	1.448×10^5	0.481	7.692
Five Beam – 10c	2.406×10^5	0.799	12.782
Seven Beam – 11b	2.734×10^5	0.908	14.524

3.2.4 Cantilever Beam Design

Electrostatic actuation is one of the most popular actuation principles used for RF MEMS applications and is used in this design for actuating the beam. Multiple structures varying in beam size, beam dimension, and the number of beams supported on a single structure are designed. For a simple parallel – plate style capacitor electrostatic actuation is created by applying the voltage across

the two plates that are separated by dielectric material. The force generated by applying a voltage can be given by [19, 33]

$$F = \frac{V^2 \partial U}{2 \partial d} \tag{3.3}$$

Where F is the electrostatic force, V is the applying voltage, d is the distance between the two plates, U is the energy stored in the two – plate capacitor, which can be obtained by $CV^2/2$, and C is the capacitance. From the fabrication point of view, the electrostatic actuation principle can be easily integrated on a chip because all fabrication processes are compatible with traditional IC fabrication.

The beam with higher area would actuate at a lesser applied voltage than the beam with a lesser area. The pull down / actuation voltage (V) is given by [9, 19 and 33]

$$V = \left(\frac{2}{3}d\right)\sqrt{\frac{2kd}{3\varepsilon_o a}} \tag{3.4}$$

Where d is the initial beam to electrode distance, ε_0 is the electrical permittivity of free space, a is the area of the capacitor and k is the spring constant of the beam which is given by [19, 33]

$$k = \left(\frac{32bt^3E}{l^3}\right) \tag{3.5}$$

Where b is the beam width, l is the beam length, t is the beam thickness and E is the Young's modulus of the metal used as the beam.

From the above equations it is evident that pull down voltage can vary for a given capacitor area by altering the parameters like length, width and thickness. Considering the physical size of the capacitor and the capacitance value, the above mentioned concept is being used in designing the varactor which can provide a down state capacitance in the pico farad range.

Table 3.2: Calculated Actuation Voltage (Equation 3.4) for the Beams Incorporated in the Capacitor Structures

Beam Topology – Structure	Expected Actuation Voltage (V)						
	Beam 1	Beam 2	Beam 3	Beam 4	Beam 5	Beam 6	Beam 7
Single Beam – 1c	14.25						
Two Beam – 6d	19.12	19.12					
Two Beam – 8a	14.46	14.46					
Three Beam – 3c	14.25	89.27	89.27				
Three Beam – 9a	22.18	17.18	17.18				
Four Beam – 5b	37.62	126.97	126.97	37.62			
Four Beam – 10d	19.11	14.25	14.25	19.11			
Five Beam – 5a	14.25	37.62	89.27	89.27	37.62		
Five Beam – 10c	14.46	19.11	12.63	12.63	19.11		
Seven Beam – 11b	29.52	19.22	89.27	14.25	14.52	89.27	19.22

3.3 Capacitor Simulation

Simulations are performed from 1 – 25 GHz using Agilent's ADS Momentum EM field simulator. The multi-dimensional variable RF MEMS capacitors are simulated on a silicon substrate, 425µm thick with an ε_r –11.7 and a loss tangent of 0.0008. The CPW line of thickness 0.5µm and the beams of thickness 1.5µm are defined in the "strip mode" in Momentum. Silicon monoxide of thickness 1µm with an ε_r – 6 and a loss tangent of 0.0004 are used to define the dielectric layer. Figure 3.4 shows the Momentum simulation setup for a capacitor with a five beam topology.

In a simplified analysis, the capacitance value rises in steps when various beams snap at their respective pull down voltages, as shown in Figure 3.5. The capacitance at lower voltage values is mainly determined by the up state capacitance (0.35 pF). Beam 1 snaps down at 14 volts causing an increase in the capacitance value to 2.8 pF; followed by beams 2 and 5 actuating at 38 volts to give a combined capacitance value of 5.8 pF. Finally beams 3 and 4 actuate at 89 volts to give a final capacitance of 7.7 pF. Practically the capacitance does not increase in steps; the response is more like a smooth slope, with sudden increase in the capacitance value around the pull down voltages for the individual beams. This gradual increase occurs as the beams bend downward with an increase in

the actuation voltage, until their respective actuation voltage is met and the beams (ideally) snap down completely.

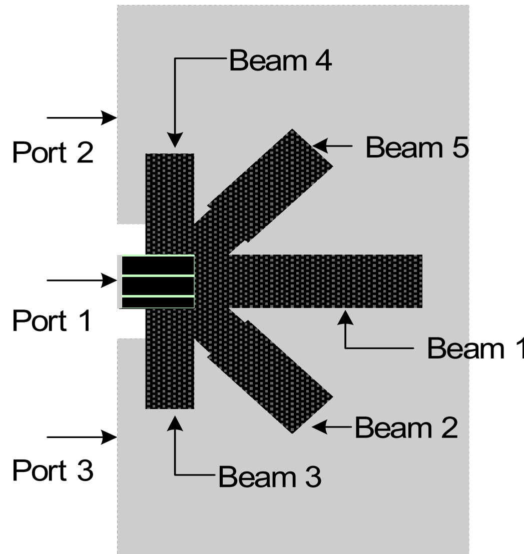

Figure 3.4: Top View of the 5 – Beam Capacitor Topology used in Momentum Simulation

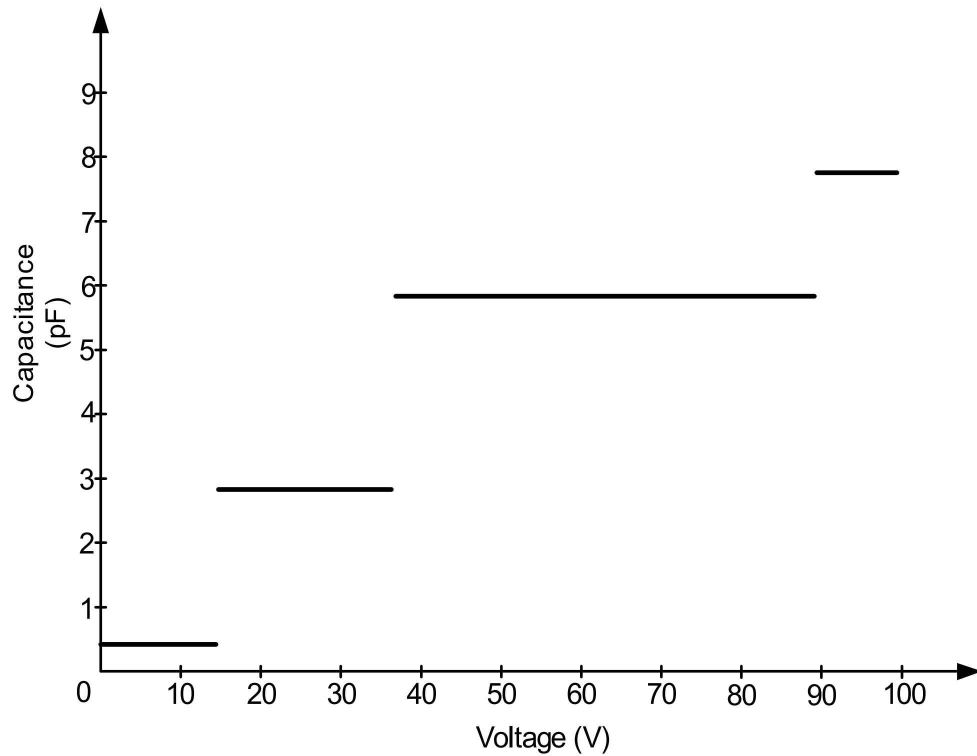

Figure 3.5: Theoretical Response (First Order Approximation) of the Capacitance Value of the Five Beam Topology

For demonstration purposes, simulated results for the 5-beam topology in various actuation states are shown in Figures 3.6 and 3.7. The results of S_{11} (dB) with all beams in the up-state shows the magnitude of S_{11} close to 0dB. When all the beams are down S_{11} decreases to approximately 1dB at 21GHz. The loss is attributed to the parasitics associated with the varactors, which are more prominent at higher frequencies. A series RLC lumped element model is used to extract the parasitics as discussed in Chapter 5.

The process of extracting the capacitance at low frequency (1GHz) from EM simulation is outlined below. The input impedance of the EM simulation can be approximated as that of a simple capacitor. The 50Ω feed line used in the EM simulation is 10μm long. The electrical length of the feed is approximately 0.03° and it is negligible at the frequency of interest (1GHz). Therefore the input impedance is equal to [34]

$$Z_{in} = \frac{1}{j\omega C} \tag{3.6}$$

A circuit level simulation is performed in ADS with EM simulation data as a data block. The capacitance is extracted from the knowledge of Z_{in} (available as measurement block). Rearranging Equation 3.6, the capacitance values are extracted by

$$C = \frac{1}{j\omega Z_{in}} \tag{3.7}$$

Table 3.3 shows a comparison of the extracted capacitance using Equation 3.7 and the calculated capacitance using equation 3.1 and 3.2. The percentage difference for the extracted capacitance in the down states is less than 10% while in the up state the percentage difference is approximately 27%. Figure 3.8 compares the extracted capacitance (Equation 3.7) for a 5 – beam topology at various beam states.

Table 3.3: Comparison of the Theoretical Capacitance Value with the EM Simulated Capacitance Value

Beam States	Theoretical Capacitance Value (pF)	EM Simulated Capacitance Value (pF) (at 1GHz)	% Difference
All beams in the up – state	0.481	0.351	27.027
Beam 1 in down – state with beams 2-5 in the up–state	2.867	2.874	0.2441
Beams 1,2&5 in the down–state with beams 3&4 in the up–state	5.831	6.331	8.574
All beams in the down – state	7.692	8.046	4.602

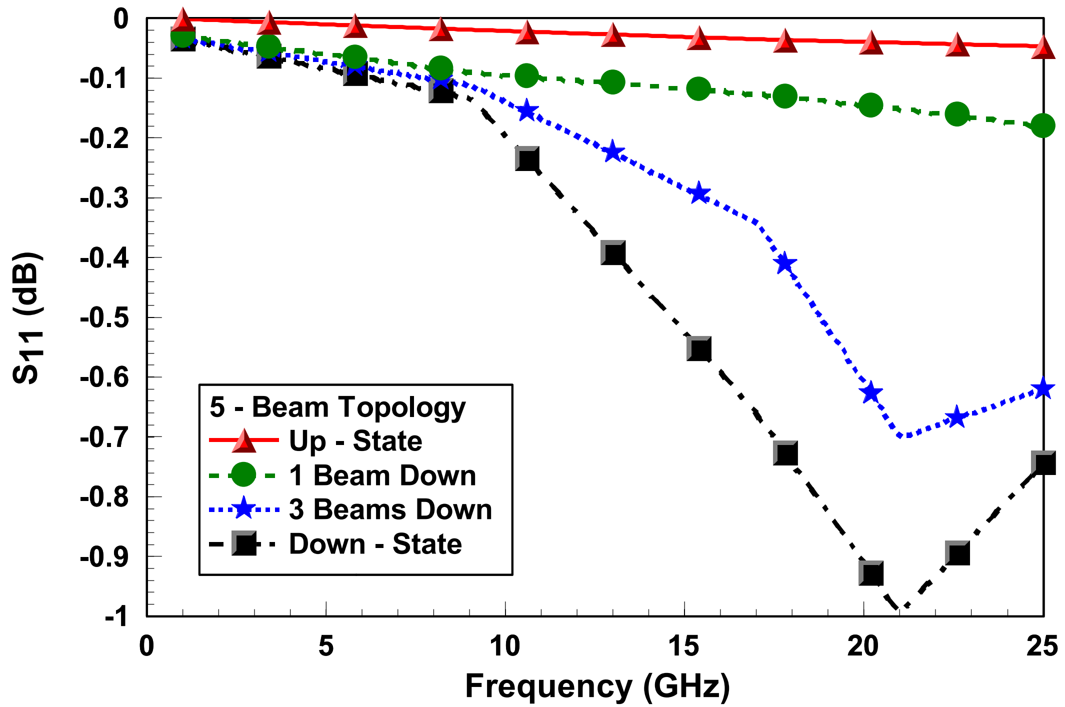

Figure 3.6: EM Simulation Plots of S_{11} Magnitude as a Function of Frequency for a 5 – Beam Topology at Various Beam States

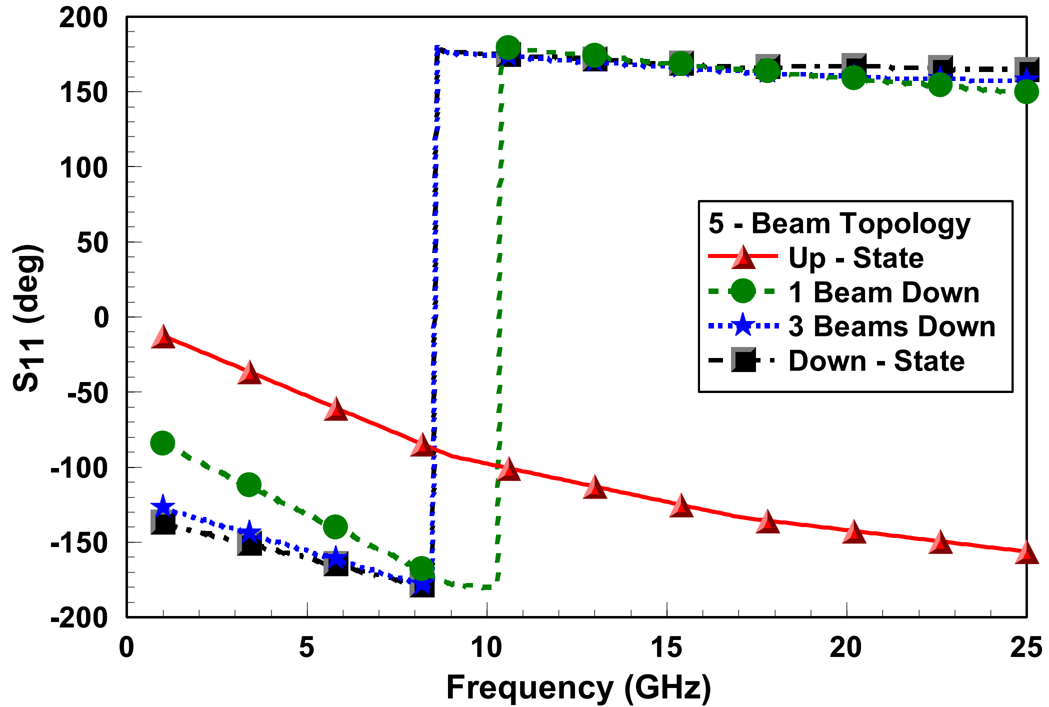

Figure 3.7: EM Simulation Plots of S_{11} Phase as a Function of Frequency for a 5 – Beam Topology at Various Beam States

3.4 Summary

The MEMS variable capacitor in a CPW topology is designed with multiple beams (1 – 7 beams) supported on a single pedestal that utilizes electrostatic actuation principle. Neglecting fringing the theoretical up – state and the down – state capacitance values are calculated using the parallel plate capacitor formula. The theoretical pull down voltage of the varactor is approximately 30 – 90V. A full wave EM simulation is performed from 1 – 25GHz to predict the parasitics associated with the varactor structures. The extracted capacitance from the EM simulations compares favorably with the theoretically used formulae.

CHAPTER 4

FABRICATION TECHNIQUE

4.1 Introduction

The multi dimensional MEMS variable capacitors are fabricated on a silicon substrate (ε_r – 11.7) using surface micromachining techniques. Surface micromachining involves processing above the substrate, mainly using it as a foundation layer on which to build [8, 9]. Material is added to the substrate in the form of layers of thin films on the surface of the substrate. These layers can either be structural layers or act as sacrificial layers. Each additional layer is accompanied by an increasing level of complexity and a resulting difficulty in fabrication [14, 15].

The dielectric materials that are typically used in RF MEMS devices are silicon nitride or silicon monoxide due to high break down voltage (>10^6 volts/cm) and can be fabricated with ease. In this work, a 1µm thick silicon monoxide (ε_r – 6) is used as a dielectric layer for the varactor. The pedestal is comprised of electroplated gold to a thickness of approximately 2.5µm above the metal layer. The movable membrane is comprised of Al and it is preferred due to its high young's modulus which refers to longitudinal strain [35]. Alternatively electroplated gold or nickel beams can also be used which has comparable Young's modulus [36].

The success of the surface micromachining process depends on the ability to successfully remove all of the sacrificial layers to free the structural elements so that they can be actuated. This step is responsible for curtailing the yield (percentage of the devices on a wafer that function properly) and reliability of fabricated MEMS device.

The photoresist (SC 1818) is used as a sacrificial layer and can be removed either using wet or dry etching techniques. When using wet etching method the samples should not be dried in air because the surface tension of the liquid trapped between the beam and the bottom layer will pull the beam down causing it to stick to the bottom layer. Therefore, the sample is released using CO_2

supercritical point drying (CPD). Alternatively, the sacrificial layer can be etched away using an oxygen plasma; the dry etch technique is avoided due to stresses induced in the beams due to the bombardment of the ions.

4.2 Silicon Substrate Characteristics

Silicon has been successful in the microelectronics industry and will continue to be used in areas of microelectronics miniaturization for several reasons:

- Silicon's ability to be deposited in thin films is very amenable to MEMS
- High definition and reproduction of silicon device shapes using photolithography are perfect for high levels of MEMS precision
- Silicon microelectronics circuits are batch fabricated and can be processed to unparalleled purity

The homogeneous crystal structure of silicon gives it the electrical properties needed in microelectronic circuits, and it also has desirable mechanical properties. Silicon forms the same type of crystal structure as diamond, and although the interatomic bonds are much weaker, it is harder than most metals. In addition, it is highly resistant to mechanical stress, having a higher elastic limit than steel in both tension and compression. Single crystal silicon also remains strong under repeated cycles of tension and compression.

4.3 Process Flow

The various steps involved in the fabrication of the RF MEMS variable capacitor are discussed below and the process flow is shown in Figure 4.1. In this design, a 1µm thick silicon monoxide layer is used as the dielectric for the capacitor. The pedestal is gold electroplated to ~2.5µm and aluminum is used for beam formation.

4.3.1 Pattern First Metal (CPW)

Lift – off technique is used in pattering the first metal (CPW) layer. The fabrication of the first metal layer is conducted using standard photolithography used in IC fabrication. A light field mask contained the first-metal CPW lines to be patterned onto the silicon/silicon dioxide sample. This

pattern is transferred using image reversal with Clariant's AZ 5214-E photoresist, commonly used for metal liftoff. The metal is 0.5μm thick comprised of Cr/Ag/Cr/Au (300Å/3200Å/300Å/1200Å) respectively. Cr/Ag/Cr/Au metal layer is typically deposited using thermal evaporation. The initial pressure of the evaporation chamber before evaporation is maintained at 1μT. The evaporation is carried out at a pressure of about 0.2μT. 100Amps of current is used in the low current electrode to evaporate chrome and 240, 300Amps of current in the high current electrode is used to evaporate silver and gold, respectively. The rate of deposition is monitored using a crystal thickness monitor. The profile of the resist pattern, etch and thickness of the metal film are measured using a Tencor Alpha step 200 profilometer.

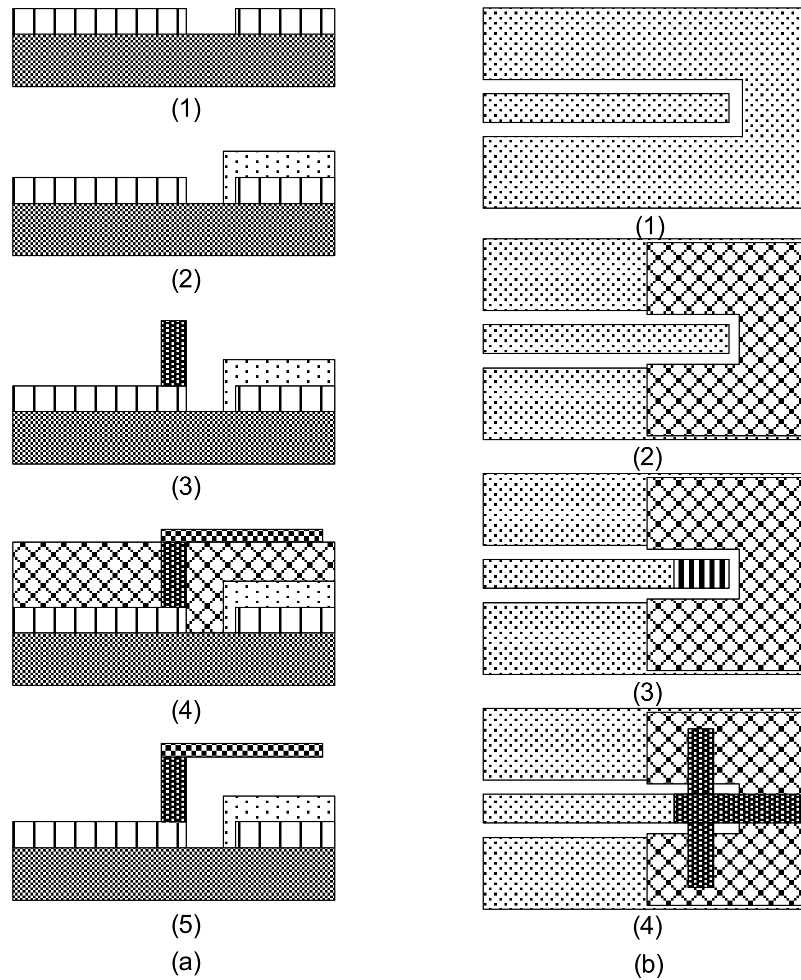

Figure 4.1: Process Flow of the Multi Dimensional RF MEMS Variable Capacitors (a) Cross Sectional View (1) CPW / Bottom Electrode Deposition (2) Dielectric Layer Deposition (3) Pedestal Electroplating (4) Top Electrode Deposition (5) Membrane Release (b) Top View (1) CPW / Bottom Electrode Deposition (2) Dielectric Layer Deposition (3) Pedestal Electroplating (4) Top Electrode Deposition and Membrane Release

4.3.2 Silicon Monoxide Deposition

Silicon monoxide is used as the dielectric layer ($\varepsilon_r - 6$) and is also deposited using thermal evaporation. Chrome is used as the adhesion layer and silicon monoxide of ~1µm is deposited. A current of 310Amps is used to evaporate silicon monoxide.

4.3.3 Pedestal Gold Electroplating

The pedestals are gold electroplated to about 2 µm using a current of ~0.125mA throughout the process to ensure uniformity in the deposition. In this process, Shipley photoresist SC 1818 is used as the sacrificial layer. The pedestal areas are defined by developing the photoresist in MF-319 developer. Technic gold plating solution is used and the entire process is carried out at 50°C. Platinum coated gold wire mesh is used as the positive electrode. The experimental setup is shown in Figure 4.2.

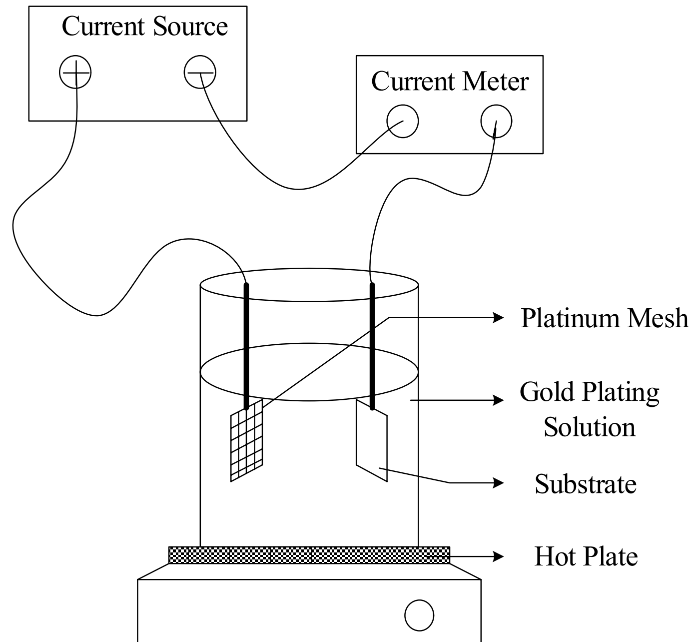

Figure 4.2: Experimental Setup for Gold Electroplating

4.3.4 Beam Formation and Final Release

The top electrode (beam) of the MEMS capacitor is deposited using an e-beam evaporator. Cr (300 Å) and Al (1.5µm) are evaporated onto the sample. In this process, Shipley photoresist SC 1818 is used to define the beam and the unwanted Al and Cr layer is etched away using Cr and Au etchants.

4.3.5 Release process

The release process is done by placing the sample in acetone for approximately 15 minutes for removing the sacrificial photoresist (SC 1818), then placing it in another clean beaker of resist remover 1165 at 70°C for 20 minutes to ensure the removal of any residual photoresist between the top electrode and the dielectric layer.

A CO_2 critical point drying (CPD) setup is used for the final release process. The released samples are placed in high purity methanol before placing it inside the CPD setup. A dry run without the sample is performed and several test runs with carbon dioxide filling and methanol flushing are performed to ensure complete removal of methanol from the chamber. Finally the sample is placed in the chamber and the process is repeated. The chamber pressure is increased from 800psi to 1350psi and the temperature is brought above super critical temperature of carbon dioxide (~32°C). Finally the carbon dioxide is vented out of the chamber maintaining the chamber roughly constant and the pressure is lowered back to the atmospheric pressure without condensation.

4.4 Problems in Fabrication Technique

4.4.1 Shorting of Electrodes

When depositing the insulating dielectric layer on the CPW conductors it is important to completely cover the metallization in order to avoid shorting during actuation of the MEMS device. It is especially critical near the edges of the conductors, where uneven edges might occur during the metal deposition and/or lift-off process.

In this work, the initial designs are attempted using a dielectric thickness of 0.2µm, with a metal thickness of 1µm. However, this is found to result in significant current draw (partial shorting) during actuation and a burning effect was seen at the edges of the bottom electrode and the SiO insulator interface (Figure 4.3). To overcome this problem the insulator thickness is increased to 1µm. One effect of this design change is to decrease the effective capacitances by a factor of ~5.

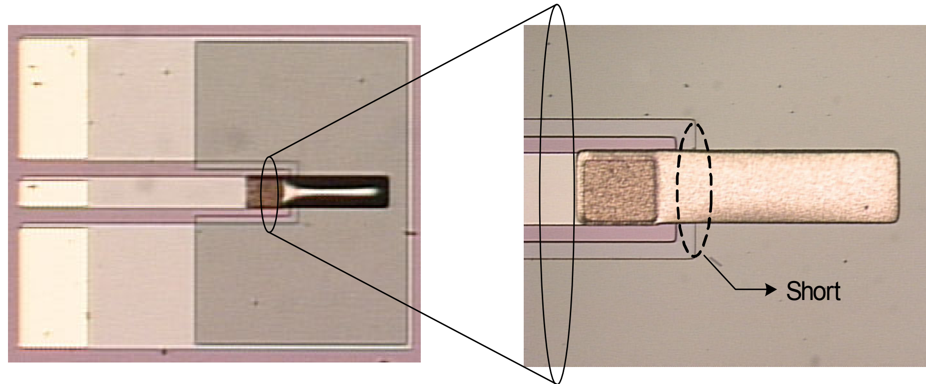

Figure 4.3: Partial Shorting (Indicated by Dotted Line) at the Interface of Edge of the Bottom Electrode and the Dielectric Layer

4.4.2 Membrane Release Failure

The photoresist underneath the beam layer is supposed to be completely removed after the final release process. But, few structures would not actuate even at an actuation voltage of 100V because of the presence of photoresist underneath the top electrode. This actuation problem is attributed to the width of the beam (~150µm) and associated difficulties in removing all the underlying resist. Possible ways of avoiding this problem are

- Having holes in the beams
- Increasing the distance between the dielectric layer and the top electrode

These approaches facilitate the acetone and the resist remover in attacking the photoresist.

4.4.3 Stiction

During actuation a few structures adhered to the dielectric layer and did not return to the original state after removing the voltage supply. Adhesion of the top electrode to the dielectric layer is one of the main difficulties in MEMS process. This phenomenon is called stiction. Stiction arises if the adhesive force between the contacted areas is larger than the elastic restoration force of the deformed top electrode. Hence the structure remains stuck to the substrate even if completely dried.

4.5 Summary

The multi dimensional MEMS variable capacitors are fabricated on a 425µm thick silicon substrate with 1µm thick silicon monoxide as the dielectric layer using surface micromachining techniques. The movable metallic beam that is comprised of Al is suspended 2µm above the metal layer on an electroplated gold pedestal. Photoresist is used as the sacrificial layer and the beams are released using conventional CO_2 supercritical point drying method. It is necessary to exercise caution when fabricating movable structures due to various stresses that can be inadvertently induced in the structure when processing. Some of the problems encountered while processing was shorting of the cantilever to the ground pads especially at the ground-dielectric interface due to non-conformal nature of the evaporated SiO. This problem is overcome by increasing the dielectric thickness.

CHAPTER 5

MEASUREMENTS AND MODELING

5.1 Introduction

Accurate measurement data is essential for developing reliable equivalent circuit models. The quality of the measurement depends on the calibration method used. The Thru – Reflect – Line (TRL) technique is the most accurate calibration method for broad band on-wafer measurements. A full 2 – port TRL is calibration is performed from 1 – 25GHz using NIST's Multical software with the reference plane at the edge of the pedestal. A Wiltron 360B Vector Network Analyzer (VNA) is used to measure the 1 – port S – parameter data. Measurements are performed in the up state (i.e., 0V bias) and in increments of 2V until all the beams are actuated.

A series RLC lumped equivalent circuit is used to model the varactor. The element values of the lumped model are extracted by optimizing the measurement results with the equivalent circuit model. A good agreement between the measurement results and the lumped model is obtained. Furthermore, the measurement result is used to extract the unloaded Q of the varactor in the up and in the down state. The unloaded Q that is extracted at 1GHz in the up and down state is 234 and 27, respectively. The low Q factor in the down state is primarily attributed to the lossy SiO dielectric.

5.2 TRL Calibration Technique

The TRL technique requires a through-line (Through), a transmission-line offset (Line), and highly reflecting impedances (Reflects) as standards [30]. As TRL is a 'self-calibrating' technique, the exact electrical characteristics of the standards need not be known a priori. The number of delay lines used in the calibration procedure is determined by the frequency range over which the calibrations are performed. The measurement uncertainties increases significantly when the insertion phase of the delay line nears 0° or an integer multiple of 180°, therefore, 18° to 162° is the nominal bandwidth for a delay line.

A limitation of the TRL technique is the limited bandwidth of Line standards. For broadband measurements, several Line standards may be required. At low frequencies, Line standards can become inconveniently long. The finite length of the delay line in the TRL method may prohibit the performance of the calibration at low frequencies.

The reference impedance for all measurements in this work is 50Ω. The length of the thru line was chosen to be 2000µm. The length of the delay line is the total length of the thru line plus the length corresponding to the quarter wave length at a given frequency. Line Calc was used to find the length of the of the delay lines which were designed at 10, 16 and 26GHz. The calibration standards for the TRL calibration technique are shown in Figure 5.1.

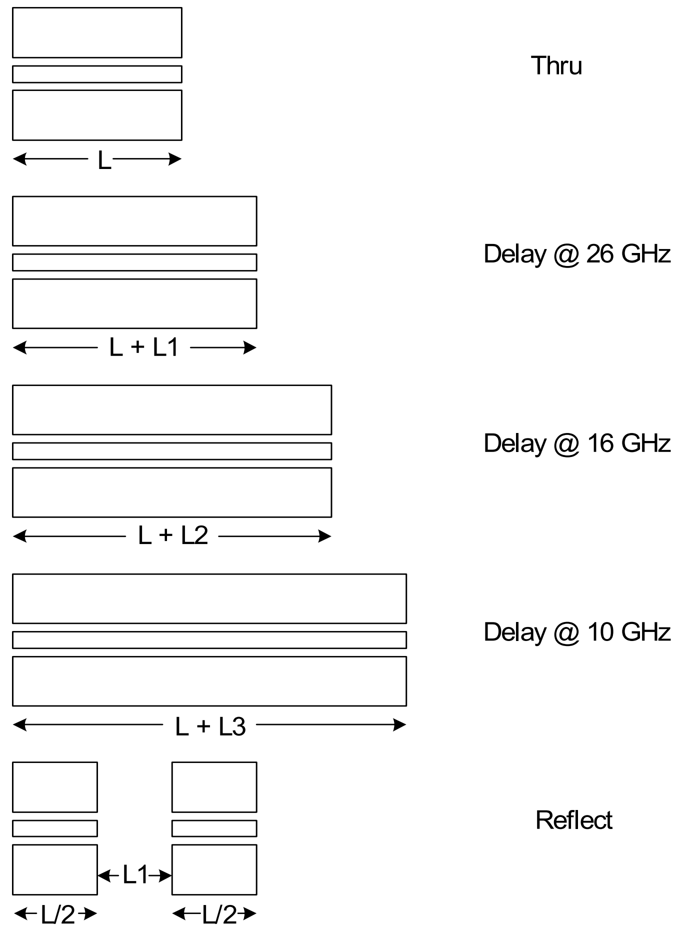

Figure 5.1: Calibration Standards for the TRL Calibration Technique

The TRL calibration must be verified before taking the measurements on the actual device. Since the reference plane is ideally located at the center of the thru line, the insertion loss and the insertion phase of the thru line after calibration should be equal to 0dB and 0°, respectively, over the entire frequency range. The insertion loss and the insertion phase of the delay line after calibration should decrease monotonically. The measured effective dielectric constant and the characteristic impedance of the CPW line should have a minimal variation over the entire frequency range. Table 5.1 lists the set of general guidelines for calibration verification and Figure 5.2 through Figure 5.6 shows the results of the TRL calibration.

Table 5.1: General Guidelines to Verify the Accuracy of Calibration Procedure

TRL Standard	Measured data	Acceptable value
Thru	Magnitude of S_{21}, S_{12}	Close to 0dB over the entire frequency range (Figure 5.2)
Thru	Phase of S_{21}, S_{12}	Close to 0 degrees over the entire frequency range (Figure 5.3)
Thru	Magnitude of S_{11}, S_{22}	Less than -40dB over the entire frequency range (Figure 5.4)
Delay Line	Magnitude of S_{11}, S_{22}	Less than -40dB over the entire frequency range (Figure 5.5)
Reflect	Magnitude of S_{11}, S_{22}	Close to 0dB over the entire frequency range (Figure 5.6)

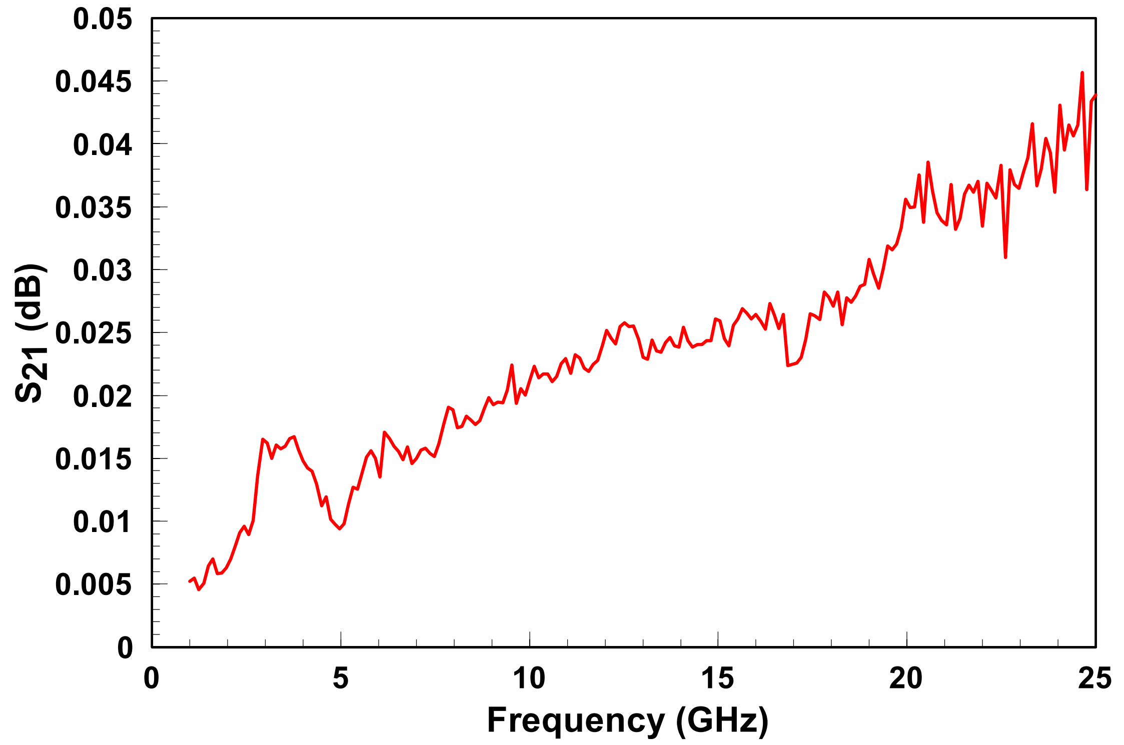

Figure 5.2: Magnitude of S_{21} for the Thru

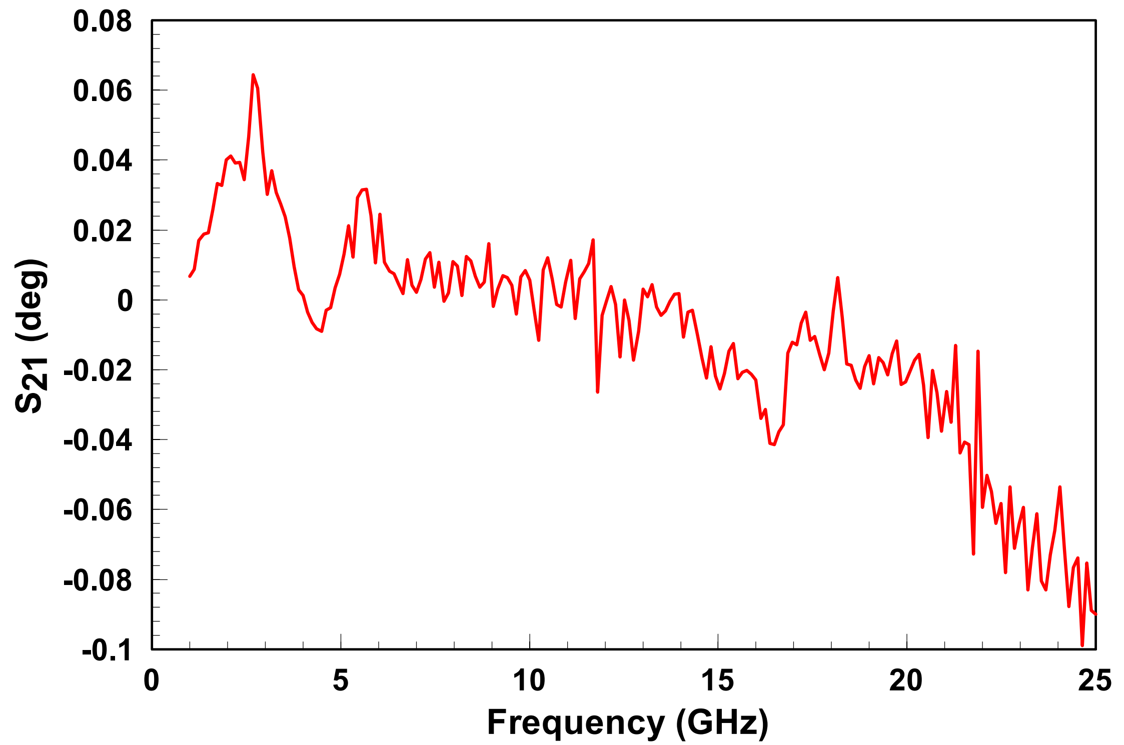

Figure 5.3: Phase of S_{21} for the Thru

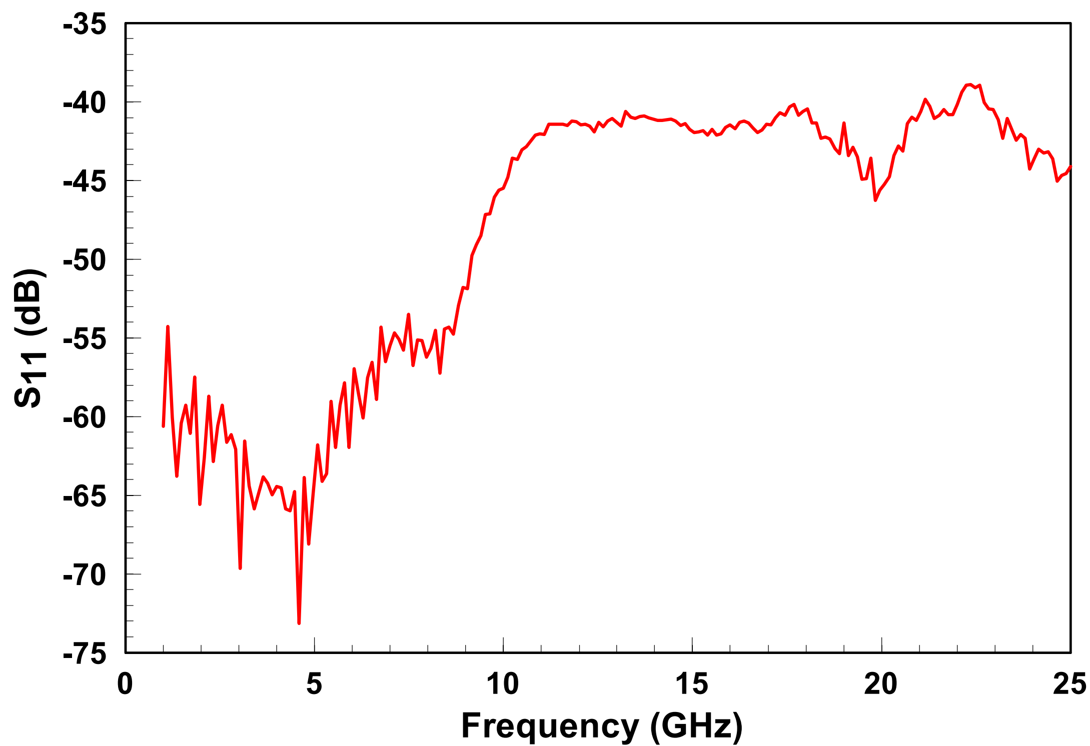

Figure 5.4: Magnitude of S_{11} for the Thru

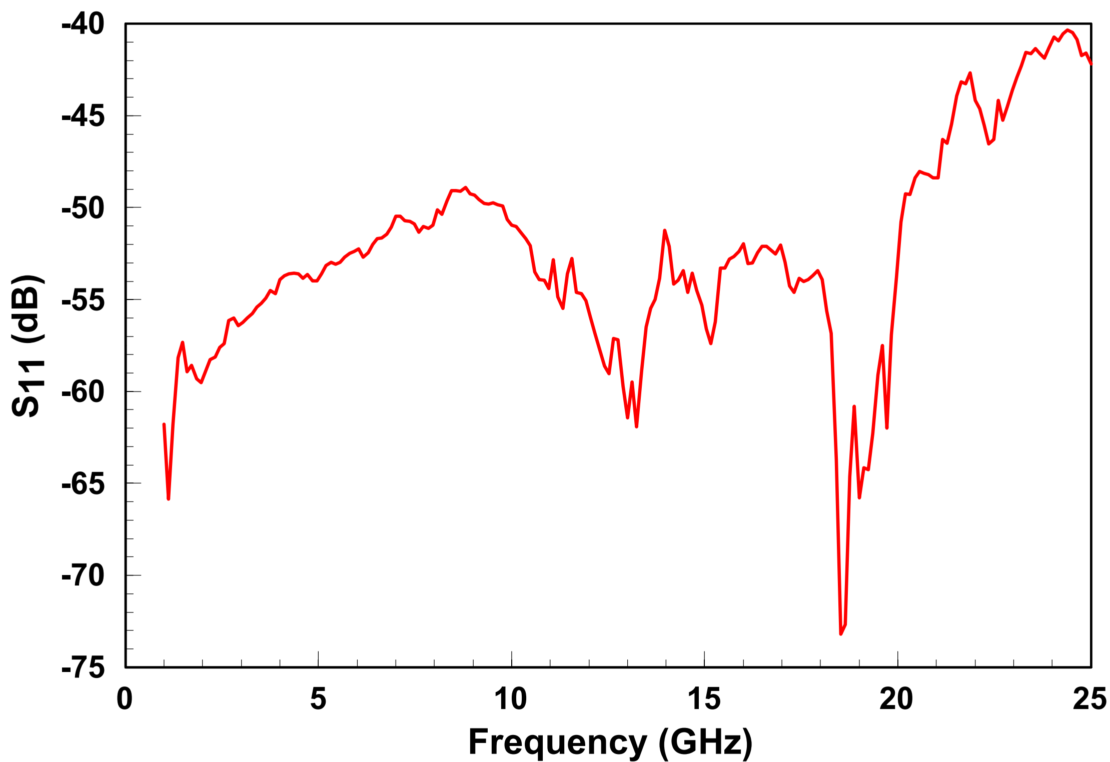

Figure 5.5: Magnitude of S_{11} for the Delay Line

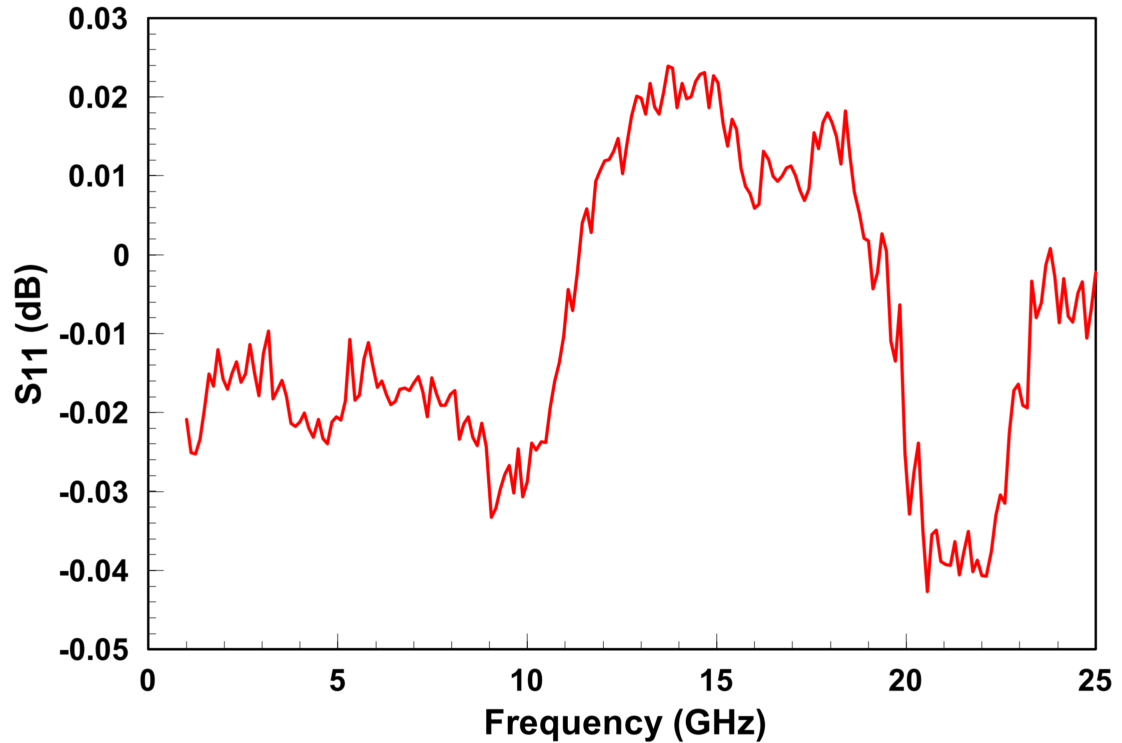

Figure 5.6: Magnitude of S_{11} for the Reflect

5.3 Measurement Setup

Measurements were performed using a Wiltron model 360B vector network analyzer and 150µm pitch probes on a Karl Suss probe station. A bias tee from Picosecond Labs rated at 100V is used for providing DC bias to the DUT. The schematic of the setup is shown in Figure 5.7. An on-wafer TRL calibration was performed using NIST's Multical calibration software and the calibrated S-parameter data was captured from 1 to 25GHz. The S-parameter data was taken in increments of two volts from 0 to 90 volts. A 10KΩ resistor is used in the current path to suppress any potential current spikes in the circuit (e.g. due to capacitive shorting).

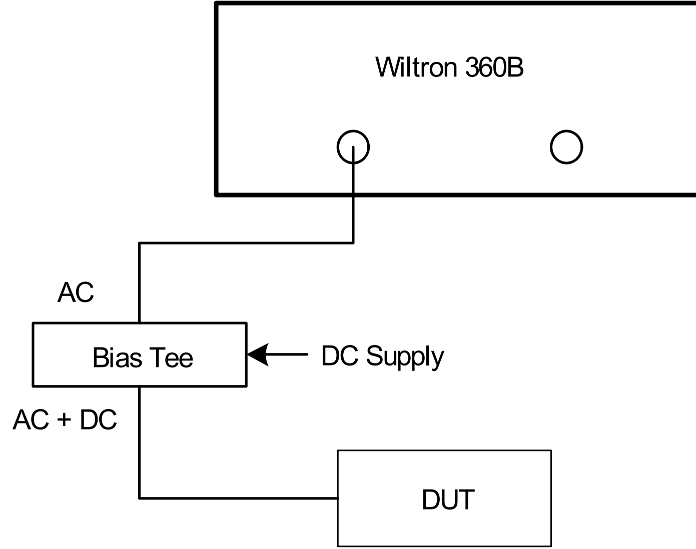

Figure 5.7: Measurement Setup used for Measuring the One – port MEMS Variable Capacitors

5.4 Equivalent Circuit Modeling

Equivalent circuit modeling of the MEMS varactor measured herein provides information regarding the parasitics. The varactor can be visualized as a series combination of resistance (R), inductance (L) and capacitance (C) to ground. Figure 5.8 represents the lumped element equivalent circuit model for the MEMS variable capacitor. The resistance (R) represents the dielectric loss of the capacitor and conductor losses in the metal lines. The resistance is modeled as frequency dependant variable given by Equation 5.1 [37]. In this equation, A represents the DC resistance of the membrane and B is used to fit the frequency-dependent loss.

$$R = A + \left(B\sqrt{f}\right) \tag{5.1}$$

where, f represents the frequency in Hz.

The current crowding and propagation delay in the membrane is modeled as an inductor (L). The capacitance C represents the capacitance of the MEMS variable capacitor that is designed using Equation 3.1 and 3.2.

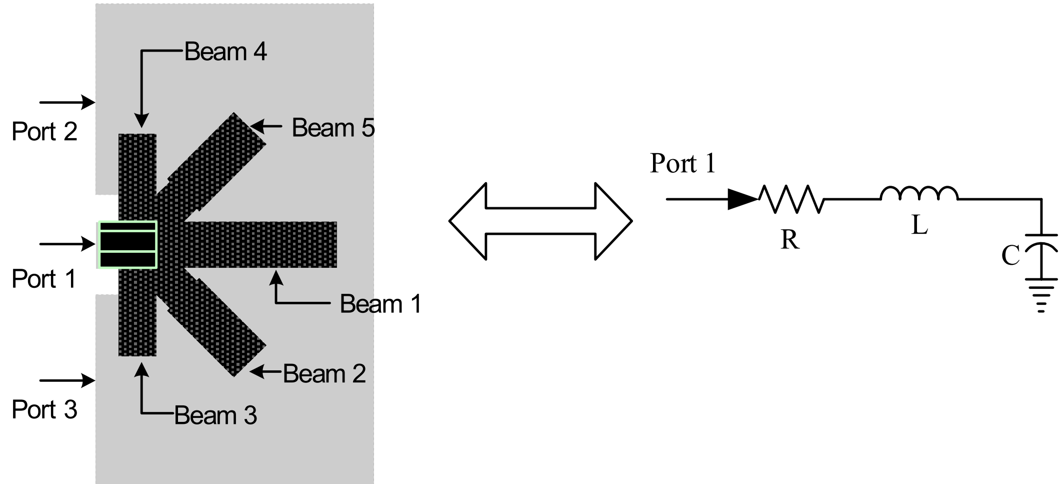

Figure 5.8: Lumped Element Equivalent Circuit Model for the One – Port MEMS Variable Capacitor (5 – Beam Topology)

The process of extracting the element values in the model is achieved by using circuit optimization. The magnitude and angle of S_{11} of the model is optimized with the measured data from 1 – 25GHz. The capacitor C in the model is allowed to vary within 10% of the designed value because the theoretical value does not account for fringing. The inductance L, and the variables A and B in equation 5.1 are extracted using optimization. Table 5.2 compares the extracted capacitance value with the theoretical value.

Table 5.2: Comparison of the Theoretical Value of the Capacitor (Equation 3.1 and 3.2) with the Extracted Capacitance Value in the Up and Down State (5 – Beam Topology)

Capacitance (pF)	Up – state	Down – state
Theoretical	0.48	7.69
Extracted @ 1GHz	0.52	6.00

From Table 5.2, the increase in the up – state capacitance for the extracted value is due to the fringing capacitance and it is close to the calculated value. The down – state capacitance value shows a discrepancy of 1.69pF. This is attributed to two reasons (1) the fabricated beams are not perfectly flat and hence the beams in the down – state are not in complete contact with the dielectric layer resulting in the decrease in the capacitance value, and (2) beams 3 and 4 of Figure 5.7 did not completely actuate for a maximum bias of 94 volts. (The bias – T used in the measurement setup was rated for 100 volts and to keep some safety margin the measurements were limited to a maximum of

94 volts.) The capacitance contributed by beams 3 and 4 is ~1.71pF and adding this to the down – state extracted capacitance increases the total to 7.713pF, which compares favorably to the theoretical value. The curvature in the beams can be potentially avoided by annealing the sample before releasing or by electroplating the beams instead of evaporating. The element values of the model for a 5 beam topology are illustrated in Table 5.3.

Table 5.3: Lumped Element Equivalent Circuit Component Values for the One Port MEMS Variable Capacitor in the Up – State and Down – State

Element Values	Up – State	Down – State
Capacitance (pF)	0.52	6.00
Inductance (nH)	0.05	0.05
Resistance (Ω) @ 1GHz	0.77	0.80

A comparison of the theoretical and the measured capacitance as a function of voltage is shown in Figure 5.9. The theoretical capacitance values are indicated by straight dotted lines. Beam 1 is expected to snap down around 15V and the snapping is observed around 30V with a linear increase in the capacitance value. Beams 2 and 5 (symmetrical beams) are expected to snap around 40V; instead the snapping occurs around 75V. Finally Beams 3 and 4 (symmetrical beams) are expected to snap around 90V and it is observed that the beams appear not to snap down. The applied voltage is limited to 94V as the bias tee used in the measurement setup is rated to a maximum of 100V.

Figure 5.10 and Figure 5.11 compare the magnitude and phase of S_{11} between the measurement results and the modeled data for the 5 – beam capacitor in the up state. Similarly, the magnitude and the phase response of S_{11} in the down state are shown in Figure 5.12 and Figure 5.13, respectively. From the figures it is seen that the agreement between the measurement results and the model is good. The comparisons of magnitude and phase between measurement and modeled data for other beam topologies are shown in Appendix B through Appendix D.

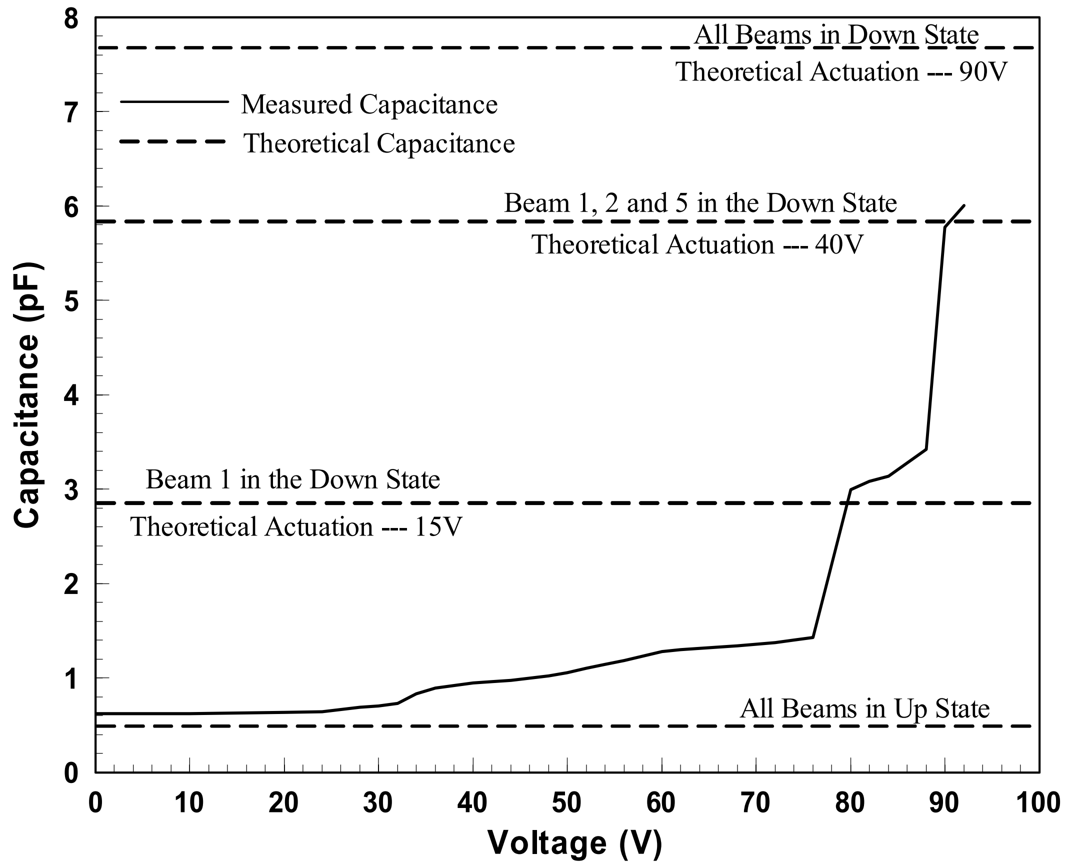

Figure 5.9: Comparison of Measured and Theoretical Capacitance as a Function of Voltage (5 – Beam Topology)

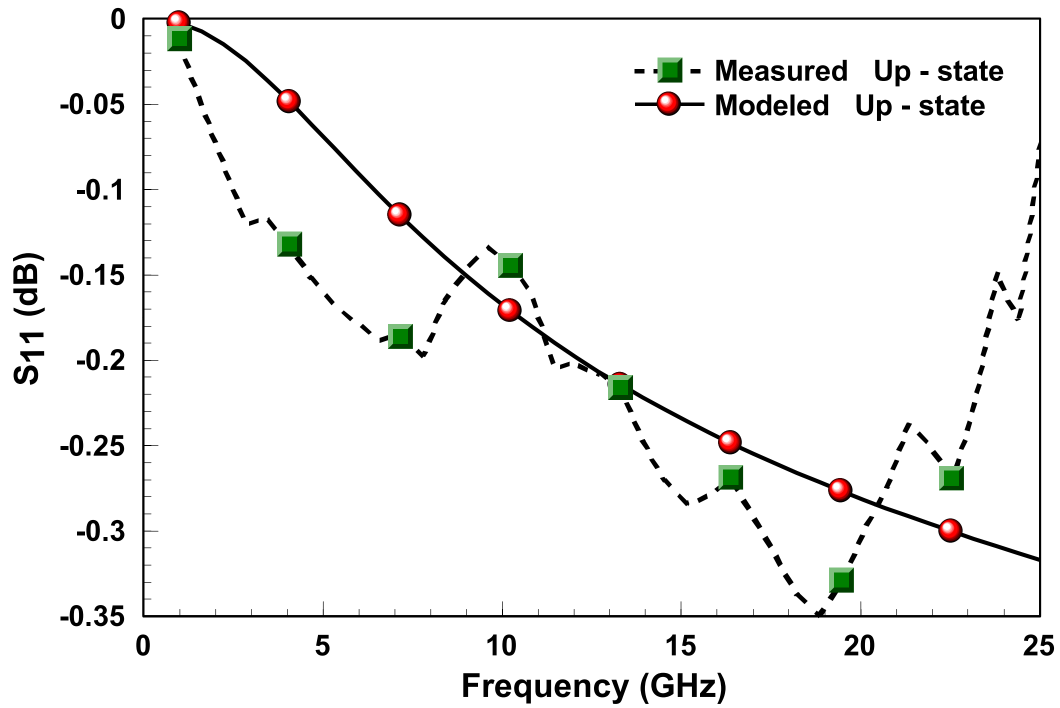

Figure 5.10: Comparison between the S_{11} Magnitude of the Measured and the Modeled Capacitor (5 – Beam Topology) in the Up – State

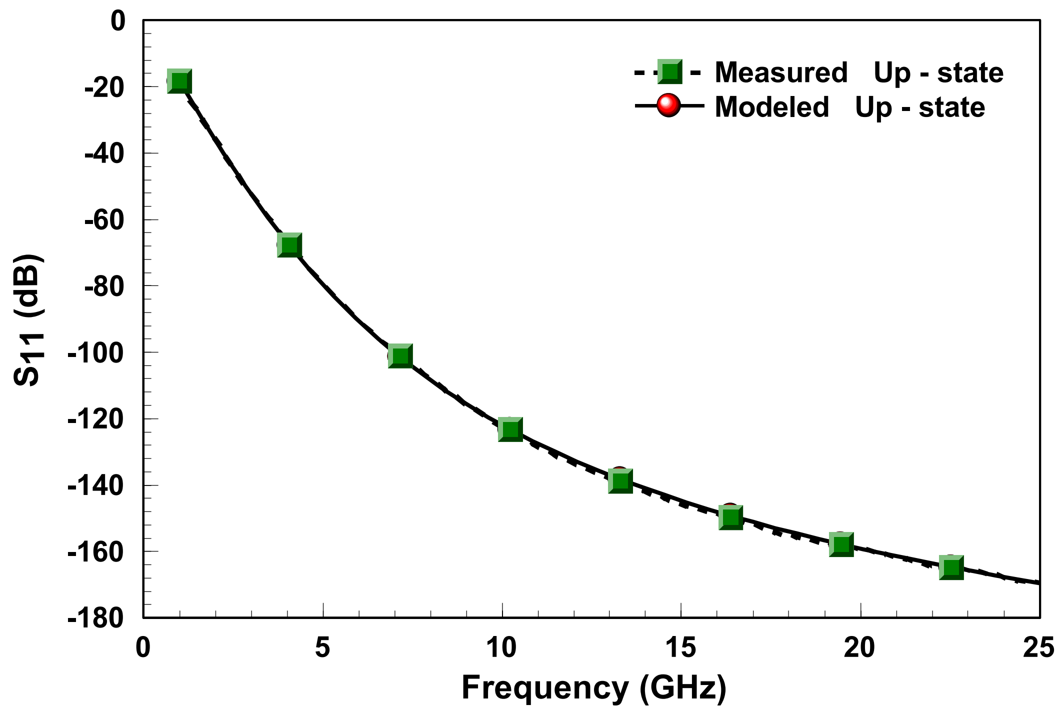

Figure 5.11: Comparison between the S_{11} Phase of the Measured and the Modeled Capacitor (5 – Beam Topology) in the Up – State

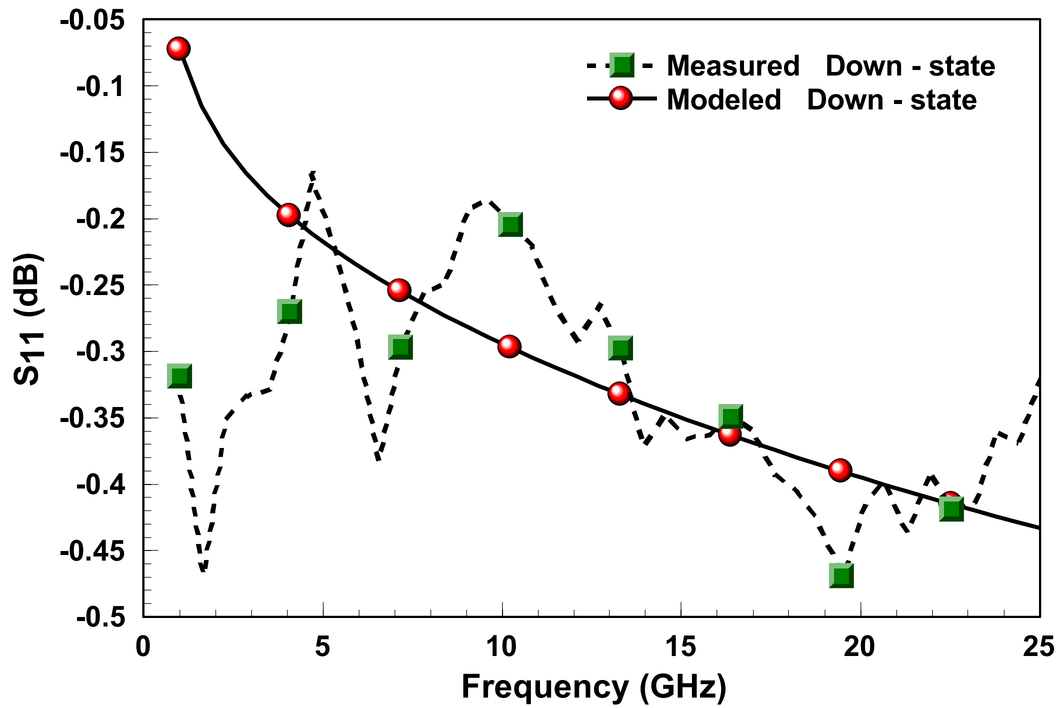

Figure 5.12: Comparison between the S_{11} Magnitude of the Measured and the Modeled Capacitor (5 – Beam Topology) in the Down – State

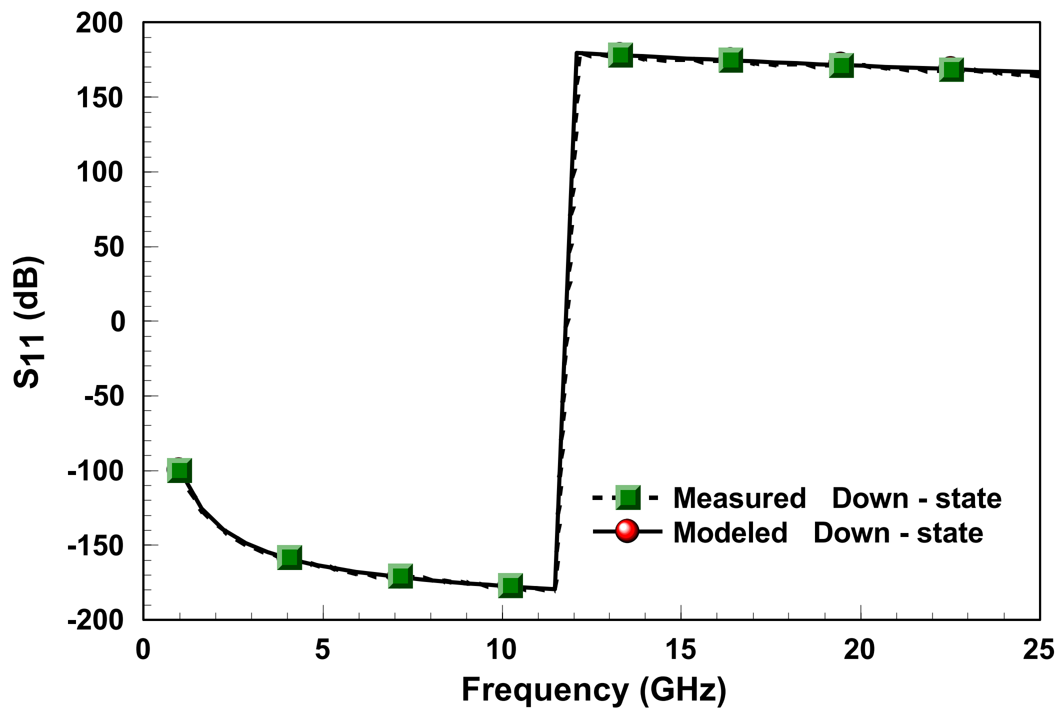

Figure 5.13: Comparison between the S_{11} Phase of the Measured and the Modeled Capacitor (5 – Beam Topology) in the Down – State

5.5 Quality Factor Measurements

The quality factor Q of a device is a measure of loss of RF signal through the circuit. A high Q device implies low loss and vice – versa. The 1 port S – parameter data is used to extract the unloaded Q of the MEMS varactor. The Z – parameter block in the ADS circuit simulator is used to provide the 1 – port Z parameter information (Z_{11} in this case). Using Equation 5.2 [19], the unloaded Q factor (Q_{meas}) is extracted from the measured data. Similarly, the Z_{11} of the equivalent circuit model (Figure 5.8) is used to extract the unloaded Q factor (Q_{model}). Figure 5.14 and Figure 5.15 shows a comparison between Q_{meas} and Q_{model} in the up and down states, respectively. Figure 5.15 is curtailed to 11GHz as the capacitor nears its resonant frequency. Table 5.4 list the extracted Q factor at 1GHz using the measurement data and the model. It is seen that the Q_{meas} in the down state is low (~ 27). This is due to the lossy dielectric SiO layer used in the varactor.

$$Q = -\frac{\text{Im}[Z_{11}]}{\text{Re}[Z_{11}]} \tag{5.2}$$

Table 5.4: Extracted Q Factor at 1GHz Using the Measurement Data and the Model

Beam State	Extracted Q factor	
	Measurement Data	Model
Up – State	243	401
Down – State	27	53

The rate of deposition of SiO layer and the temperature has a strong correlation with the dielectric loss tangent [38]. The authors in [38] show that the loss factor is reduced from 0.007 to 0.003 if the rate is reduced from 6Å/s to 2Å/s for a 1µm thick film (similar to the thickness used in this work). In this work, the SiO coated wafer is subjected to a high thermal budget which changes the properties of the film. A more stable nitride dielectric can be used instead of SiO dielectric to reduce the dielectric loss. A performance based comparison of RF MEMS variable capacitor with other researchers is shown in Table 5.5. Considering the large capacitance value of the designed capacitor, the measured unloaded Q factor is acceptable.

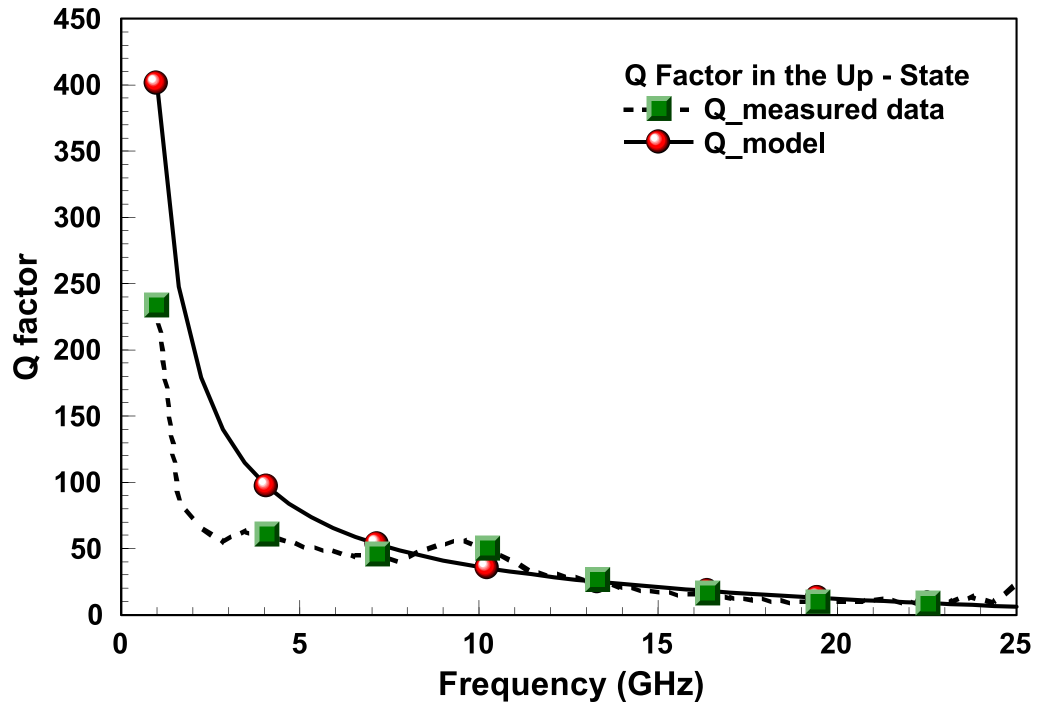

Figure 5.14: Comparison between the Q – Factor of the Measured and the Modeled Capacitor (5 – Beam Topology – Figure 5.8) in the Up – State

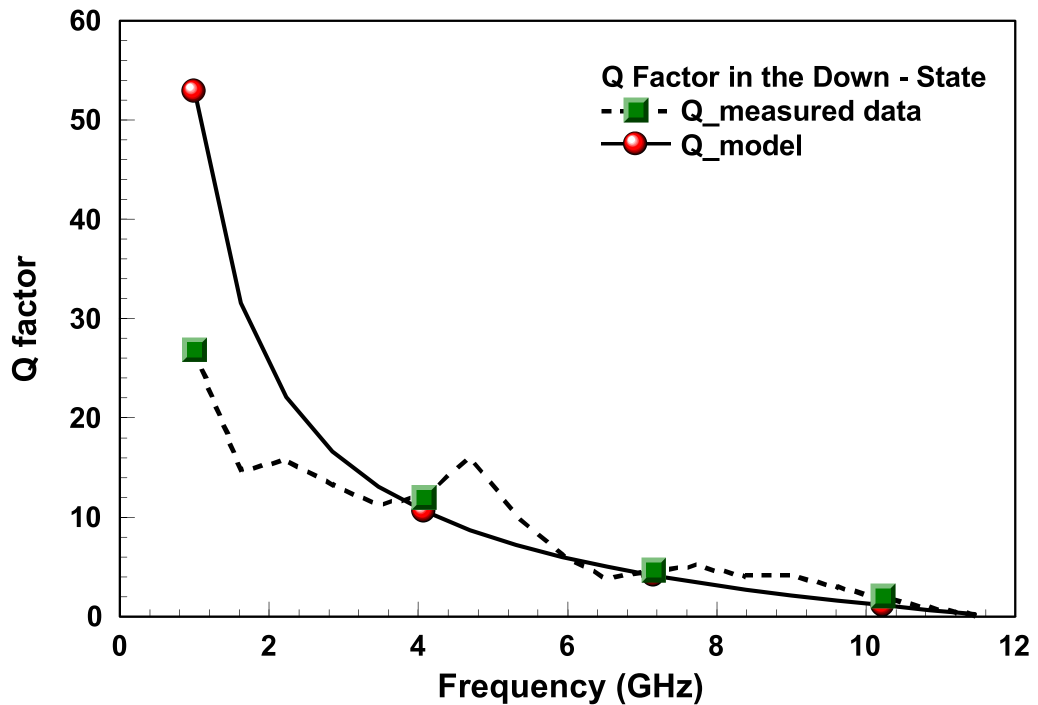

Figure 5.15: Comparison between the Q – Factor of the Measured and the Modeled Capacitor (5 – Beam Topology – Figure 5.8) in the Down – State

Table 5.5: Performance Based Comparison of RF MEMS Variable Capacitors with Other Researchers [21 – 27]

Authors	Actuation Mechanism	Actuation Voltage (V)	Capacitance Down – State (pF)	Q-factor
Amal Mohamed et al.	Thermal	3	2.5	60 @ 950MHz
Zhiping Feng et al.	Thermal	5	1.7	256 @ 1GHz
Gregory V. Ionis et al.	Zipper	35	4.6	6.5 @ 1.5GHz
Nils Hoivik et al.	Electrostatic	32	4	140 @ 750MHz
Jad B. rizk et al.	Electrostatic	20	2.25	90 @ 1GHz
Hari Kannan et al.	Electrostatic	30	6.00	27 @ 1GHz

5.6 Summary

The MEMS varactor designed herein is measured using Wiltron 360B VNA from 1 – 25GHz. NIST's Multical TRL calibration routine is used in the calibration. The reference plane is established at the edge of the pedestal. The S-parameter data is measured from 0V (up state) to the pull in voltage of all the beams (down state). The measured actuation voltage of the beams is approximately 30 – 90V. Furthermore, the measured capacitance ratio is approximately 12:1 with capacitance value of 6pF in the down state and 0.5pF in the up state.

A series RLC lumped equivalent circuit is used to model the varactor. The element values of the model are extracted by optimizing the measurement data with the model. A frequency dependent resistor is used to account for the skin depth. The parasitic resistance and the inductance in the model is approximately 0.7Ω (at what frequency) and 0.05nH, respectively. The extracted unloaded Q from the measurement results at 1GHz is approximately 234 in the up state and 27 in the down state. The low Q factor of the varactor is primarily due to the lossy SiO dielectric. A nitride dielectric can be used instead of the SiO layer to increase the Q factor.

CHAPTER 6

STUDY ON ANODIC BONDING TECHNIQUES

6.1 Introduction

Anodic bonding is among the more popular methods used to bond silicon wafers with glass [8, 9]. The anodic bonding technique has been extensively utilized in the microelectromechanical systems (MEMS) for the packaging of micro sensors and micro actuators. In this work an improved anodic bonding technique is demonstrated successfully. This technique can be potentially applied towards the packaging of the MEMS variable capacitors.

6.2 Anodic Bonding

Anodic bonding is a field assisted thermal bonding that permits the sealing of silicon to glass, well below the softening point of glass. Bonding of silicon wafer and glass in an anodic bonding process involves high temperature and high applied voltage.

In the past high temperatures (1200-1500°C) and high pressure (2000-2500 psi) have been used for bonding [39, 40]. These high temperatures and high pressures are hard to achieve. Anodic bonding is an alternative approach that works at a relatively lower temperature and with an external applied electric field which replaces the high pressure. The temperature during bonding is in the range from 200 to 600 degree Celsius and the voltage is in the range from 500 to 1500 volts. In the bonding process the silicon wafers are maintained in a positive potential with respect to the glass.

The mechanism involved in the bonding process is attributed to mobile ions in the glass [8, 9]. At an elevated temperature the positive sodium ions (Na^+) in the glass have an increased mobility and are attracted to the negative electrode on the glass surface, and are removed. The stronger-bound negative ions in the glass form a space charge layer adjacent to the silicon surface. Initially the potential is uniformly distributed across the glass, but after the Na^+ ions have drifted toward the

surface a large potential drop occurs at the glass/anode interface, as shown in Figure 6.1. The resulting electric field between the surfaces pulls them into contact.

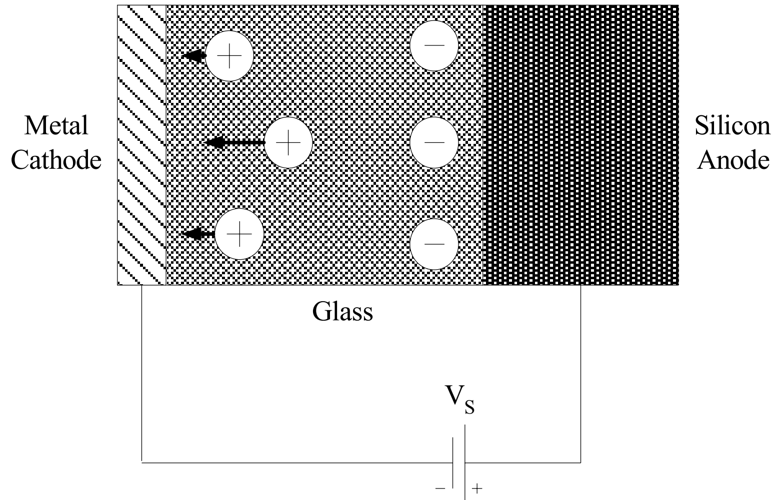

Figure 6.1: Schematic Showing the Anodic Bonding Process between Silicon and Glass

Typically the bonding begins below the negative electrode and spreads across the surface. For good bonding, a higher voltage is required if lower temperatures are used. After the voltage is removed the structures are held together by a chemical bond. This is an irreversible bonding process. The conditions for bonding described above are that the surface to be bonded must be in intimate contact and sufficient oxidation must occur at the anode to provide permanent bonds.

Some of the bonding samples have defects due to the foreign particles present in the bonding area. The particles get in the way and prevent the bonding from being complete. Around these particles a ring of air is created which is visible under a microscope.

6.3 Improved Anodic Bonding Technique

The experimental setup in Figure 6.2 is used to bond silicon with glass and the setup has one probe in contact with the glass. At 400°C and 1000V the time taken to bond a 1.5 X 1.5 cm^2 glass was approximately ninety minutes. The probe tip is placed in the center of the glass for uniform distribution of the pressure. In a modified setup two probes, placed at opposite corners of the sample, are used. The addition of a new probe decreases the bonding time; for the same temperature and voltage the bonding time is approximately sixty minutes.

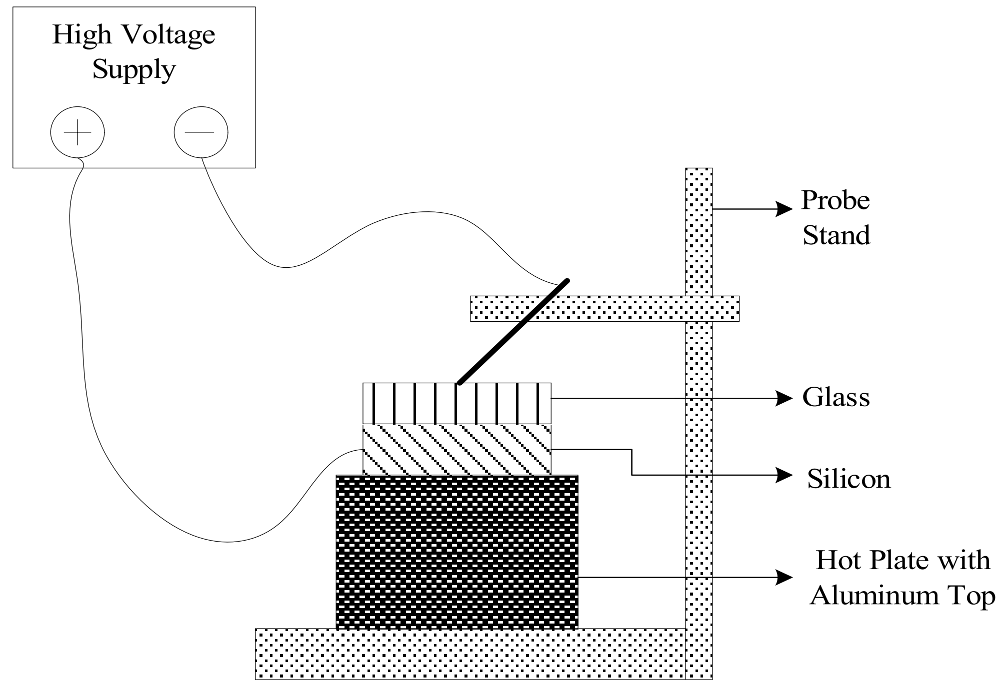

Figure 6.2: Schematic of the Anodic Bonding Setup

Instead of placing the probes directly on the glass, an aluminum block is used in between the glass and the probes as show in Figure 6.3. The aluminum block acts as infinite probes, which further reduces the bonding time. Table 6.1 lists the bonding time for a 1.5 X 1.5 cm^2 glass for varying temperature setting. The bonding time is reduced to as little as seven minutes through this improved technique.

Table 6.1: Comparison of Bonding Time for Different Temperatures at 1000 Volts

Applied Voltage (V)	Temperature (°C)	Bonding Time ~ (Min)
1000	400	7
1000	390	11
1000	380	22
1000	370	30
1000	360	38

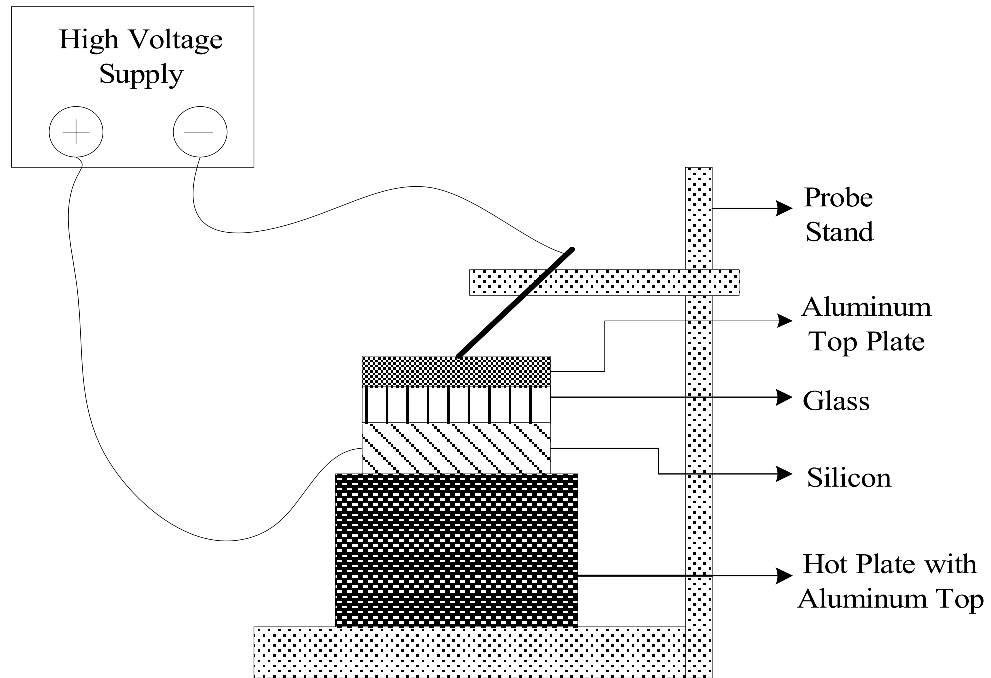

Figure 6.3: Schematic of the Improved Anodic Bonding Setup

6.4 Procedure for Anodic Bonding Process

6.4.1 Silicon Wafer Cleaning

- Rinse sample with Acetone and IPA and dry using nitrogen air gun.
- Place sample in a solution of 5% Micro 90 cleaning detergent and DI-H_2O and clean for 10 minutes in an ultrasonic cleaner.
- Rinse with DI-H_2O and dry using a Nitrogen air gun.
- Rinse again with Acetone, IPA and dry using Nitrogen air gun.

6.4.2 Glass Cleaning

- Rinse sample with Acetone and IPA and dry using Nitrogen air gun.
- Place sample in a solution of 5% Micro 90 cleaning detergent and DI-H_2O and clean for 10 minutes in an ultrasonic cleaner.
- Rinse with DI-H_2O and dry using a Nitrogen air gun.
- Rinse again with Acetone, IPA and dry using Nitrogen air gun.

- Place sample in a Piranha etch (H_2SO_4:H_2O_2, 1:1) for ten minutes, rinse with DI-H_2O and dry with dry Nitrogen.

6.4.3 Experimental Procedure

- Place silicon wafer on the hot plate with aluminum top.
- Place glass die on top of the wafer.
- Connect the voltage supply. The polarity of the applied voltage on the hot plate must be positive. Connect the negative voltage to the probe and position over the glass die.
- Set the temperature on the hot plate (350-450°C).
- Once the desired temperature is obtained, increase the voltage to 1000V through increments of 50V.
- Observe multiple fringes on the silicon-glass interface.
- Once the fringes disappear, turn off the voltage to zero through a slow incrimination of 50V.
- Turn off the hot plate. Wait for 30-40 minutes for the hot plate to cool down.
- Observe bonded surface under the microscope.

6.5 Summary

The anodic bonding procedure is certainly dependant on both the temperature and the applied voltage. An increase in temperature will cause the sodium ions to have higher mobility and are attracted to the cathode at a faster rate. The increase in the temperature has a significant effect in bonding as compared to the increase in the voltage. The addition of an aluminum plate on top of the glass has significantly reduced the bonding time.

CHAPTER 7

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

7.1 Conclusion

A one – port multi dimensional RF MEMS variable capacitor that utilizes electrostatic actuation is successfully designed and fabricated. The measurements of the fabricated circuits show good agreement with the corresponding full wave EM simulations. A cantilever beam topology was adopted for the varactors in a CPW topology. Initially the varactors with a single beam topology are designed and then later extended for multiple beam topologies (up to seven beams) in a single pedestal. The capacitance ratio varied from 12 – 20 depending on the number of beams used for designing the capacitor. The capacitance value varied from 0.11pF – 0.91pF in the up state and from 1.72pF – 14.51pF in the down state.

An equivalent circuit model was used to extract the capacitance and the parasitic element values and was found to be valid over the desired frequency range. The extracted capacitance value in the up state showed very good correlation to the designed value, while the down state showed an average reduction of 1.6pF – 2.4pF when compared to the designed value. This reduction in capacitance is attributed to the high stress in the beams (tensile in nature) which buckles the center of the beams upward. The unloaded Q factor of the varactor is extracted from the measurement results and is found to be 234 in the up – state and 27 in the down – state at 1GHz for a 5 – beam topology.

An improved anodic bonding technique is demonstrated successfully. The anodic bonding procedure is dependant on both the temperature and the applied voltage. From experimental results it is found that the increase in temperature has a significant effect in bonding when compared to the increase in the voltage. To facilitate a uniform temperature distribution over the bonding area, a 1” x 1” aluminum plate is used. The addition of an aluminum plate on top of the glass has significantly reduced the bonding time from fifty minutes to seven minutes.

7.2 Recommendations for Future Work

The proposed single beam cantilever type MEMS variable capacitors can be modified to a suspended beam topology (Figure 7.1(a)). The fabricated cantilever beams shows considerable stress which is tensile in nature. The suspended beam topology provides uniform height across the capacitor area when compared to the cantilever type design. The actuation voltage of the beams can be reduced by meandering the beams as shown in Figure 7.1(b). The silicon monoxide layer that is used in this work can be replaced by ferroelectric materials such as BST (Barium Strontium Titanate). This offers additional tunability in the design.

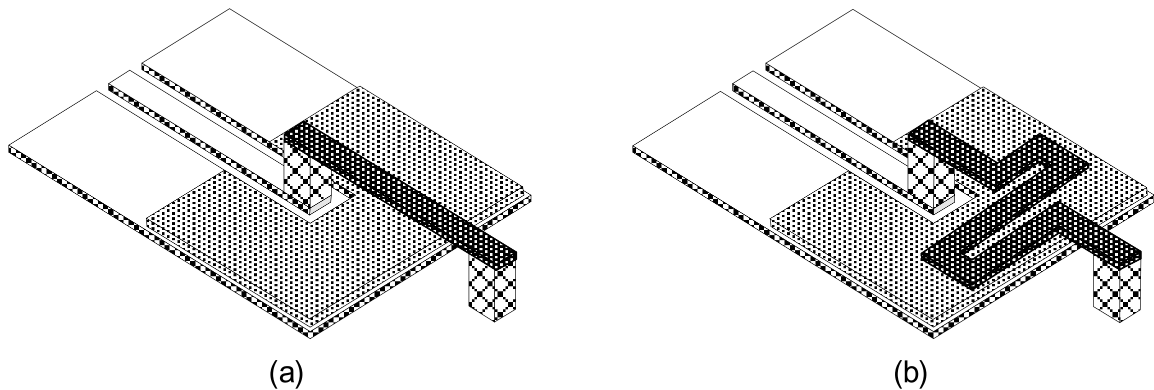

Figure 7.1: Single Beam Topology MEMS Variable Capacitor (a) Suspended Beam (b) Meandered Beam

The stress in the beams can be reduced by annealing the sample before release. This type of annealing step for a photo resist sacrificial layer creates bumps in the circuit at places with considerable height variation. To avoid this problem PMMA (polymethyl methacrylate) can be used as a sacrificial layer instead of photo resist. Electroplated gold beams can also be used instead of aluminum beams for reducing the stress.

The MEMS variable capacitors can be implemented for RF filter applications as they offer many advantages over conventional varactor based filters, including an increased dynamic range and a dramatic parts reduction.

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APPENDICES

Appendix A: Physical Characteristics and the Calculated Actuation Voltage of the Multiple Beam Capacitor Topologies

Table A.1: Physical Characteristics of the Multiple Beam Capacitor Topologies (Beam Topology, Beam Area, Up / Down State Capacitance)

Structure	Area of the top plate (μm^2)	Number of beams	Up-state capacitance (pF)	Down-state capacitance (pF)
1A	4.84×10^4	1	0.161	2.571
1B	4.84×10^4	1	0.161	2.571
1C	4.84×10^4	1	0.161	2.571
1D	4.84×10^4	1	0.161	2.571
2A	4.84×10^4	1	0.161	2.571
2B	4.84×10^4	1	0.161	2.571
2C	4.84×10^4	1	0.161	2.571
2D	4.84×10^4	1	0.161	2.571
3A	8.064×10^4	3	0.286	4.284
3B	8.064×10^4	3	0.286	4.284
3C	8.064×10^4	3	0.286	4.284
3D	3.24×10^4	2	0.108	1.721
4A	8.064×10^4	3	0.286	4.284
4B	8.064×10^4	3	0.286	4.284
4C	8.064×10^4	3	0.286	4.284
4D	8.064×10^4	3	0.286	4.284
5A	1.448×10^5	5	0.481	7.692
5B	9.69×10^4	4	0.322	5.148
5C	9.62×10^4	4	0.319	5.111
5D	9.69×10^4	4	0.322	5.148
6A	1.448×10^5	5	0.481	7.692
6B	6.38×10^4	2	0.212	3.389
6C	6.45×10^4	2	0.214	3.426
6D	6.45×10^4	2	0.214	3.426
7A	1.441×10^5	5	0.478	7.655

Appendix A: (Continued)

Table A.1: (Continued)

Structure	Area of the top plate (μm^2)	Number of beams	Up-state capacitance (pF)	Down-state capacitance (pF)
7B	1.441×10^5	5	0.478	7.655
7C	1.441×10^5	5	0.478	7.655
7D	1.441×10^5	5	0.478	7.655
8A	1.284×10^5	2	0.426	6.821
8B	1.284×10^5	2	0.426	6.821
8C	1.284×10^5	2	0.426	6.821
8D	1.284×10^5	2	0.426	6.821
9A	1.769×10^5	3	0.587	9.398
9B	1.769×10^5	3	0.587	9.398
9C	1.284×10^5	2	0.426	6.821
9D	1.284×10^5	2	0.426	6.821
10A	2.093×10^5	5	0.695	11.119
10B	2.406×10^5	5	0.799	12.782
10C	2.406×10^5	5	0.799	12.782
10D	1.878×10^5	4	0.624	9.977
11A	2.698×10^5	7	0.896	14.333
11B	2.734×10^5	7	0.908	14.524
11C	2.089×10^5	5	0.694	11.098
11D	2.732×10^5	7	0.907	14.513
12A	6.24×10^4	1	0.207	3.315
12B	3.23×10^4	1	0.107	1.716
12C	3.23×10^4	1	0.107	1.716
12D	1.61×10^4	1	0.053	0.855
13A	9.468×10^4	2	0.314	5.03
13B	9.468×10^4	2	0.314	5.03
13C	7.85×10^4	2	0.261	4.17
13D	4.84×10^4	2	0.161	2.571

Table A.2: Calculated Actuation Voltage (Equation 3.4) for the Beams Incorporated in the Capacitor Structures

Structure	Expected Actuation Voltage (V)						
	Beam 1	Beam 2	Beam 3	Beam 4	Beam 5	Beam 6	Beam 7
1A	39.51						
1B	22.18						
1C	14.25						
1D	39.51						
2A	31.74						
2B	47.81						
2C	47.81						
2D	29.52						
3A	39.51	136.92	136.92				
3B	22.18	89.27	89.27				
3C	14.25	89.27	89.27				
3D	126.97	126.97					
4A	29.52	89.27	89.27				
4B	47.81	136.92	136.92				
4C	47.81	126.97	126.97				
4D	29.52	89.27	89.27				
5A	14.25	37.62	89.27	89.27	37.62		
5B	37.62	126.97	126.97	37.62			
5C	57.85	126.97	126.97	57.85			
5D	38.24	126.97	126.97	38.24			
6A	14.25	19.21	89.27	89.27	19.21		
6B	60.23	60.23					
6C	26.06	26.06					
6D	19.12	19.12					
7A	29.52	60.23	89.27	89.27	60.23		
7B	47.81	19.22	136.92	136.92	19.22		

Appendix A: (Continued)

Table A.2: (Continued)

Structure	Expected Actuation Voltage (V)						
	Beam 1	Beam 2	Beam 3	Beam 4	Beam 5	Beam 6	Beam 7
7C	29.52	37.02	89.27	89.27	37.02		
7D	29.52	19.22	89.27	89.27	19.22		
8A	14.46	14.46					
8B	17.18	17.18					
8C	22.46	22.46					
8D	12.63	12.63					
9A	22.18	17.18	17.18				
9B	14.25	12.63	12.63				
9C	14.25	14.25					
9D	14.25	14.25					
10A	22.18	126.97	17.18	17.18	126.97		
10B	14.25	57.85	12.63	12.6	57.85		
10C	14.46	19.11	12.63	12.63	19.11		
10D	19.11	14.25	14.25	19.11			
11A	29.52	19.22	89.27	14.25	14.52	89.27	19.22
11B	29.52	19.22	89.27	14.25	14.52	89.27	19.22
11C	29.52	89.27	14.25	14.25	89.27		
11D	14.25	19.22	89.27	12.63	12.63	89.27	19.22
12A	14.25						
12B	22.18						
12C	31.98						
12D	89.27						
13A	14.25	31.98					
13B	31.98	14.25					
13C	89.27	14.25					
13D	89.27	31.98					

Appendix B: Multi – Dimensional RM MEMS Variable Capacitor with a 1 – Beam Topology

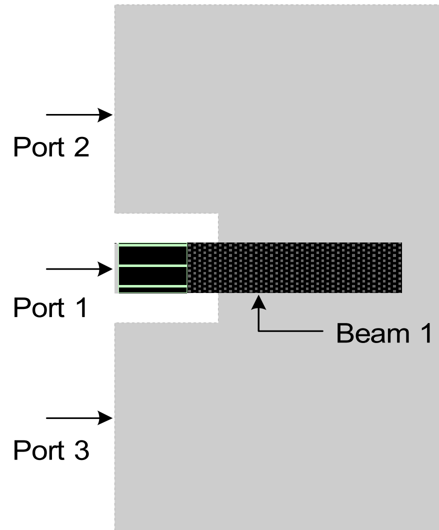

Figure B.1: Top View of the 1 – Beam Capacitor Topology used in Momentum Simulation

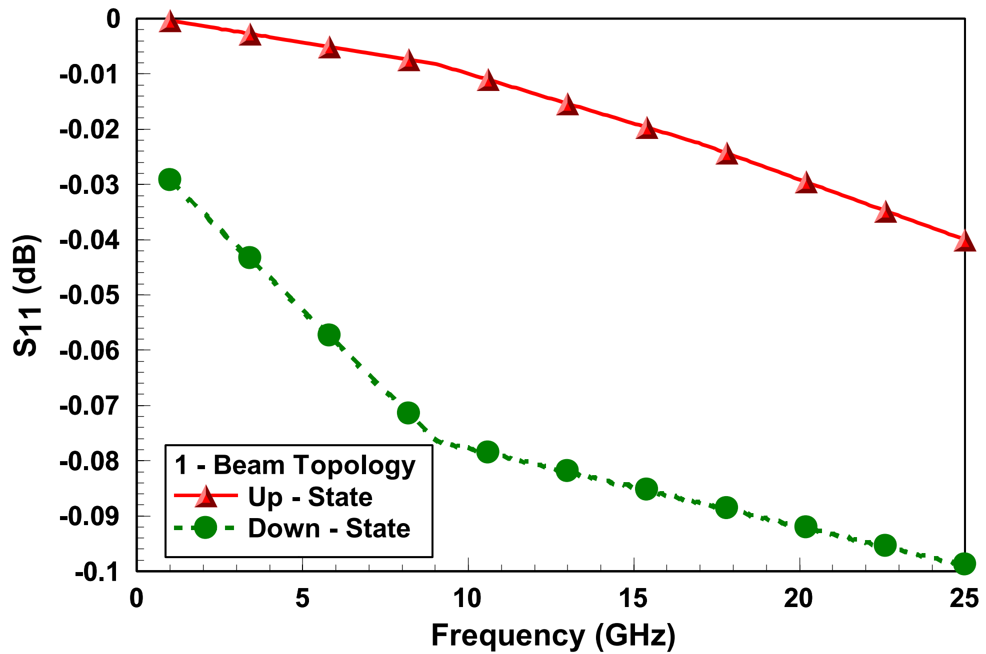

Figure B.2: EM Simulation of S_{11} Magnitude as a Function of Frequency for a 1 – Beam Topology at Various Beam States

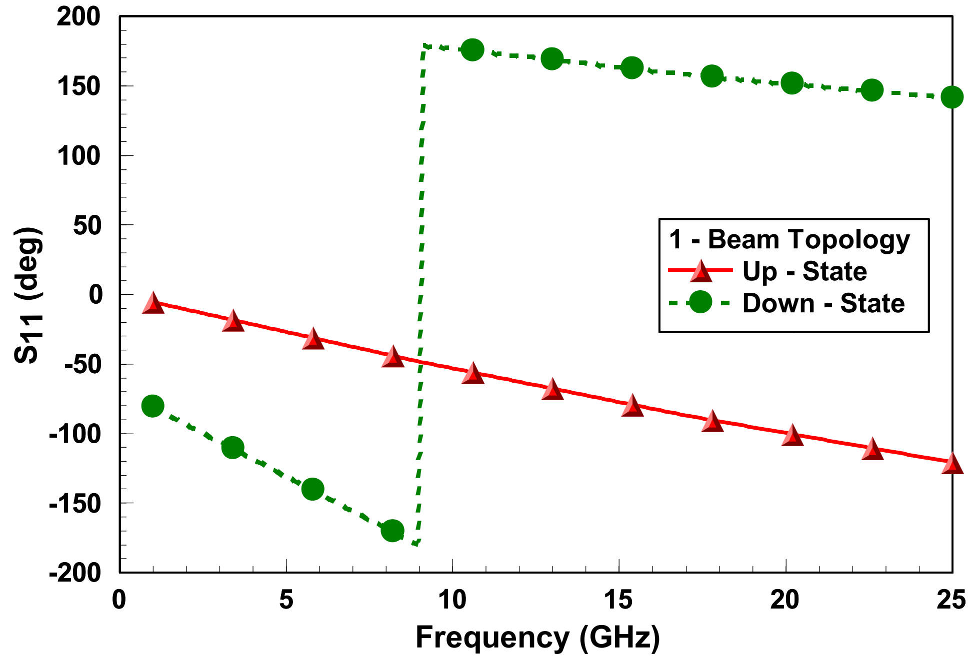

Figure B.3: EM Simulation of S_{11} Phase as a Function of Frequency for a 1 – Beam Topology at Various Beam States

Table B.1: Comparison of the Theoretical Capacitance Value with the EM Simulated Capacitance Value for the 1 – Beam Topology Capacitor

Beam States	Theoretical Capacitance Value (pF)	EM Simulated Capacitance Value (pF) (at 1GHz)
Beam in the up – state	0.16	0.15
Beam in the down – state	2.57	2.67

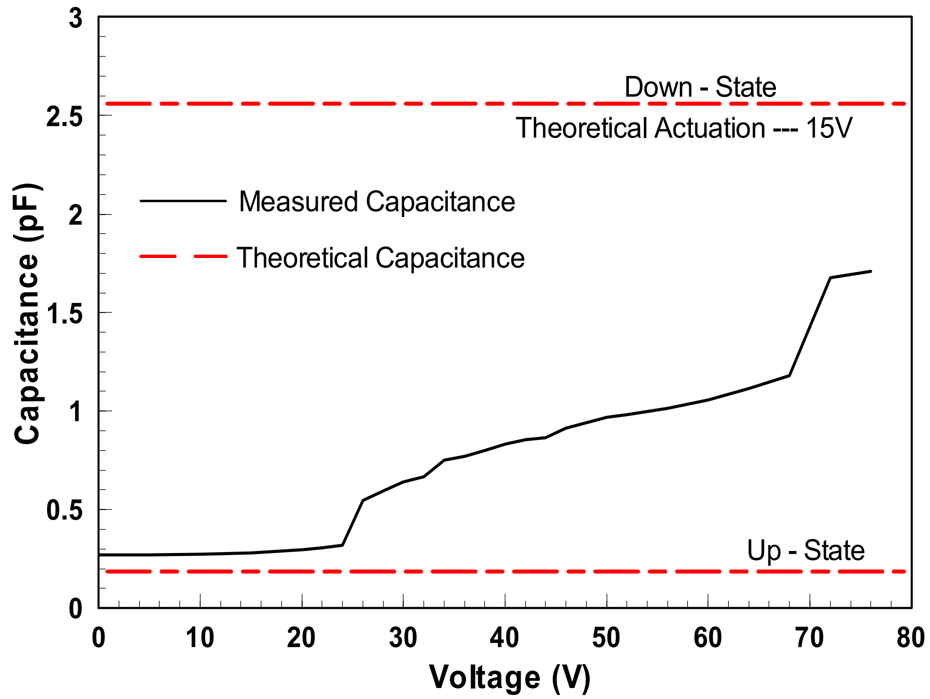

Figure B.4: Comparison of Measured and Theoretical Capacitance as a Function of Voltage for the 1 – Beam Topology Capacitor

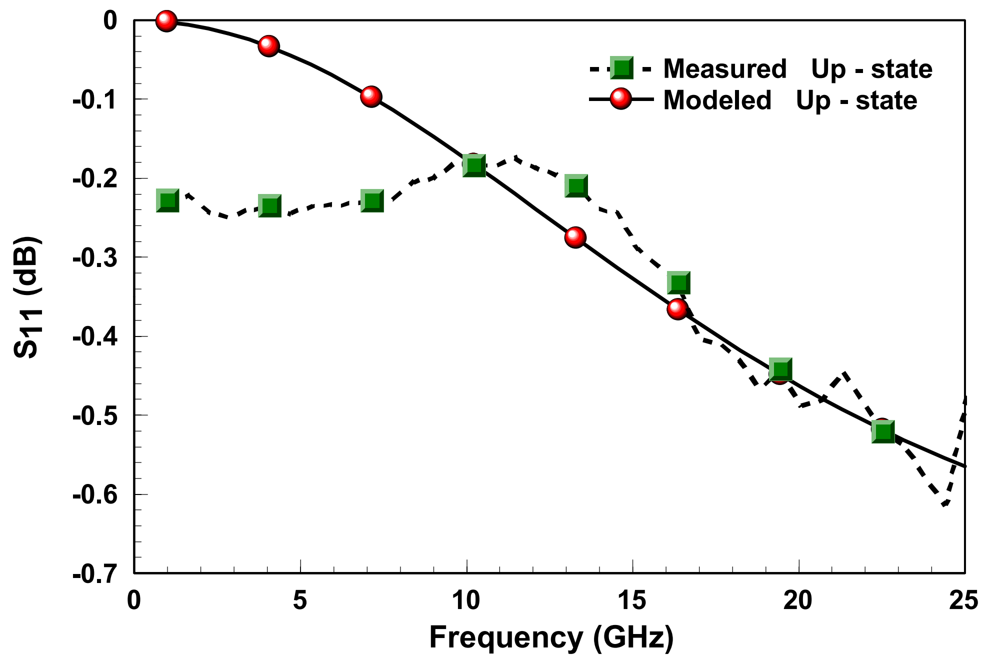

Figure B.5: Comparison between the S_{11} Magnitude of the Measured and the Modeled Capacitor (1 – Beam Topology) in the Up – State

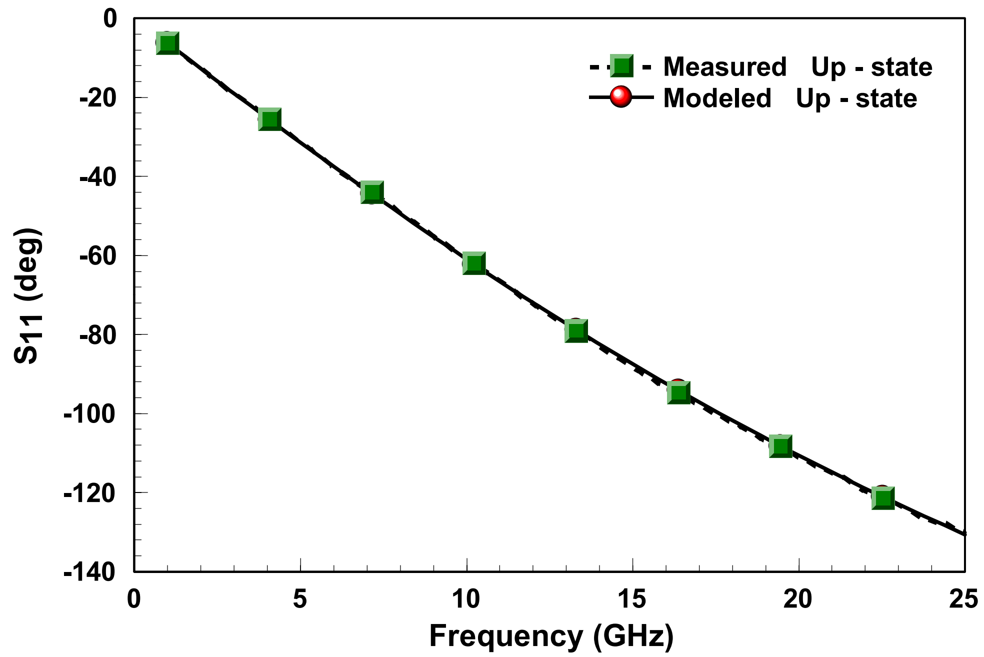

Figure B.6: Comparison between the S_{11} Phase of the Measured and the Modeled Capacitor (1 – Beam Topology) in the Up – State

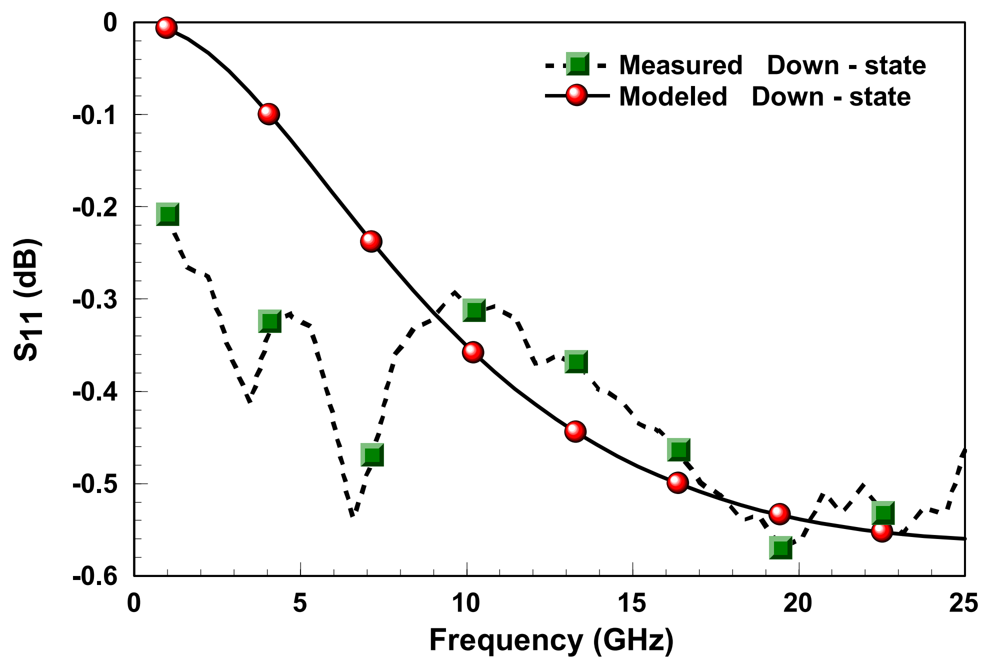

Figure B.7: Comparison between the S_{11} Magnitude of the Measured and the Modeled Capacitor (1 – Beam Topology) in the Down – State

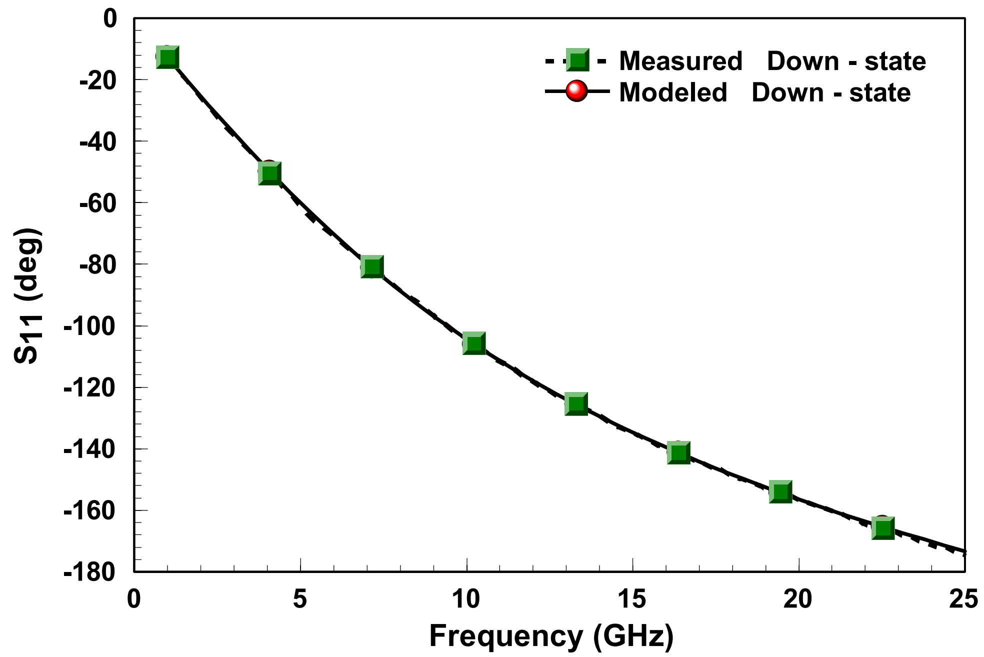

Figure B.8: Comparison between the S_{11} Phase of the Measured and the Modeled Capacitor (1 – Beam Topology) in the Down – State

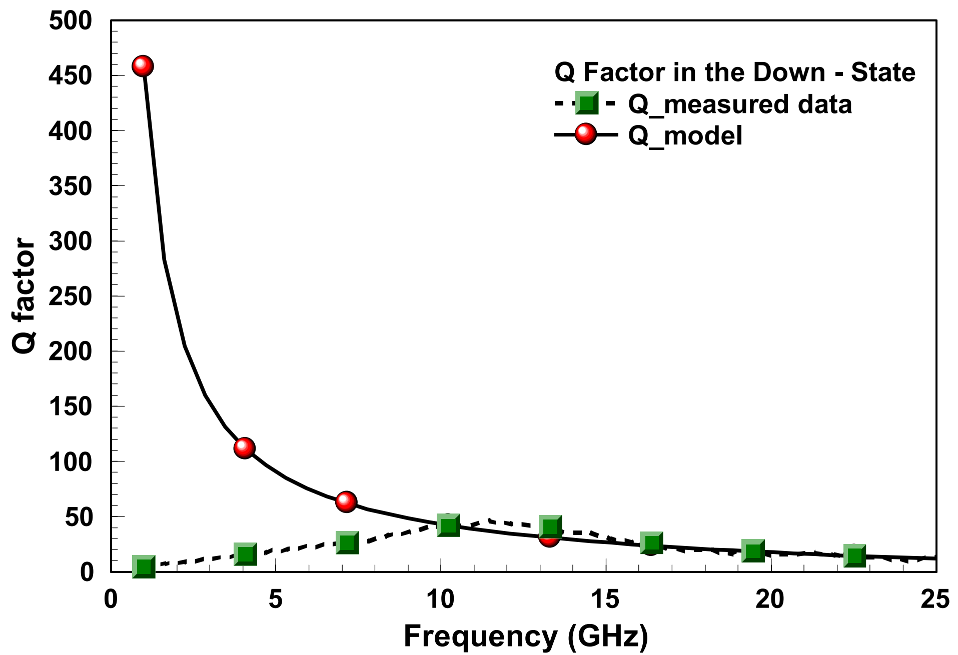

Figure B.9: Comparison between the Q – Factor of the Measured and the Modeled Capacitor (1 – Beam Topology) in the Up – State

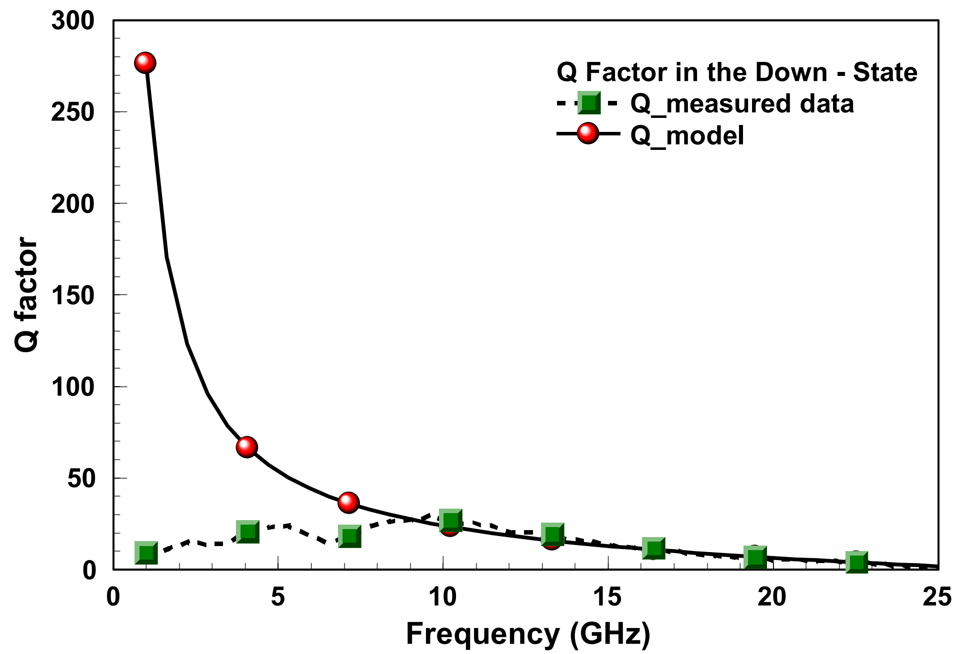

Figure B.10: Comparison between the Q – Factor of the Measured and the Modeled Capacitor (1 – Beam Topology) in the Down – State

Appendix C: Multi – Dimensional RM MEMS Variable Capacitor with a 2 – Beam Topology

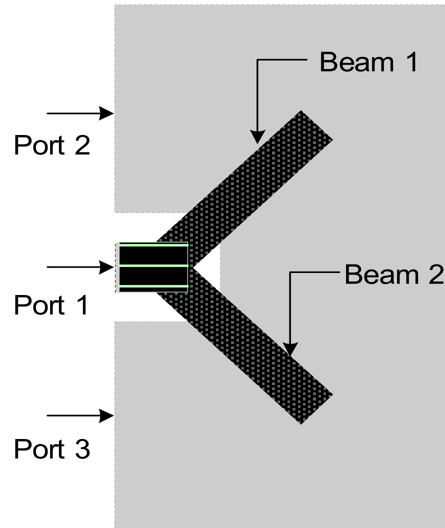

Figure C.1: Top View of the 2 – Beam Capacitor Topology used in Momentum Simulation

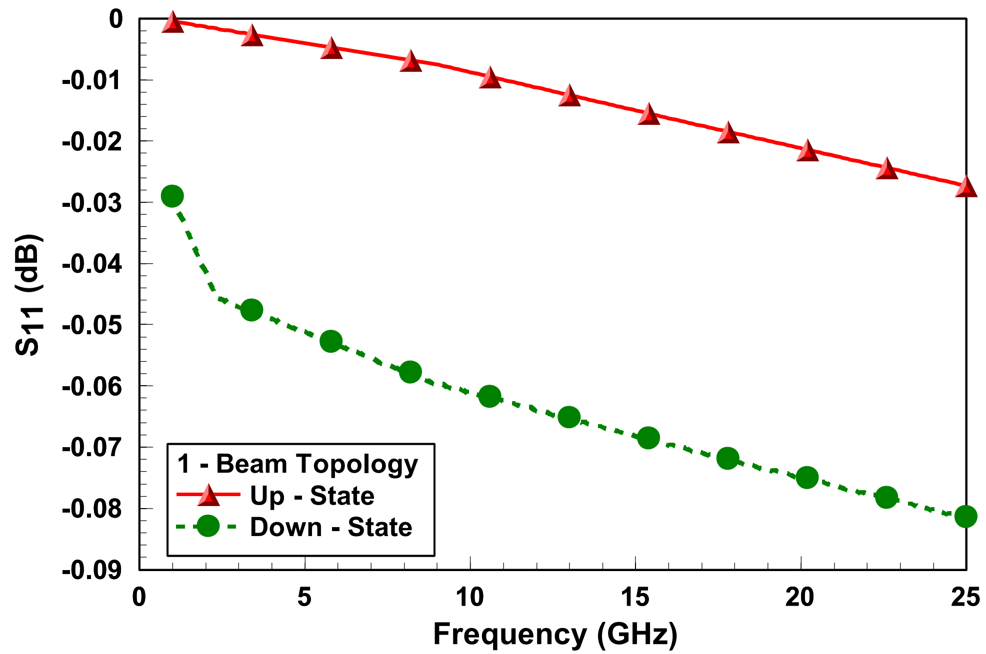

Figure C.2: EM Simulation of S_{11} Magnitude as a Function of Frequency for a 2 – Beam Topology at Various Beam States

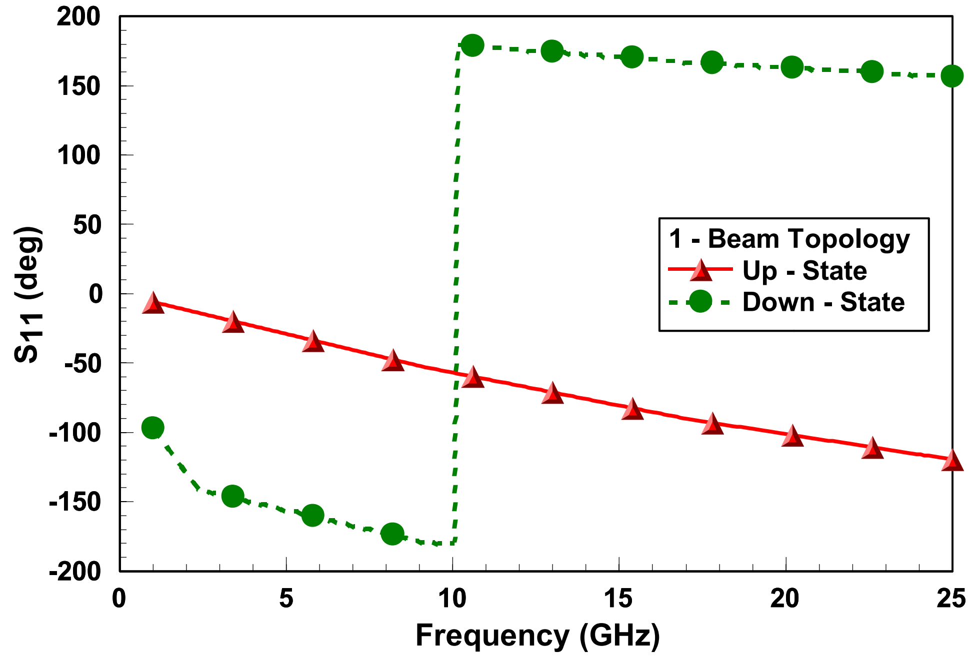

Figure C.3: EM Simulation of S_{11} Phase as a Function of Frequency for a 2 – Beam Topology at Various Beam States

Table C.1: Comparison of the Theoretical Capacitance Value with the EM Simulated Capacitance Value for the 2 – Beam Topology Capacitor

Beam States	Theoretical Capacitance Value (pF)	EM Simulated Capacitance Value (pF) (at 1GHz)
Beams in the up – state	0.21	0.17
Beams in the down – state	3.43	3.59

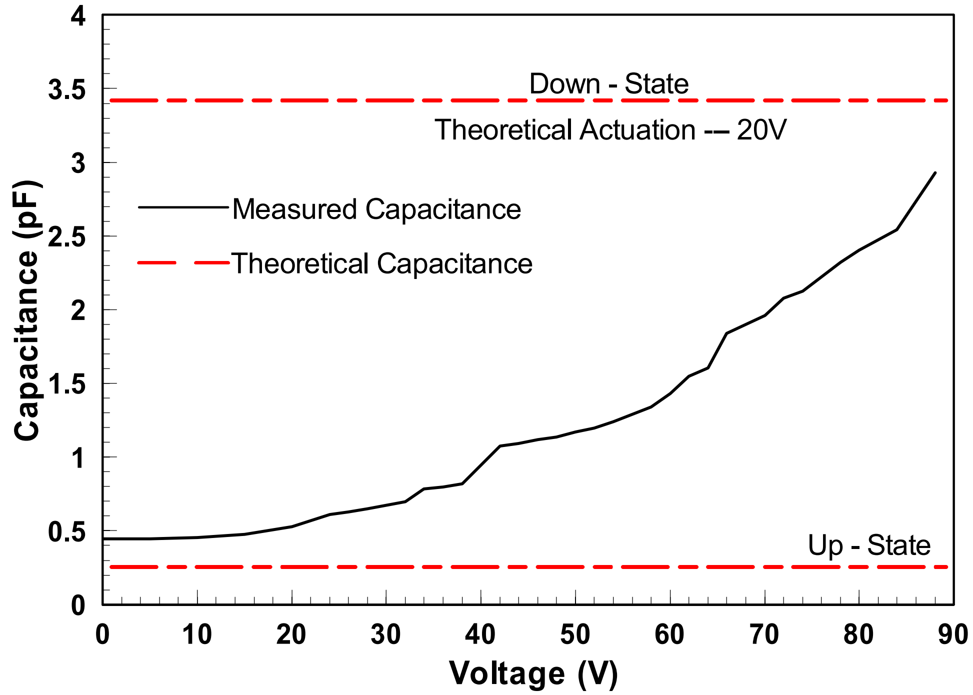

Figure C.4: Comparison of Measured and Theoretical Capacitance as a Function of Voltage for the 2 – Beam Topology Capacitor

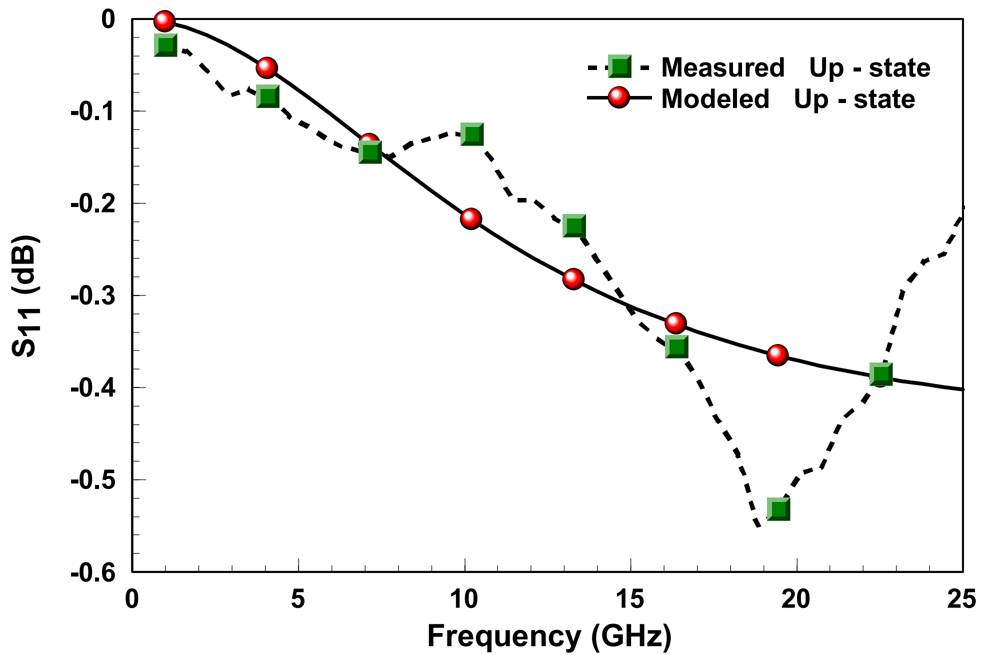

Figure C.5: Comparison between the S_{11} Magnitude of the Measured and the Modeled Capacitor (2 – Beam Topology) in the Up – State

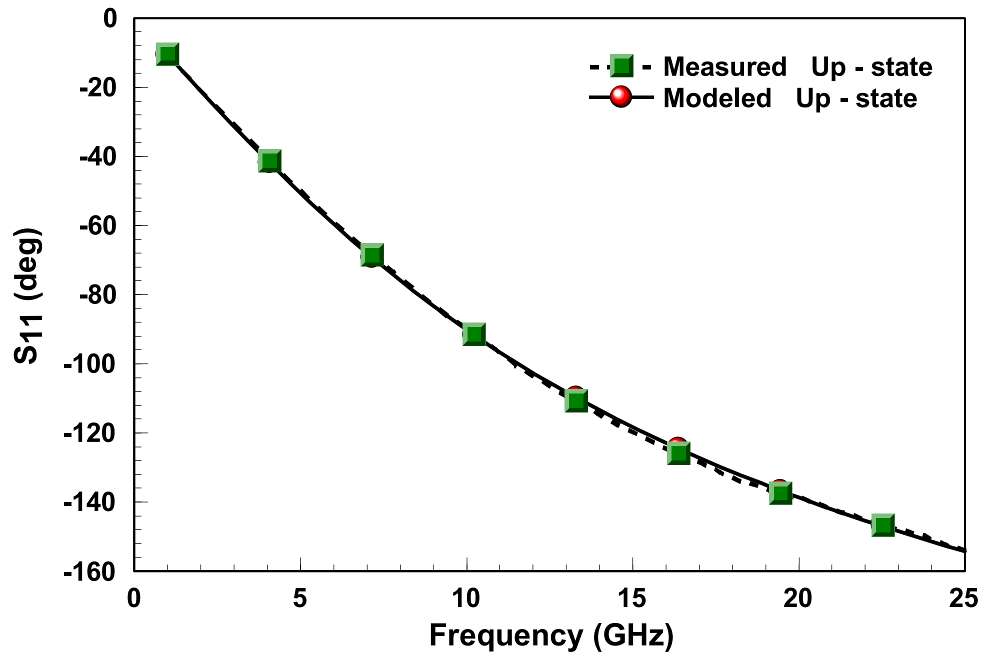

Figure C.6: Comparison between the S_{11} Phase of the Measured and the Modeled Capacitor (2 – Beam Topology) in the Up – State

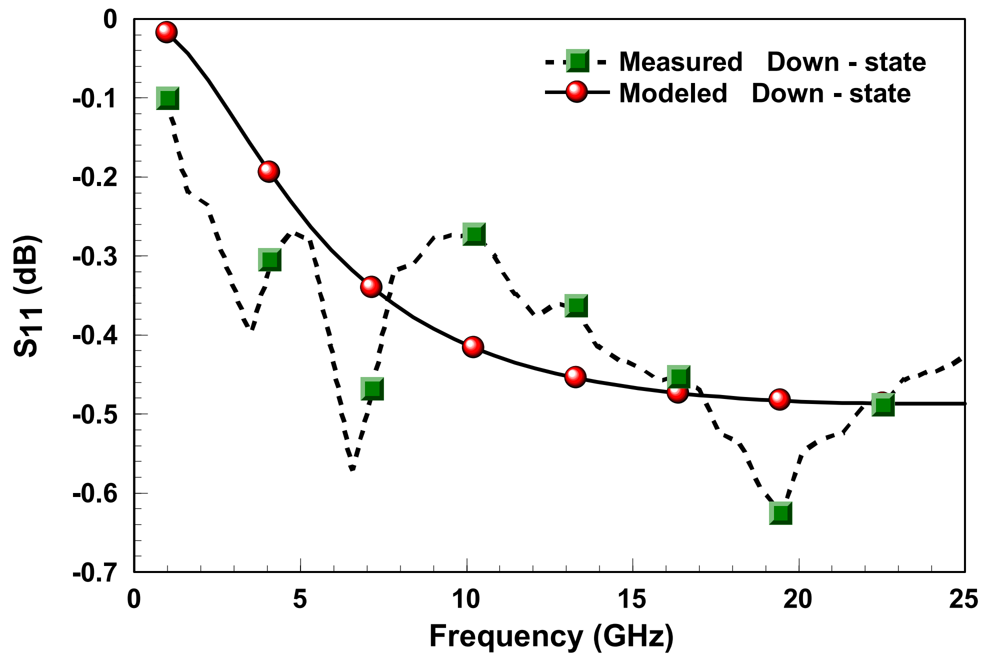

Figure C.7: Comparison between the S_{11} Magnitude of the Measured and the Modeled Capacitor (2 – Beam Topology) in the Down – State

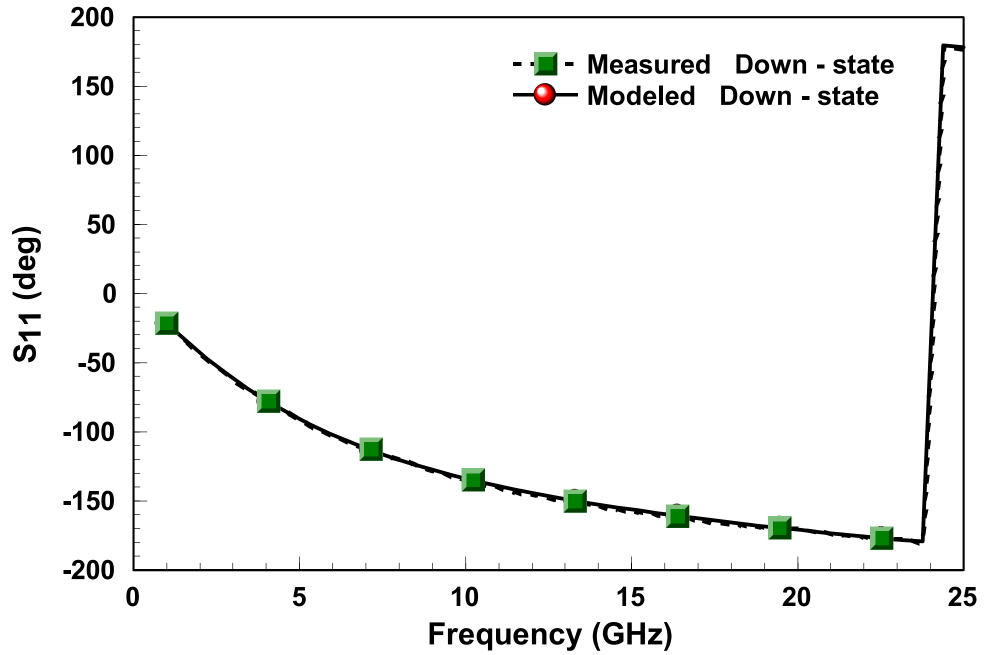

Figure C.8: Comparison between the S_{11} Phase of the Measured and the Modeled Capacitor (2 – Beam Topology) in the Down – State

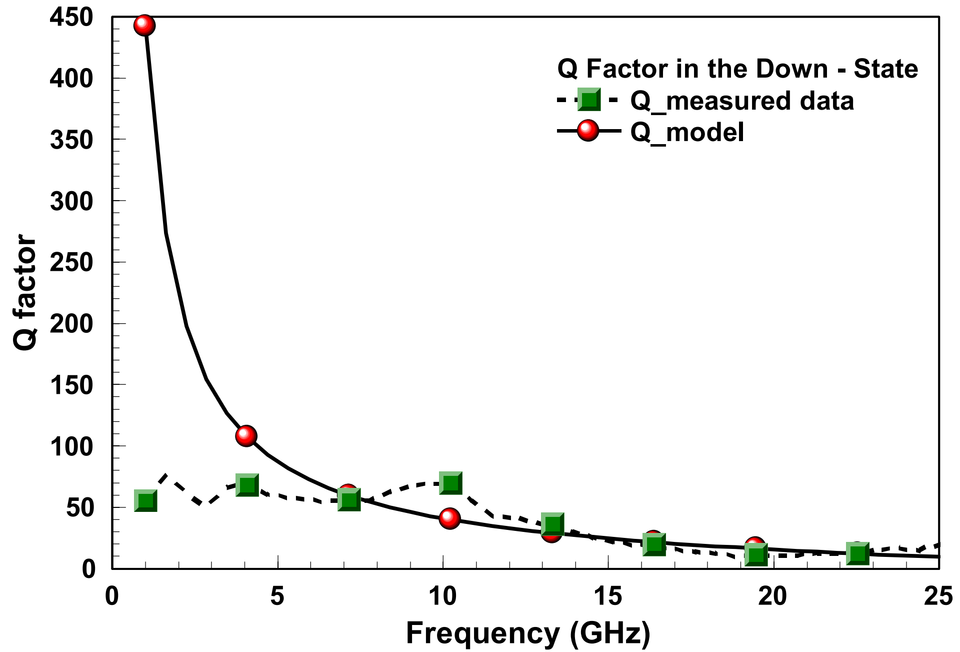

Figure C.9: Comparison between the Q – Factor of the Measured and the Modeled Capacitor (2 – Beam Topology) in the Up – State

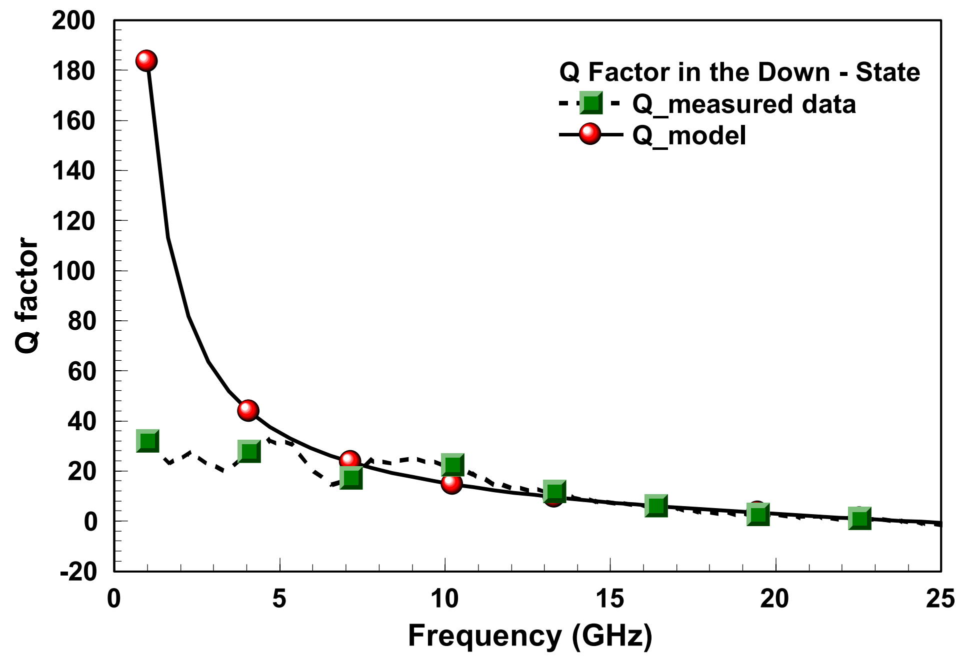

Figure C.10: Comparison between the Q – Factor of the Measured and the Modeled Capacitor (2 – Beam Topology) in the Down – State

Appendix D: Multi – Dimensional RM MEMS Variable Capacitor with a 3 – Beam Topology

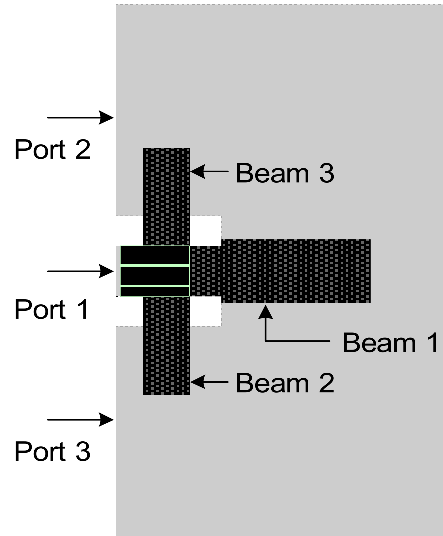

Figure D.1: Top View of the 3 – Beam Capacitor Topology used in Momentum Simulation

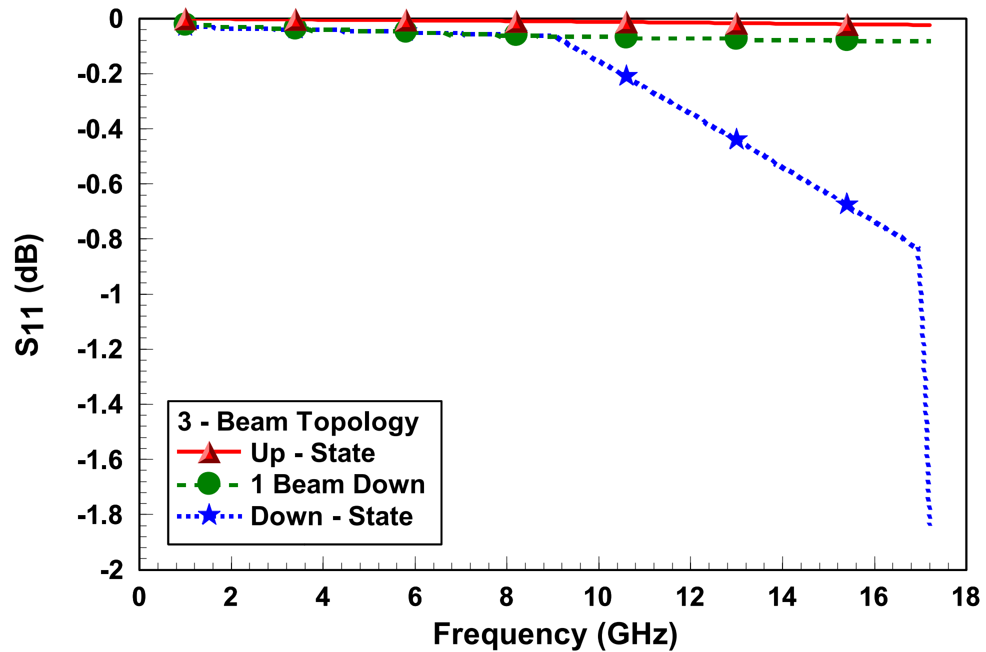

Figure D.2: EM Simulation of S_{11} Magnitude as a Function of Frequency for a 3 – Beam Topology at Various Beam States

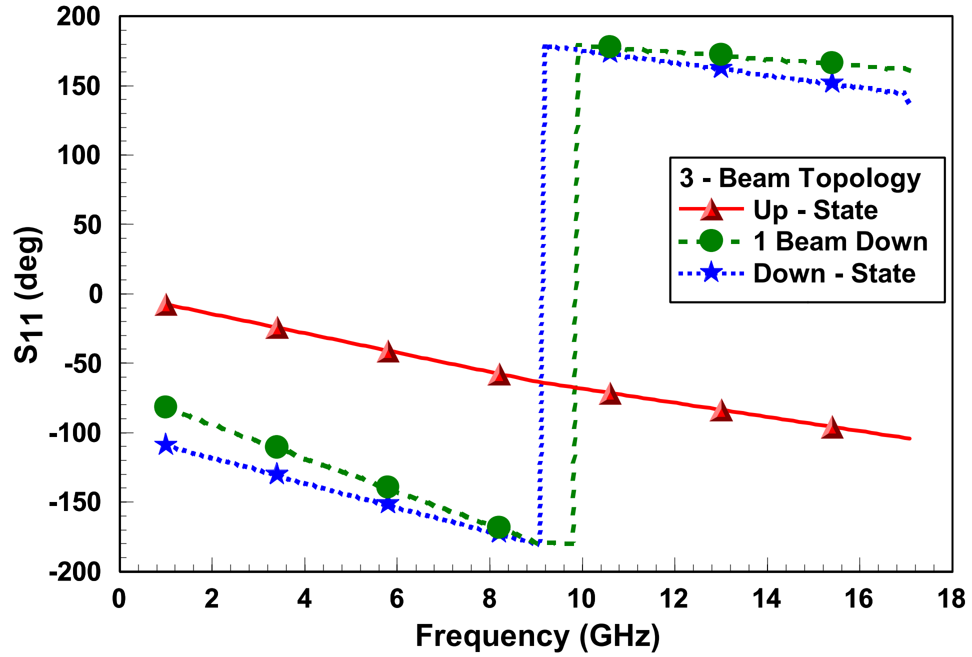

Figure D.3: EM Simulation of S_{11} Phase as a Function of Frequency for a 3 – Beam Topology at Various Beam States

Table D.1: Comparison of the Theoretical Capacitance Value with the EM Simulated Capacitance Value for the 3 – Beam Topology Capacitor

Beam States	Theoretical Capacitance Value (pF)	EM Simulated Capacitance Value (pF) (at 1GHz)
Beams in the up – state	0.27	0.21
Beam 1 in the down – state	2.68	2.75
Beams in the down – state	4.28	4.46

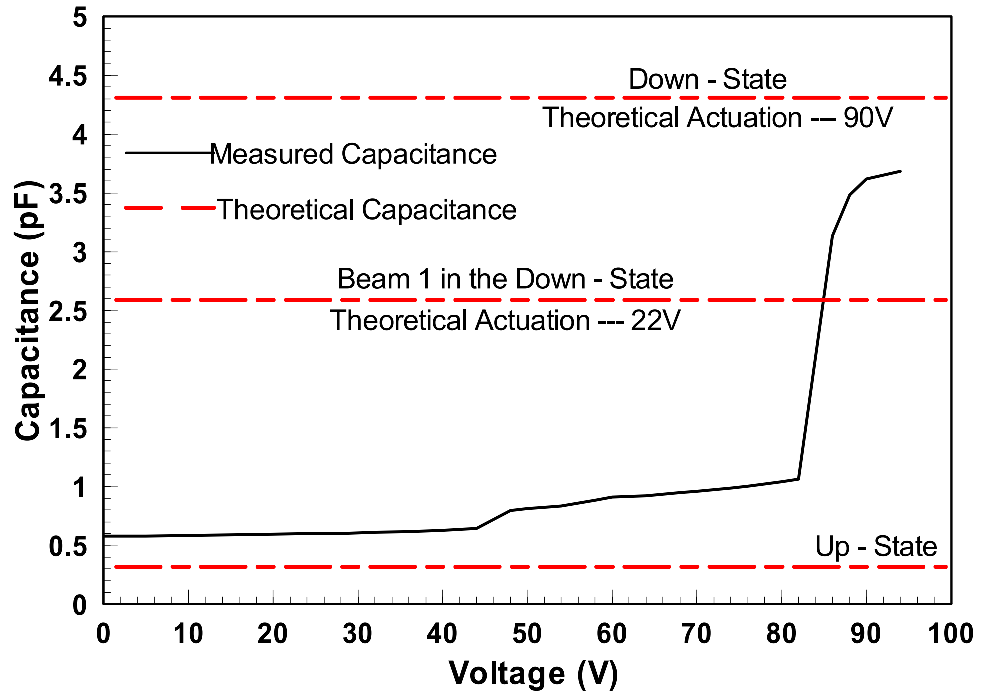

Figure D.4: Comparison of Measured and Theoretical Capacitance as a Function of Voltage for the 3 – Beam Topology Capacitor

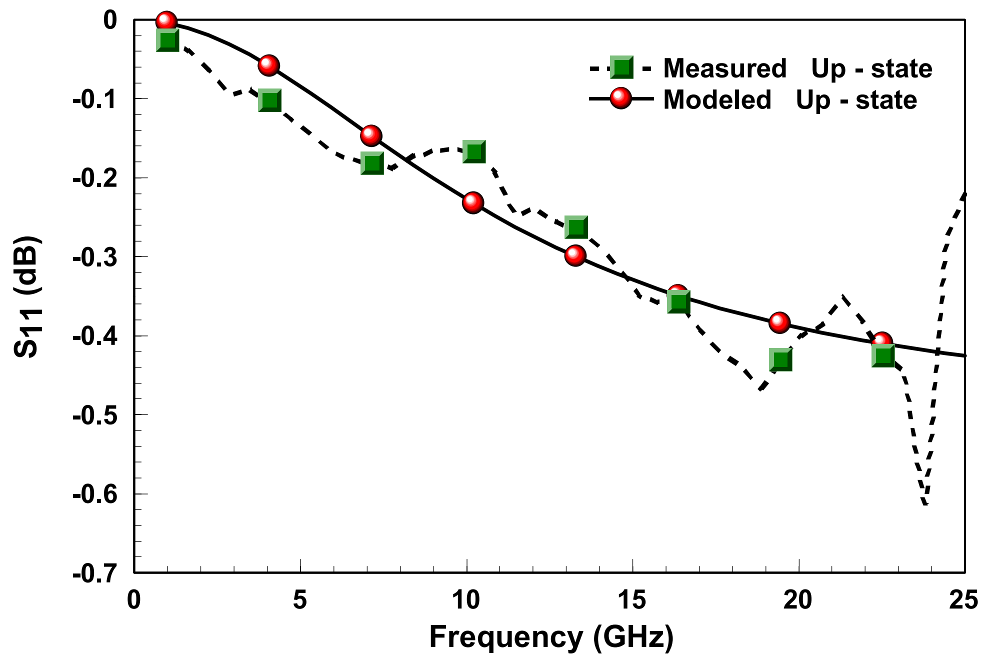

Figure D.5: Comparison between the S_{11} Magnitude of the Measured and the Modeled Capacitor (3 – Beam Topology) in the Up – State

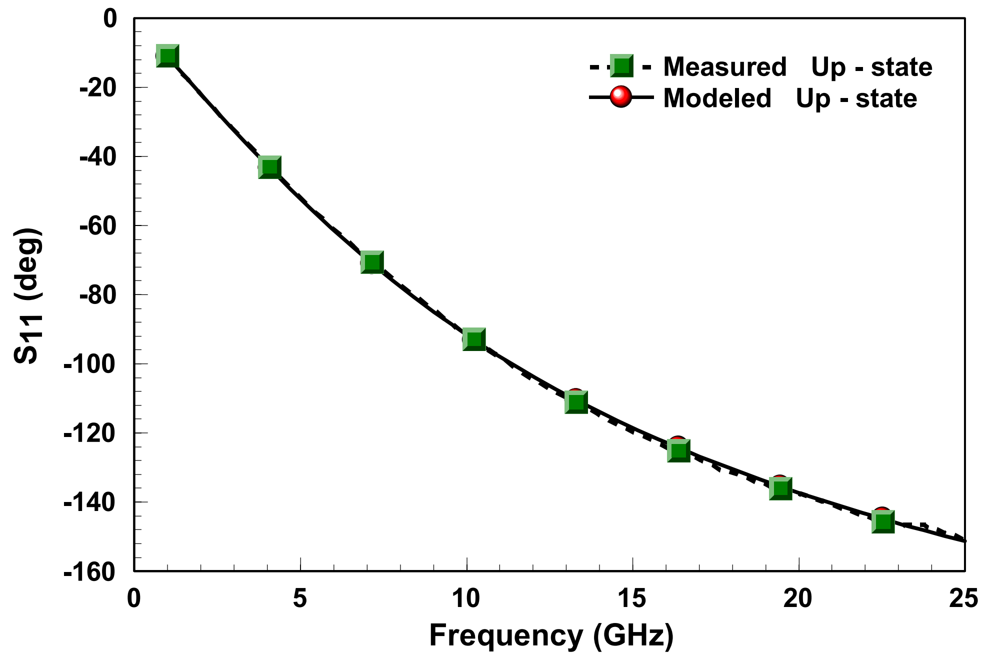

Figure D.6: Comparison between the S_{11} Phase of the Measured and the Modeled Capacitor (3 – Beam Topology) in the Up – State

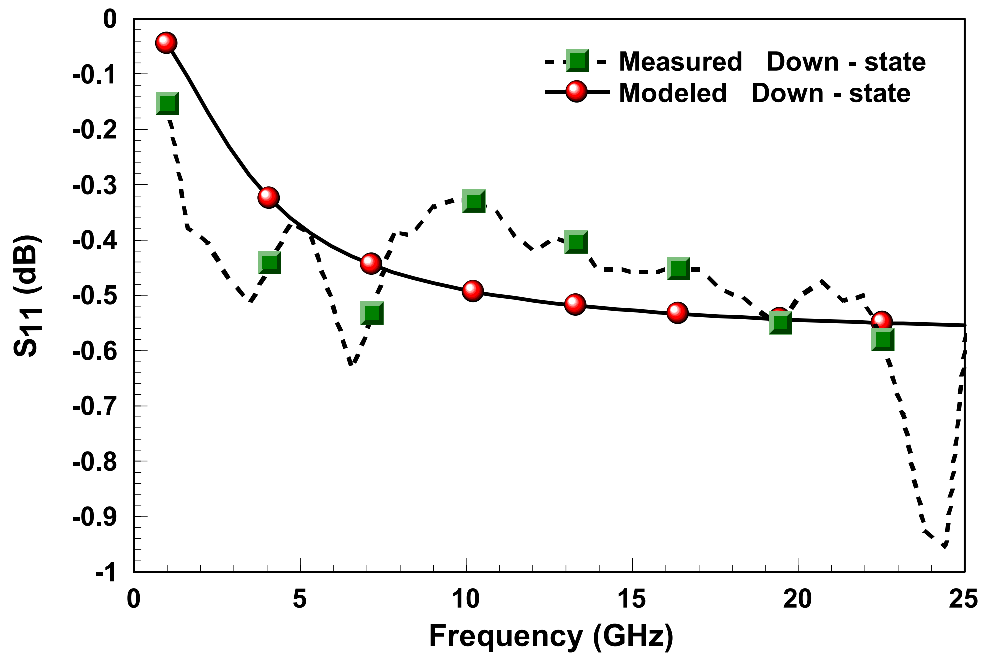

Figure D.7: Comparison between the S_{11} Magnitude of the Measured and the Modeled Capacitor (3 – Beam Topology) in the Down – State

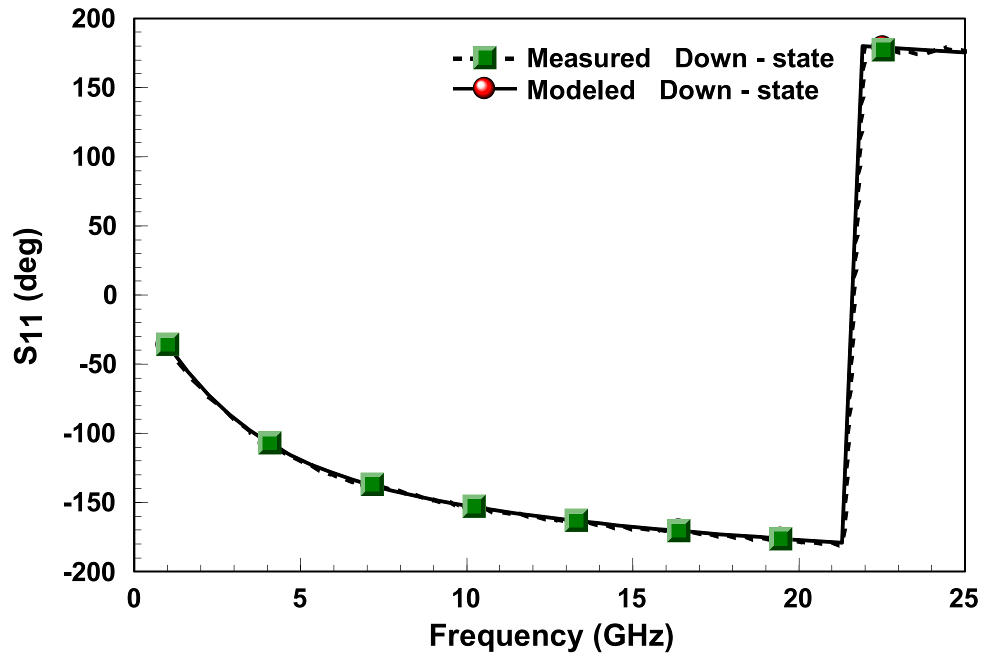

Figure D.8: Comparison between the S_{11} Phase of the Measured and the Modeled Capacitor (3 – Beam Topology) in the Down – State

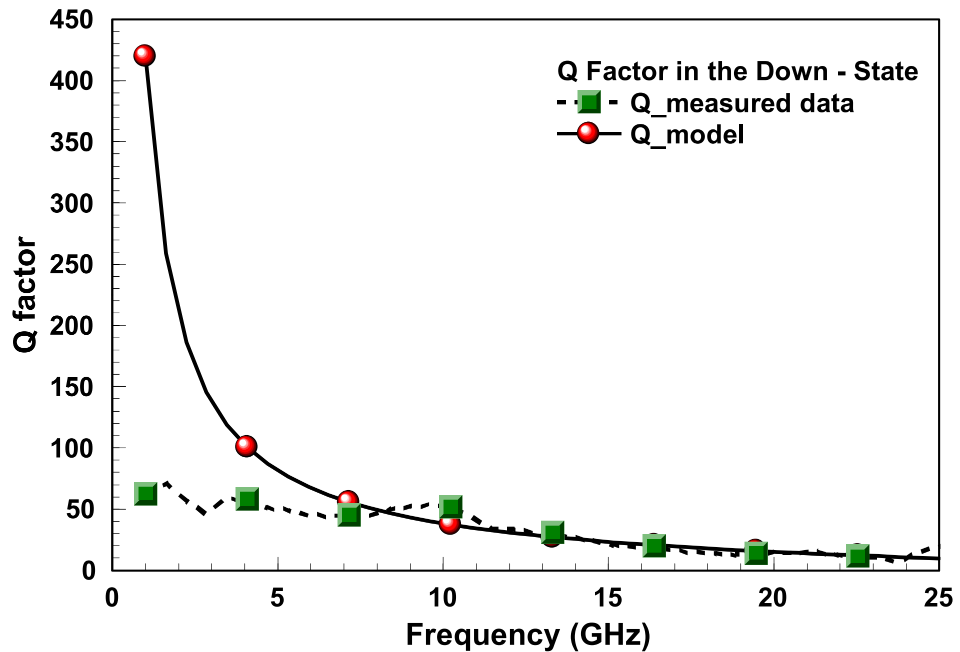

Figure D.9: Comparison between the Q – Factor of the Measured and the Modeled Capacitor (3 – Beam Topology) in the Up – State

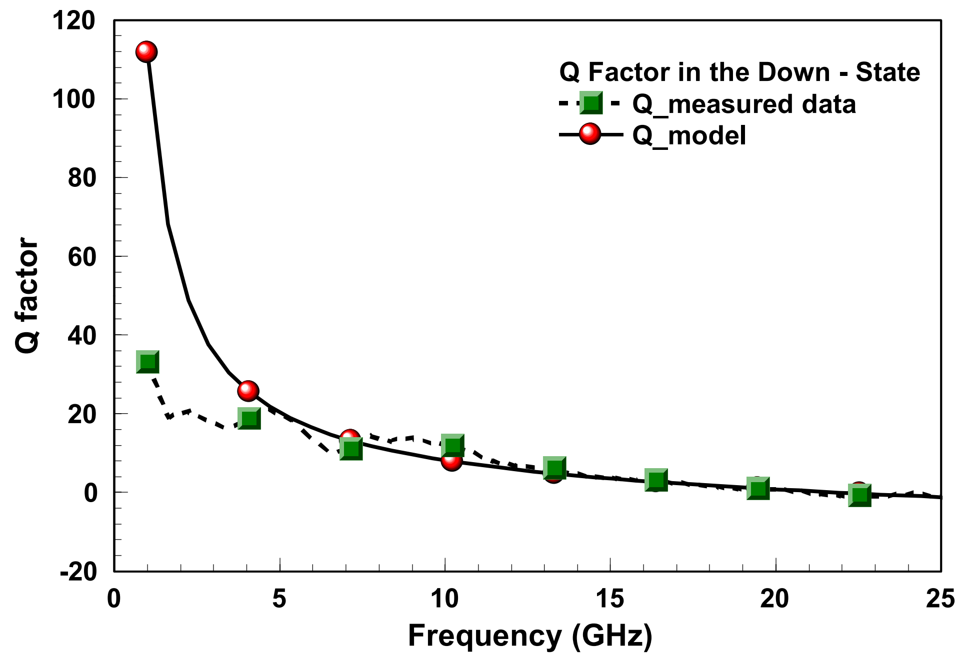

Figure D.10: Comparison between the Q – Factor of the Measured and the Modeled Capacitor (3 – Beam Topology) in the Down – State