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Fabrication of CIGS Absorber Layers Using a Two-Step Process for Thin Film Solar Cell Applications

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Cell Applications

by

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DEDICATION

To my family for their love and support

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FABRICATION OF CIGS ABSORBER LAYERS USING A TWO-STEP PROCESS FOR THIN FILM SOLAR CELL APPLICATIONS

Harish Sankaranarayanan

ABSTRACT

Copper Indium Gallium DiSelenide absorber layers are fabricated using a two step manufacturing-friendly process. The first step involves the sequential deposition of Copper and Gallium and codeposition of Indium and Selenium, not necessarily in that order, at 275° C. This is followed by the second stage, where the substrate is annealed in the presence of Selenium and a thin layer of Copper is deposited to neutralize the excess Indium and Gallium on the surface to form the Copper Indium Gallium diSelenide absorber layer. Elimination of the need for high degree of control and elimination of toxic gases like hydrogen selenide aid in the easy scalability of this process to industry.

The performance of $CuInGaSe_2$/CdS/ZnO solar cells thus fabricated was characterized using techniques such as I-V, C-V, Spectral Response and EDS/SEM. Cells with open circuit voltages of 450-475 mV, short circuit current densities of 30-40 mA/cm^2, fill factors of 60-68% and efficiencies of 8-12% were routinely fabricated. Gallium in small amounts seems to improve the open circuit voltages by 50-100 mV without significantly affecting the short circuit currents and the band gap in Type I precursors. Gallium also improves the adhesion of the CIS layer to the molybdenum back contact.

Efforts are also being aimed at improving the short circuit current densities in our high bandgap devices. It is believed that improperly bonded Ga is hurting the electronic properties of the CIGS films. A part of this work involves the reduction of the detrimental effect of Ga on the J_{sc}'s by modifying the base process, so as to improve the homogeneity of the film. The modifications include lowering the Ga level as well as fine-tuning the annealing step. Ar annealing of the samples has also been incorporated. The short circuit current densities have been improved significantly by the above mentioned modifications. At present, the best J_{sc}'s are in the 33-35 mA/cm^2 range. The V_{oc}'s have also been improved by splitting the Ga into two layers and replacing the top Cu layer by a Ga layer. Light soaking studies of the absorber have also been carried out.

The baseline Type I process has also been adapted to a new load-locked in-line evaporator system. Device performance dependence on Ga and In thickness as well as the top selenization temperature has been determined in this research. The effect of moisture on the quality of the films has been studied. Bandgap variations due to the presence/absence of Se during the Cu deposition has been investigated. The impact of substrate cleaning/Moly deposition conditions on the device performance has been explored. Insitu Ar annealing studies of CIGS absorbers have been carried out. Alternate buffer layers have been pursued. Devices with V_{oc}'s as high as 480 mV, J_{sc}'s as high as 40.7 mA/cm^2 and fill factors of 66% have been fabricated.

CHAPTER 1

INTRODUCTION

The demand for energy has been increasing ever since the onset of the industrial revolution. This has led to an alarming rate of consumption of fossil fuels such as coal, oil and natural gas. The supply of these fuels is decreasing while the demand for these is increasing all the time. In addition, waste products formed during the burning of these fuels have led to environmental pollution. Because of the dwindling supply and the resulting pollution, alternate sources of clean energy are required to meet the energy demands of the developing world. Alternate sources include hydroelectric, nuclear, tidal, wind, geothermal and solar energy.

Although a source of clean energy, hydroelectric plants destroy the river ecosystems on which they are built. Nuclear energy is attractive because of its immense potential. It is not very popular because of its radioactive waste products and accidents in the power plants which can cause widespread damage. Tidal energy and wind power are not attractive because there are viable only in selected parts of the world.

Solar energy on the other hand is economically viable and has unlimited potential. The advantages of solar power are that it is environmentally clean and virtually inexhaustible. The only cost involved in the generation of solar power are the fabrication and initial installation costs of the solar modules. Once installed the solar modules hardly require any maintenance.

Photovoltaics is a high-technology approach to converting sunlight directly into electrical energy. The electricity is in the form of direct current which can be used directly or can be converted to A.C or stored for later use. Although discovered in 1839 by Henri Becquerel solar cells were given a serious thought only after the fabrication of the first practical solar cell at Bell labs in 1954 [1]. Silicon solar cells eventually found widespread use as a source of power on satellites where reliability as opposed to cost was the primary concern.

Photovoltaics started to be considered as a terrestrial source of power due to the lack of availability of oil in the industrialized world during the early 1970's. The recent California power crisis highlighted the need for alternate energy sources. In order to be a commercially viable source of terrestrial power, attention needs to be focussed on improving performance, lowering costs and increasing reliability.

A photovoltaic device is a solar powered battery whose only consumable is the light that fuels it. There are no moving parts, operation is environmentally benign and there is nothing to wear out if the device is encapsulated [2]. Photovoltaic systems are modular, and so their electrical power output can be engineered for any application, The incremental additions are also easily accomadated as opposed to conventional approaches.

While single crystal silicon (Si) solar cells have exhibited efficiencies of 24% [3], the high processing costs involved make them unsuitable for extensive terrestrial applications. The material cost of Si solar cells is also high, as Si is an indirect band-gap semiconductor and hence a larger thickness is needed to efficiently absorb the incident sunlight. Since the thickness of the cell is larger, higher material purity is required to ensure the collection of the generated carriers and avoid recombination process. This increases the cost even further. This has led the PV industry to explore alternate technologies which are cost effective.

PV technologies based on thin films offer a suitable alternative as material costs are low. Thin films used in solar cells are usually direct bandgap semiconductors which effectively absorb the incident sunlight within a few microns. This ensures that the material cost is low. Moreover, thin films support low cost processing techniques as well as low cost substrates which further reduce the cost of a module as compared to crystalline Si.

While being cost-effective, solar cells based on thin films are not as efficient as those based on Si. This is due to the fact that most of the thin films used in solar cells are compound semiconductors and are polycrystalline in nature. This leads to a higher recombination rate due to grain boundaries as well as due to the complex defect chemistry of these semiconductors. So there is a cost to efficiency trade-off. Thin film technologies based on CIS, CIGS, CdTe have shown lot of promise with high efficiencies for laboratory area cells [4]. The module performance at the moment is comparatively lower. Research groups and the PV industry are collaborating to address the issue of improved module efficiency. Table 1.1 lists the efficiencies of some modules based on thin films [5, 6, 7].

Electricity generated from conventional sources cost about 6 to 10c/kwh, while solar power costs 25c/kwh. So the cost of electricity generation has to be reduced considerably for solar power to compete with conventional energy plants. In order to achieve this goal module efficiencies need to be around the 15% mark.

Table 1.1 Comparison of Performance of Commercial Thin Film Modules

Company	Material	Area(cm^2)	Efficiency %	Power (W)
Solar Cells Inc.	CdTe	6728	9.1	61.3
Solarex	a-Si/a-SiGe	7417	7.6	56
Siemens Solar	CIS	3859	10.2	39.3
BP Solar	CdTe	4540	8.4	38.2
ECD	a-Si/a-Si/a-SiGe	3906	7.8	30.6
Golden Photon	CdTe	3350	8.7	29.3
EPZ	CIGS	3746	6.9	25.7
USSC	a-Si/a-Si	3676	6.2	22.8
Fuji	a-Si/a-Si	1200	8.9	10.7
Seimens Solar	CIS	938	11.1	10.4
Matsushita Battery	CdTe	1200	8.7	10.0
USSC	a-Si/a-SiGe/a-SiGe	903	10.2	9.2
BP Solar	CdTe	706	10.1	7.1
Energy PV	CIGS	741	8.1	6
ISET	CIS	845	6.9	508
Showa Shell	CIGS	51.7	14.2	-
Siemens Solar	CIGSS	3651	11.8	-
Showa Shell	CIGS	3459	13.4	-
U.Uppsala	CIGS	16.0	16.6	-
BP Solarex	CdTe	4874	10.7	-

CHAPTER 2

SOLAR CELL DEVICE PHYSICS

A solar cell is a device used to convert solar energy into electricity. In its simplest form, a solar cell is basically a p-n junction diode which is in turn formed by bringing a n-type semiconductor in contact with a p-type semiconductor. Contacts that can be either transparent or metallic are made to the semiconductors. Thus a solar cell is essentially a four layer device on a suitable substrate. When a semiconductor absorbs light with energy greater than its bandgap, electron-hole pairs are generated. The generated carriers are separated by the electric field in the depletion region and are eventually collected at the contacts. Since the solar cell is a p-n junction diode, a thorough understanding of a p-n junction is necessary to understand the device behavior and operation of a solar cell.

2.1 Semiconductors

A material whose conductivity is between that of a highly conductive metal and a highly resistive insulator is called a semiconductor. Semiconductors can be classified as either intrinsic or extrinsic depending on their purity. They can also be classified as single crystalline, polycrystalline or amorphous based on their structure. In addition, semiconductors are called n-type or p-type, based on whether the majority carriers are electrons or holes.

The conductivity of a semiconductor can be varied by doping it. Doping is the process of adding impurities to a semiconductor to increase the concentration of charge

carriers thereby improving its conductivity. A semiconductor is said to be extrinsic, if it has excess electrons or holes due to either ionized donor impurities or ionized acceptor impurities respectively. An intrinsic semiconductor is one in which free electrons in the conduction band or free holes in the valence band are created purely by thermal excitation across the bandgap. When a semiconductor is highly doped such that the fermi level lies within the conduction or valence bands the semiconductor is said to be degenerate.

The bandgap E_g of a semiconductor is defined as the separation between the energy of the highest valence band and the energy of the lowest conduction band. This is also called the forbidden gap as there are no allowed energy states within the bandgap. The bandgap of a semiconductor determines the interaction of light with the semiconductor. In general, the bandgaps of most semiconductors decrease with increasing temperature given by [8]

$$E_g = E_g(0) - \frac{\alpha T^2}{T + \beta} \tag{2.1}$$

where $E_g(0)$ is the bandgap at 0 kelvin and T is the absolute temperature.

2.2 P-N Junction

A n-type semiconductor has a large concentration of electrons while a p-type semiconductor has a large concentration of holes. When these two materials are brought in contact with each other a p-n junction is formed. At the instance of junction formation, a diffusion current J_{diff} flows from the p-type semiconductor to the n-type semiconductor as a result of the concentration gradient. The diffusion of mobile carriers in the region around the p-n junction leaves behind immobile (fixed) charges. Since this region is depleted of charge carriers, it is called the depletion or the space charge region. The ionized impurities in the depletion region are no longer

balanced by the mobile charge carriers. This leads to a build up of Positive ($N_D{}^+$)

charge on the n-side of the junction and a negative ($N_A{}^-$) charge on the p-side. This

causes a potential difference across the junction resulting in an internal electric field.

This electric field is directed from n to p and hence opposes the further flow of holes

from the p region and electrons from the n region. The magnitude of this field is

such that it exactly balances the further flow of majority carriers by diffusion. Hence

under thermal equilibrium, there is no current flow. The magnitude of electric field

is given by

$$E = \frac{-dV(x)}{dx} \tag{2.2}$$

where V is the potential across the junction. The potential difference is maximum at

the metallurgical junction. This leads to an electric field maximum at the junction.

Figures 2.1, 2.2, and 2.3 show the space charge region, the electric field distribution

and the potential distribution.
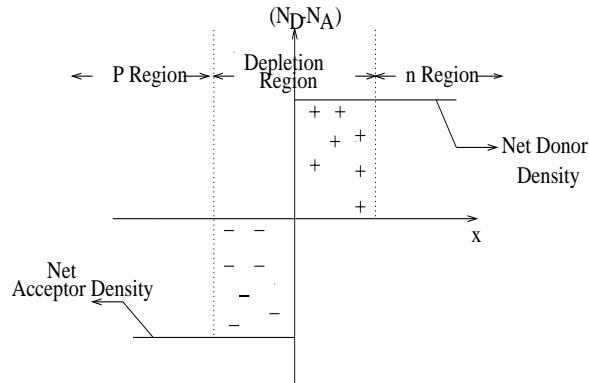
Figure 2.1 Space Charge Distribution of an Abrupt P-N Junction in Equilibrium

Equilibrium energy band diagrams of isolated n-type and p-type semiconductors

are shown in Figure 2.4. When these two semiconductors are brought in contact with

each other, there is a bending of the energy bands as depicted in Figure 2.5. This
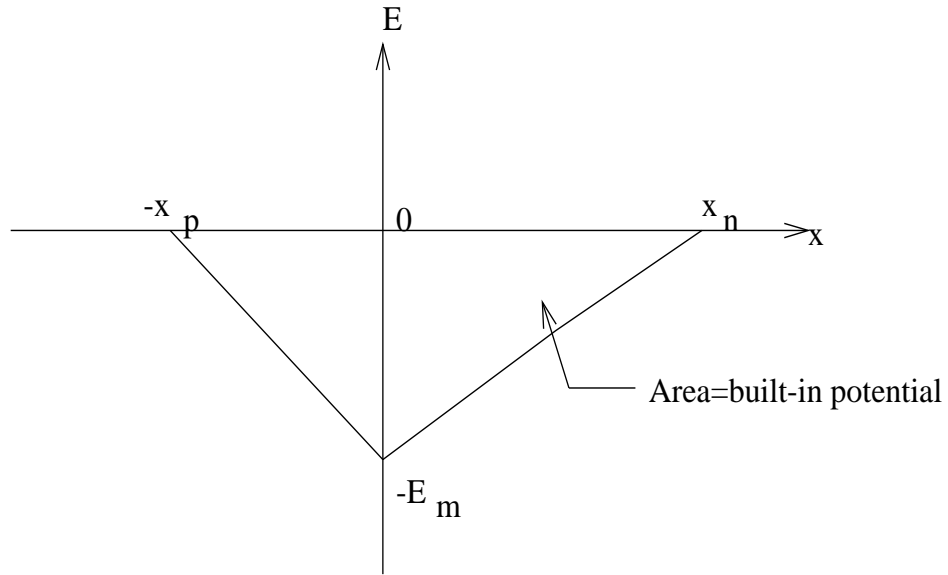
Figure 2.2 Electric Field Distribution of an Abrupt P-N Junction

The E axis is vertical, the x axis horizontal. Points $-x_p$, 0, and x_n are marked on the x axis. The minimum value is $-E_m$. An arrow points to the triangular region labeled "Area=built-in potential".
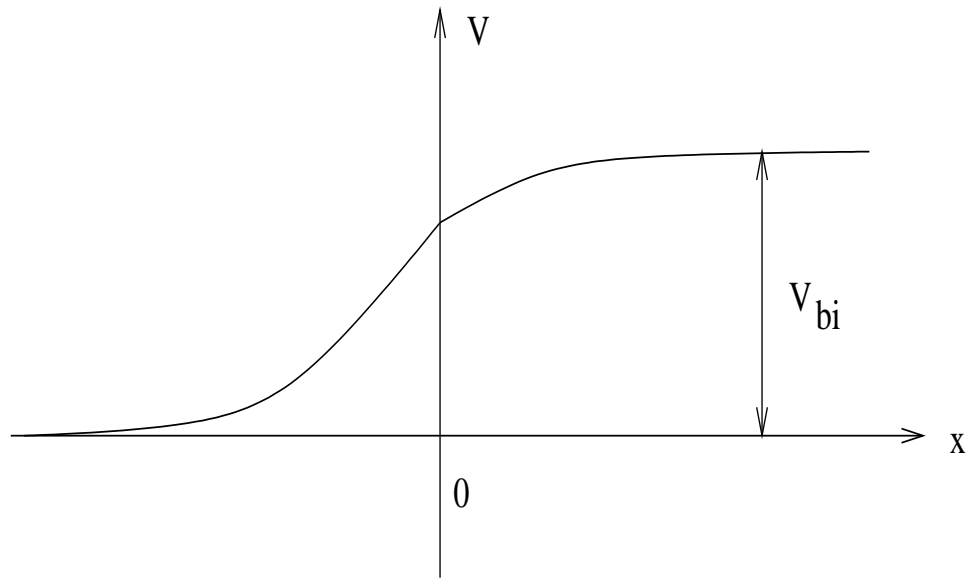
Figure 2.3 Potential Distribution of an Abrupt P-N Junction

The V axis is vertical, the x axis horizontal with 0 marked. The potential difference is labeled V_{bi}.

band bending is caused due to the fact that a system under thermal equilibrium can have only one Fermi level.
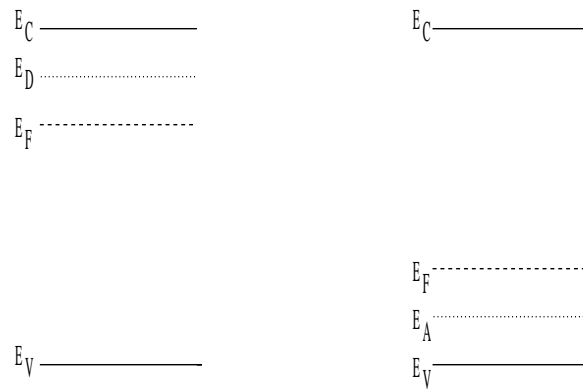
Figure 2.4 Energy Band Diagrams of Isolated N-Type and P-Type Semiconductors

A potential difference, called the built-in potential is generated as a result of the band bending. This is given by [8]

$$qV_{bi} = E_g - qV_n - qV_p \tag{2.3}$$

where V_p and V_n are barrier potentials between the intrinsic energy level and the fermi level in the p and n-type semiconductors.

$$V_{bi} = \frac{KT}{q} ln \left(\frac{N_A N_D}{n_i^2} \right) \tag{2.4}$$

where N_A and N_D are the acceptor and donor impurity concentrations in the p and n-type semiconductors and n_i is the intrinsic carrier concentration [8]. P-N junctions can be classified as step junctions or graded junctions depending on the doping profile. A step junction is one which has uniform p doping on one side of a sharp junction and a uniform n doping on the other side. A graded junction is one where N_D-N_A varies over a significant distance on either side of the junction.

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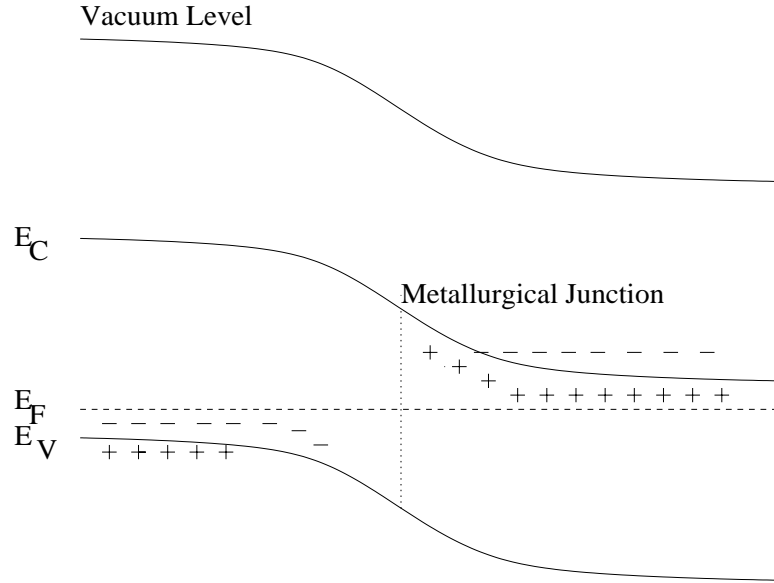
Figure 2.5 Energy Band Diagram of a P-N Junction in Thermal Equilibrium

2.3 Heterojunctions

A junction formed between two different semiconductors is called a heterojunction. Since the semiconductors have different bandgaps and electron affinities, discontinuities in the valence and conduction bands occur as a result of band bending. If these discontinuities are very large, they can adversely affect the current flow as they present a barrier to the mobile charge carriers.

Figure 2.6 shows the the energy band diagram of two semiconductor materials prior to junction formation. E_{g1} and E_{g2} are the bandgaps of two different semiconductors, ϕ_{m1} and ϕ_{m2} are their workfunctions and χ_1 and χ_2 are the electron affinities. When two semiconductors are brought together to form a junction, the energy band diagram appears as shown in Figure 2.7.

We can see that, the band bending has given rise to a spike in the conduction band. This spike called the conduction band offset, acts as a barrier that limits the electron
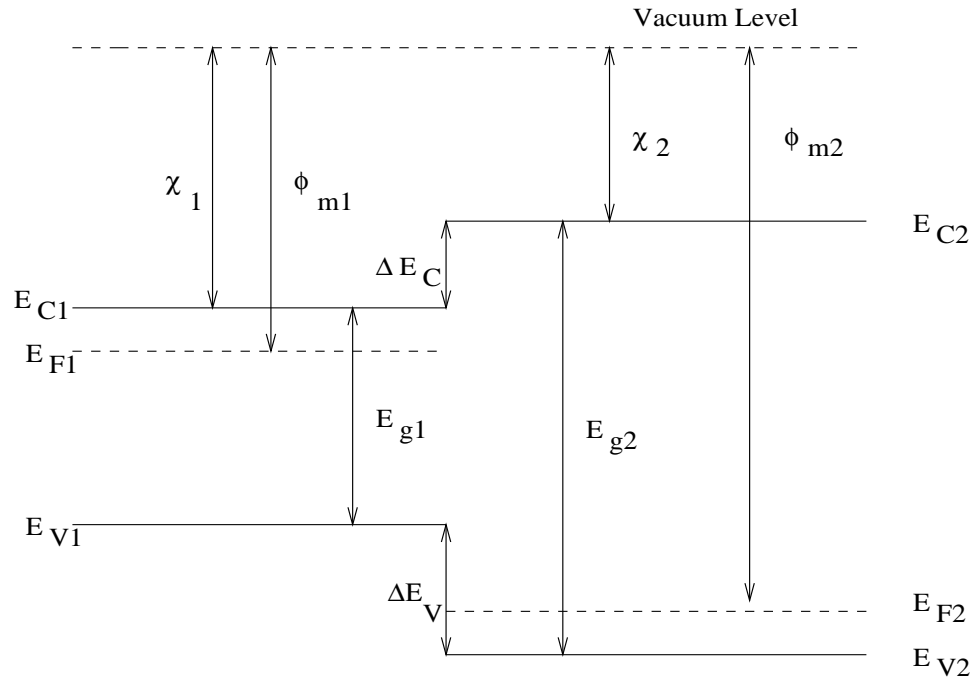
Figure 2.6 Energy Band Diagram for Two Isolated Semiconductors
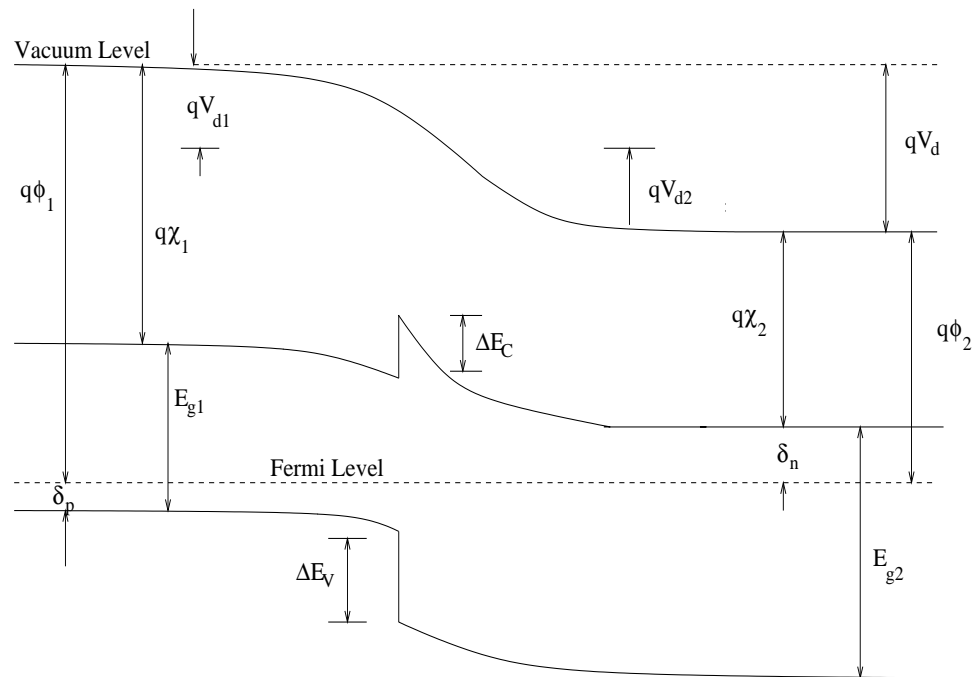
Figure 2.7 Energy Band Diagram of a Heterojunction in Thermal Equilibrium

flow from p-side to the n-side when the junction is illuminated. The magnitude of the conduction band offset is given by the equation.

$$\Delta E_c = \chi_1 - \chi_2 \qquad (2.5)$$

So in order to get optimum current flow in a solar cell ΔE_c has to be minimized by choosing an appropriate junction partner to the absorber layer. Similarly the valence band discontinuity is given by

$$\Delta E_v = (E_{g2} - E_{g1} - \Delta E_c) \qquad (2.6)$$

A heterojunction can be classified as isotype or as anisotype. In an isotype junction both semiconductors have the same type of conductivity while in an anisotype junction the conductivities are different. The $CuInGaSe_2$/CdS solar cells fabricated in this research are anisotype heterojunctions.

Heterojunction devices suffer from the problems of lattice mismatch and differences in electron affinity, resulting in interface states in the junction which acts as recombination centers. Chemical compatibility between the materials as well as stability of the fabricated junctions and the reproducibility of the physical and chemical interface are the other disadvantages of the heterojunctions. The heterojunctions also have a few advantages of their own.

The energy band diagram of a practical $CuInSe_2$/n-CdS/ZnO heterojunction solar cell structure is shown in Figure 2.8. Most of the light passes through the wide gap CdS window and onto the low bandgap CIGS (absorber) layer where it is absorbed. This structure has the advantage of reducing recombination at the front contact as most of the carriers are generated in the absorber. This is an advantage over homojunctions where high surface recombination velocity is a major loss mechanism especially at lower wavelengths. If the bandgap of the window layer is large (replace
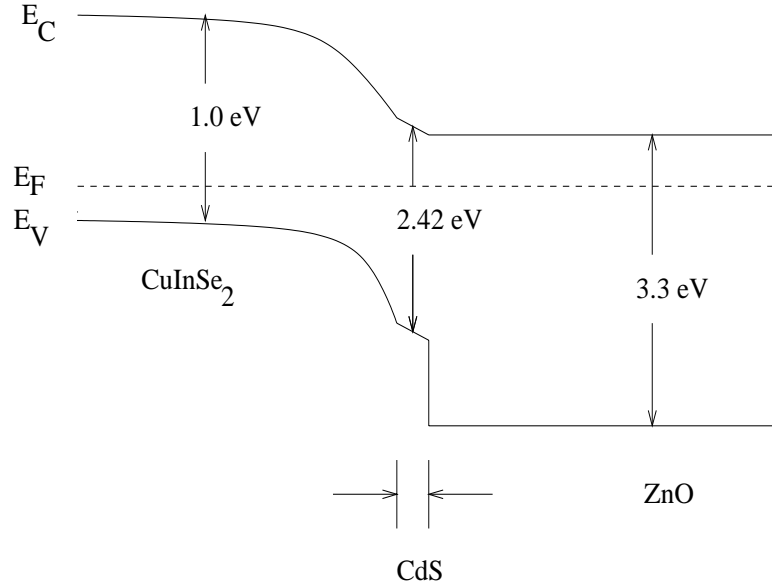
Figure 2.8 Energy Band Diagram of a CuInSe$_2$/CdS/ZnO Heterojunction Thin Film Solar Cell

CdS by ZnO) an enhanced short-wavelength spectral response is possible. This will lead to an increase in short-circuit current densities.

Heterojunction solar cells allow the use of direct bandgap semiconductors which can only be doped either p-type or n-type. The use of direct bandgap semiconductors helps in reducing costs. Heterojunctions are also a solution in overcoming surface recombination problems faced in homojunction solar cells. A lower series resistance can be achieved if the window layer is heavily doped. Heterojunction solar cells also offer better irradiation resistances.

The current transport in heterojunctions is dominated by interface phenomena [9]. The current transport in the space charge region is attributed to either recombination or tunneling or a combination of the two. The defect energy levels at the interface also aid in this current transport.

2.4   Metal Semiconductor Contacts

The contact formed between a metal and semiconductor can either be ohmic or rectifying (Schottky barriers) depending on certain conditions. The formation of an ohmic contact or atleast a quasi-ohmic contact is essential to achieve good performance in thin film solar cells. This section will briefly explain the conditions under which Schottky or Ohmic contacts are formed.

2.4.1   Schottky Contacts

2.4.1.1   Ideal Metal Semiconductor Junctions

The workfunction of a material is defined as the energy required to remove an electron from the fermi level to a position just outside the material. The band diagrams of an isolated metal (with a workfunction ϕ_m) and a n-type semiconductor (with a workfunction ϕ_s) are shown in Figure 2.9a. Let us consider the case where ϕ_m is greater than ϕ_s. When these two are brought in contact with each other, charge transfer occurs until the fermi levels align to achieve equilibrium. This results in a band diagram shown in Figure 2.9b. The case depicted here is an ideal metal semiconductor junction where there are no surface states.

In order to achieve equilibrium electrostatic potential, electrons are injected from the semiconductor into the metal. This causes a depletion of electrons from the front surface of the semiconductor leaving behind a depletion region near the junction. The depletion region is made up of ionized donors. Since the front surface of the semiconductor is less "n-type" than the bulk the bands bend upwards and give rise to a potential difference called the contact potential V_{bi}. The bending of the bands

VACUUM

$q\phi_m$

$q\chi$

E_C

E_F

E_V

(a)

$q\phi_{Bn}$

qV_{bi}

E_C

E_F

W

E_V

(b)
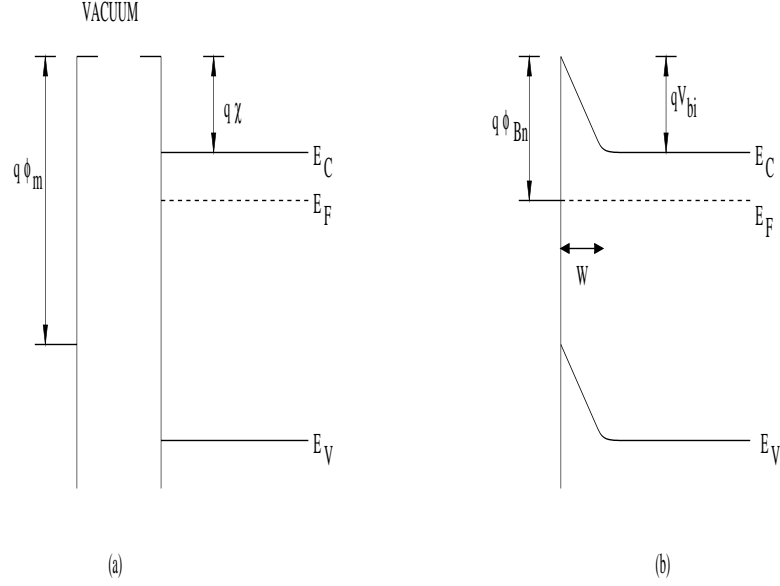
Figure 2.9 Energy Band Diagram of a Ideal Metal Semiconductor Junction (a) Before Contact (b) After Contact

results in the formation of a barrier for further electron flow from the semiconductor to the metal. The height of this barrier is given by [8]

$$q\phi_{Bn} = q(\phi_m - \chi) \tag{2.7}$$

Where χ is the electron affinity of the semiconductor. Analogously the barrier height between a p-type semiconductor and a metal in a case where ϕ_m is less than ϕ_s is given by [8]

$$q\phi_{BP} = E_g - q(\phi_m - \chi) \tag{2.8}$$

Where E_g is the bandgap of the semiconductor and χ is its electron affinity.

In summary, a Schottky contact is formed between a n-type semiconductor and a metal when the metal workfunction ϕ_m is greater than the semiconductor workfunction ϕ_s. A Schottky contact is formed between a metal and p-type semiconductor when the metal workfunction ϕ_m is less than the semiconductor workfunction ϕ_s.

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2.4.1.2 The Effect of Surface States

Let us consider a case where a large density of surface states is present on the semiconductor surface. Figure 2.10 shows equilibrium condition between the surface states and the bulk of the semiconductor.
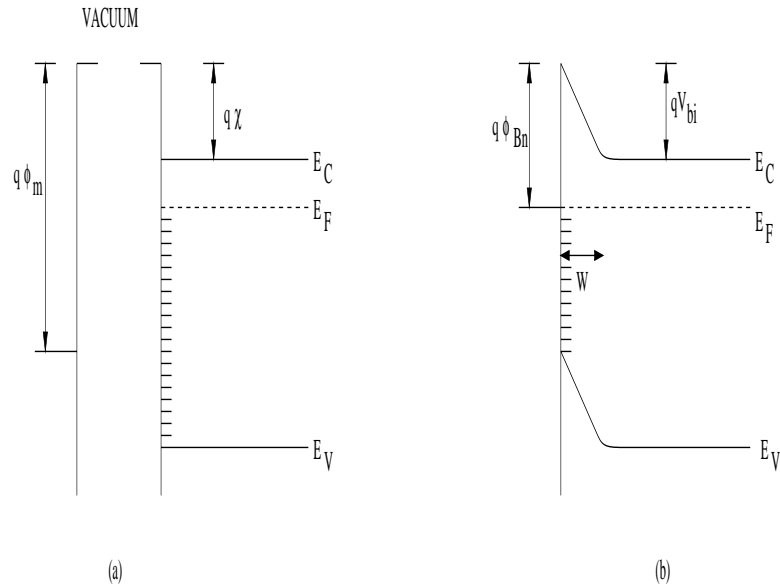
Figure 2.10 Energy Band Diagram of a Metal Semiconductor Junction with Surface States (a) Before Contact (b) After Contact

The surface states upto the fermi level E_F are filled, while those above E_F are empty. In an ideal case where there are no surface states, the negative charge on the surface of the metal (Q_m) is balanced by the positive ionized donor charge (Q_d) in the semiconductor. However, in the presence of surface states, the charge contributed by them should also be considered. If the density of the surface states is sufficiently large to accomodate additional surface charges without changing E_F, then the space charge in the semiconductor is unaffected. In this case, the barrier height becomes independent of the metal workfunction and is determined by the semiconductor surface.

2.4.1.3 Metal Semiconductor Junctions Under Applied Bias

Under thermal equilibrium, the current I_{sm}, due to the electrons flowing from the metal to the semiconductor is equal and opposite to the current I_{ms} flowing from the metal to the semiconductor. The energy band diagram under such conditions is shown in Figure 2.11(a).

(a)   (b)   (c)
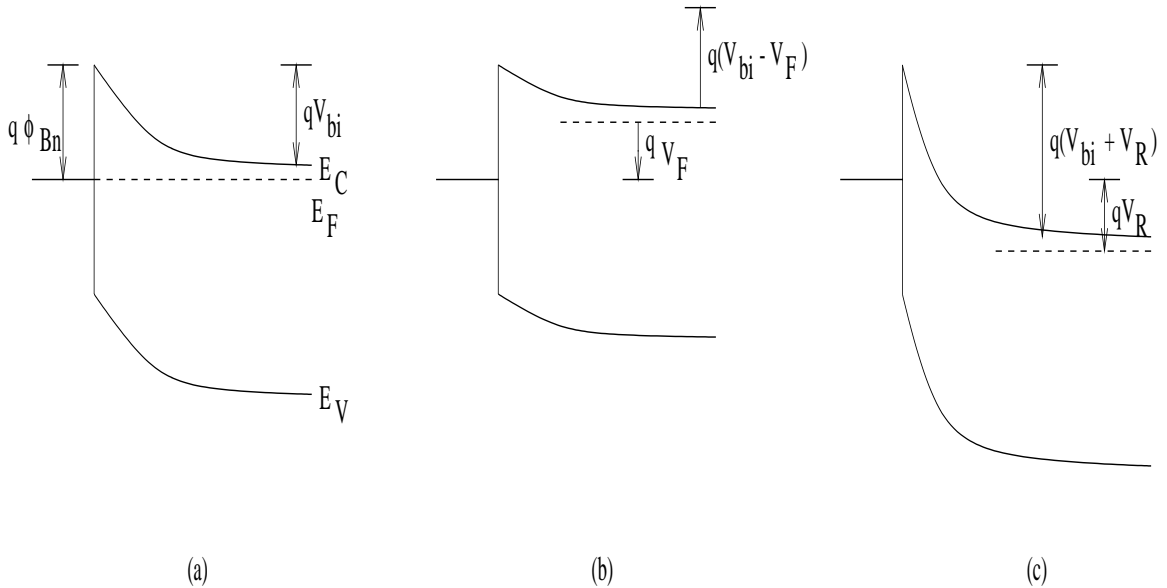
Figure 2.11 Energy Band Diagram of Metal Semiconductor Junction Under (a) Thermal Equilibrium (b) Forward Bias (c) Reverse Bias

On the application of a forward bias voltage V_F to a Schottky junction, band bending in the semiconductor is reduced. This is shown in Figure 2.11(b). This leads to a reduction in barrier height and the electrons in the semiconductor can easily overcome this barrier and flow into the metal. This leads to an increase in current from the metal to the semiconductor I_{ms}(current flow is opposite to electron flow). The current from the semiconductor to the metal, I_{sm} is constant as there is no change in electron flow from the metal to the semiconductor. Thus there is a large net current flowing from the metal to the semiconductor under forward conditions.

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When a Schottky junction is reversed biased by applying a voltage V_R to it, the band bending is increased by an amount of V_R as shown in Figure 2.11(c). So the electrons now face a big barrier and have a very little chance of overcoming it. So the current from the metal to the semiconductor is greatly reduced or negligible, while the current from the semiconductor to the metal is small and constant. So under these bias conditions a small reverse current flows from the semiconductor to the metal and is independent of the bias voltage.

The Schottky junction is a majority carrier device and current transport involves the flow of majority carriers from the semiconductor to the metal. The various transport processes under forward bias are transport of a carrier from the semiconductor into the metal over a potential barrier, quantum mechanical tunneling of carriers through the barrier, recombination in the space charge region, and recombination in the neutral region [8].

2.4.2   Ohmic Contacts

An ohmic contact is defined as a metal semiconductor contact that has a negligible contact resistance relative to the bulk resistance of the semiconductor [8]. Ohmic contacts allow equal current flow in both directions and exhibit linear I-V chracteristics. The voltage drop across a good ohmic contact should be small in comparison to the voltage drop across the actual device. Consider a case where a metal with a workfunction ϕ_m is used to form a contact to a n-type semiconductor with a workfunction ϕ_s. In the case where ϕ_m is less than ϕ_s, electrons flow from the metal to the semiconductor to enable the alignment of the fermi levels. This causes the surface of the semiconductor to be more n-type and the bands bend down. Since the majority carriers accumulate at the surface of the semiconductor, no depletion region is formed. The electrons can flow very easily from semiconductor to the metal as they do not

encounter any barrier.This is shown in Figure 2.12. Analogously, an ohmic contact is formed between a metal and a p-type semiconductor, if the metal workfunction ϕ_m is greater than the semiconductor workfunction ϕ_s.
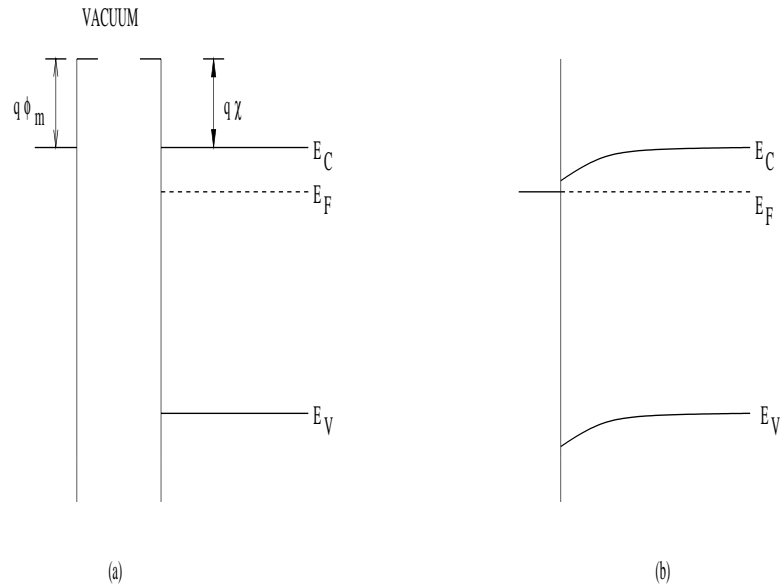
Figure 2.12 Energy Band Diagram of Metal Semiconductor Ohmic Contact (a) Before Contact Formation (b) After Contact Formation

2.5   Solar Cells

2.5.1   Theory of Operation

Solar cells utilize the photovoltaic effect wherein sunlight is converted into electrical energy. The basic operation of a solar cell depends on the absorption of photons and the subsequent generation of electron-hole pairs in the semiconductor. These carriers then diffuse to the edge of the depletion region. The electric field acting across the depletion region separates the carriers and aids in the collection of the carriers at the contact.

A solar cell consists of a thin heavily doped emitter or window layer on top of a relatively thick moderately doped base or absorber layer. The doping of the two layers

are opposite. In order to maximize the efficiency of the solar cells certain conditions or requirements have to be met [10]. The first requirement is that a major portion of the incident light is absorbed by the cell to generate electron-hole pairs. The second requirement is that the solar cell structure provide a mechanism for separating the generated charge carriers. It is also imperative that the minority carrier lifetimes are high so as to ensure good collection efficiency. This is the third requirement.

Excess electron-hole pairs can be generated either by having a absorber layer thicker than the absorption length and/or by light trapping. The absorption of light in a semiconductor is controlled by the energy of the incident photon. Absorption of light is achieved only when the energy of the incident photon is greater than the bandgap of the semiconductor. This can be summarized as follows

$$E = \frac{hc}{\lambda} > E_g \tag{2.9}$$

where h is the Planck's constant, c is the speed of light in vacuum, and λ is the wavelength of the incident radiation and E_g is the bandgap of the material. The absorption of light by a semiconductor is governed by the equation

$$I = I_o e^{-\alpha t} \tag{2.10}$$

where I_o is the intensity of light incident on the semiconductor, and t is the depth of material from surface of incidence.

The excess electron-hole pairs generated by the absorption of light are swept by the electric field present in the depletion region. This provides the required mechanism to separate the photogenerated carriers. However, most of the solar cells employ a shallow junction and thus most of the light is absorbed in the absorber. Hence most of the separated charge is made up of electrons from the absorber. A few electron-hole pairs are generated in the window layer, in the blue region of the incident light.

However, they do not contribute much to the photocurrent as a result of the heavy doping in the window layer which greatly reduces the diffusion length of the holes.

In order to achieve high carrier lifetimes, the absorber needs to have low defect densities as well as moderate doping. Higher doping results in the reduction of carrier lifetime through recombination in the bulk. The electric field in the depletion region is directly proportional to the doping concentration. So an optimum value of doping has to be chosen to achieve high enough electric fields with sufficient carrier lifetimes. This process is depicted in Figure 2.13 which shows the energy band structure of a solar cell under illumination.
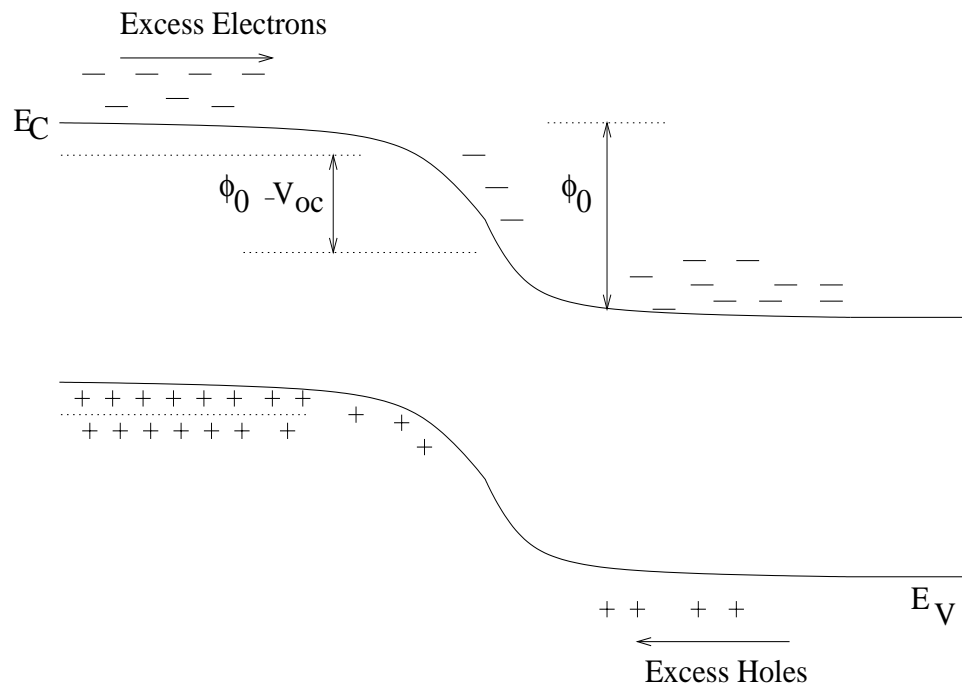
Figure 2.13 Energy Band Diagram of a P-N Junction Under Illumination

E_c and E_v are the conduction and valence band edges respectively and ϕ_0 is the built-in potential in the dark. The dotted lines represent the respective positions under illumination. The photogenerated excess charge produces a voltage across the external circuit. This voltage is termed as the open-circuit voltage of the solar cell.

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2.5.2 Photocurrent and Spectral Response

The generation rate of electron-hole pairs at a distance x from the surface of the semiconductor, due to the photon absorption of wavelength λ is [8]

$$G(\lambda) = \alpha(\lambda)F(\lambda)[1 - R(\lambda)]e^{-\alpha(\lambda)x} \qquad (2.11)$$

where $F(\lambda)$ is the number of incident photons cm^{-2}s^{-1} per unit bandwidth, $\alpha(\lambda)$ is the absorption coefficient, and R is the number of photons reflected from the surface. The term quantum efficiency(QE) can now be defined as the number of carriers collected per incident photon at each wavelength. Under low level injection conditions, the steady-state continuity equation is [8]

$$\left(\frac{1}{q}\right)\left(\frac{dJ_n}{dx}\right) + G_n - \frac{(n_p - n_{po})}{\tau_n} = 0 \qquad (2.12)$$

for electrons in the p-type material. The electron current density J_n is given by

$$J_n = q\nu_n n_p E + qD_n\left(\frac{dn_p}{dx}\right) \qquad (2.13)$$

where E is the electric field, n_p is the photogenerated minority carrier density, and n_{po} is the equilibrium minority carrier density in the dark. The hole current density is given by

$$J_p = q\nu_p p_n E - qD_p\left(\frac{dp_n}{dx}\right) \qquad (2.14)$$

The photocurrent generated in the depletion region is normally unaffected by the recombination because the electric field in this region is generally high and the carriers are quickly accelerated out of the depletion region before they can recombine. The photocurrent per unit bandwidth is equal to the number of photons absorbed. Therefore

$$J_{dr} = qF(\lambda)[1 - R(\lambda)]e^{-\alpha(\lambda)x_j}\left[1 - e^{(-\alpha(\lambda)w)}\right] \qquad (2.15)$$

where x_j is the junction depth and w is the depletion layer width. The total photocurrent at a given wavelength is then the sum of the two minority carrier currents and the depletion region current [8]

$$J(\lambda) = J_p(\lambda) + J_n(\lambda) + J_{dr}(\lambda) \tag{2.16}$$

The spectral response is equal to this sum divided by the quantum efficiency for externally observed response or by $qF(1 - R)$ for internally observed response [8],

$$SR(\lambda) = \frac{1}{qF(\lambda)[1 - R(\lambda)]}(J_p(\lambda) + J_n(\lambda) + J_{dr}(\lambda)) \tag{2.17}$$

once the spectral response is known, the total photocurrent density is obtained from the solar spectral distribution $F(\lambda)$ [8]

$$J_L = q \int_0^{\lambda_m} F(\lambda)[1 - R(\lambda)]SR(\lambda)d\lambda \tag{2.18}$$

where λ_m is the longest wavelength corresponding to the absorber bandgap.

2.5.3   Current-Voltage Characteristics

Figure 2.14 shows the I-V characteristics of a solar cell in the dark as well as under illumination. Since the solar cell is a p-n junction diode, its behavior in the dark is governed by the diode equation.

$$I = I_o(e^{\frac{qv}{AKT}} - 1) \tag{2.19}$$

The total current under illumination is given by

$$I = I_o(e^{\frac{qv}{AKT}} - 1) - I_L \tag{2.20}$$

where I is the total current, I_o is the reverse saturation current and I_L is the light generated current. Short circuit current I_{sc} is defined as the current flowing in the circuit when the load is shorted. The voltage developed by a solar cell with an infinite

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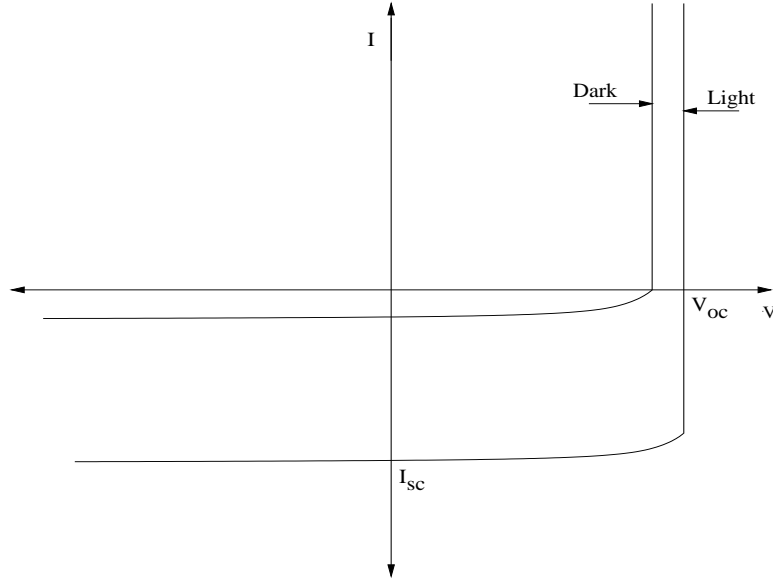
Figure 2.14 I-V Characteristics under Dark and Illumination

load attached to it, is called the open circuit voltage (V_{oc}). It is obtained by setting the total current I to 0 in the above equation. The open circuit voltage can be represented by

$$V_{oc} = \frac{AKT}{q}(ln(1 + \frac{I_{sc}}{I_o})) \tag{2.21}$$

where K is the Boltzmann's constant, A is the diode quality factor and T is the absolute temperature. A and I_o can be obtained from dark IV curves. The reciprocal of the slope of the $ln(I)$ vs V curve gives the value of A, whereas the y intercept gives J_o. These two parameters are interrelated. The value of A usually lies between 1 and 2. The highest values of V_{oc} are obtained when I_o is small. This normally corresponds to a value of 1 for A. The V_{oc} cannot be increased by increasing A as an increase in A leads to an increase in I_o thus hurting V_{oc}. Figure 2.15 shows the maximum power or an inverted I-V curve of a solar cell in the 4th quadrant.

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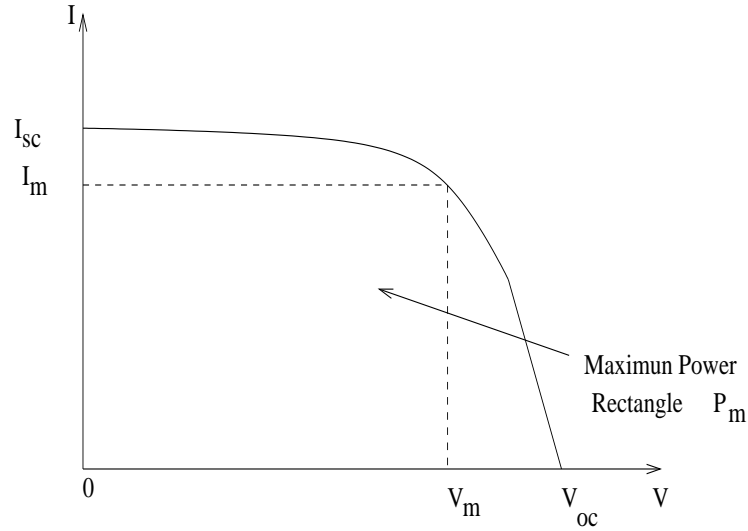
Figure 2.15 Inverted I-V Curve Showing Maximum Power Rectangle

The maximum power generated by a solar cell is given by the maximum power point, which is the product of voltage V_m and I_m. The fill factor (FF) of a I-V curve is defined by

$$FF = \frac{V_m * I_m}{V_{oc} * I_{sc}} \tag{2.22}$$

The photovoltaic conversion efficiency is defined as a measure of amount of light energy that is converted into electrical energy and is given by

$$\eta = \frac{P_m}{P_{in}} = \frac{FF * I_{sc} * V_{oc}}{P_{in}} \tag{2.23}$$

where P_m is the area of maximum power rectangle and P_{in} is the incident power.

2.5.4   Effect of Series and Shunt Resistances

An ideal solar cell has zero series resistance and an infinite shunt resistance. The equivalent circuit of an ideal solar cell is shown in Figure 2.16a.

As seen in Figure 2.16b all practical solar cells are characterized by finite series and shunt resistances. The equivalent circuit of a practical solar cell consists of a

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(a)   (b)
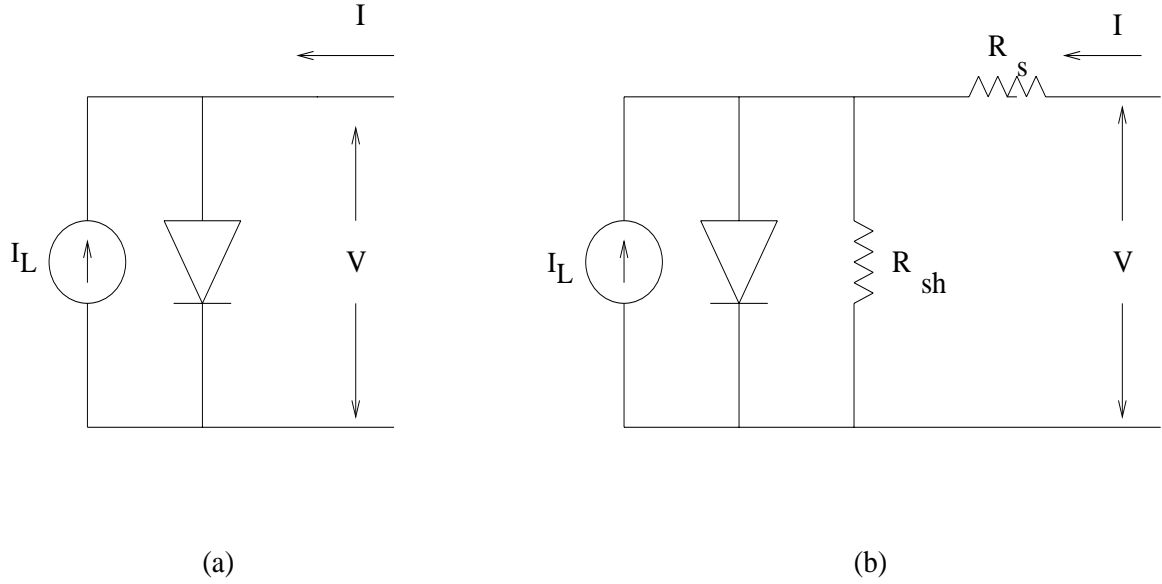
Figure 2.16 Equivalent Circuit of a Solar Cell (a) Ideal Case; (b) In the Presence of Series and Shunt Resistances

current source in parallel with a diode and a shunt resistance R_{sh}, all in series with R_s. A terminal voltage V and current I are produced in the circuit. The total current given by the ideal diode equation needs to be modified to accomodate the series and shunt resistances. The current in a practical solar cell is given by

$$I = I_o\big(e^{\frac{q(V-IR_s)}{AKT}} - 1\big) - I_L + \frac{(V - IR_s)}{R_{sh}} \qquad (2.24)$$

The series resistances R_s consists of the bulk resistance of the semiconductor, the bulk resistance of the contacts, and the contact resistance between the metallic contacts and the semiconductor. The series resistance is usually dominated by the resistance of the transparent conducting oxide(TCO), as the current flows laterally in this layer. The series resistance can be determined graphically from the I-V curve. The reciprocal of the slope of the I-V curve under high forward bias gives R_s. The effect of series resistance on the I-V curve is illustrated in Figure 2.17. As it can be seen R_s has no effect on V_{oc} and very little effect on I_{sc}. However, the fill factor is

affected by a high value of series resistance, leading to a reduction in the conversion efficiency.
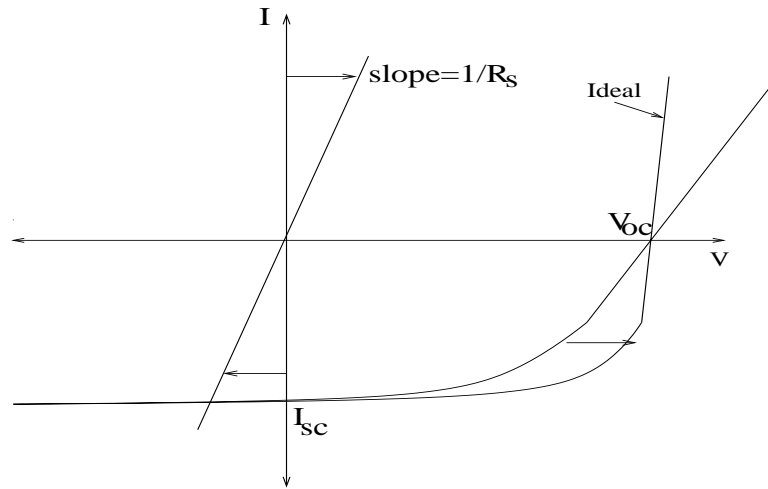
Figure 2.17 Effect of Series Resistance
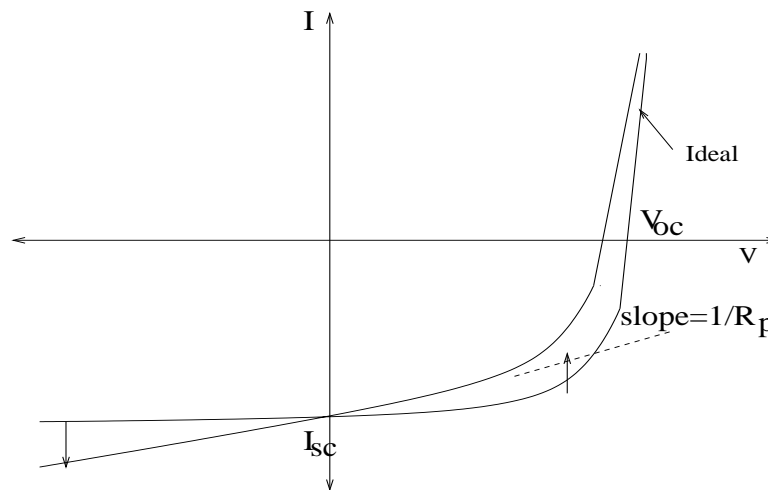
Figure 2.18 Effect of Shunt Resistance

The shunt resistance R_{sh} is lowered because of the presence of leakage paths near the junction. These leakage paths are non-uniformly distributed and can be non-linear and time varying. In addition, these shunt paths can be light sensitive leading to light induced shunting. The presence of defects like pinholes can also cause a

lowering of R_{sh}. The effect of R_{sh} on I-V curve is depicted in Figure 2.18. R_{sh} is the reciprocal of the slope of I-V curve in the reverse bias region. A low value of R_{sh} hurts the fill factor and in bad cases leads to an increased I_o. This increased I_o causes a loss in V_{oc} and hence in the efficiency.

CHAPTER 3

PHOTOVOLTAICS

3.1 Introduction

In 1839 Henri Becquerel measured a light-dependent voltage between two electrodes immersed in an electrolyte. This phenomenon is known as the Photovoltaic effect. This was also reported in an all solid-state system based on Se in 1876. Solar cells based on Se and cuprous oxide were then developed, but these demonstrated limited performance. The real breakthrough in photovoltaics came with the fabrication of a Si solar cell at Bell Labs by Chapin et al. in 1954 [1]. This was the first cell that converted sunlight into electricity with reasonable efficiency.

Irrespective of the technology being used, solar cells have certain requirement in order to be effective as terrestrial source of power. The conversion efficiencies of the solar cells need to be high. The constituent materials that make up the solar cells should be abundant and relatively inexpensive. A low cost fabrication method should be available. In addition, this fabrication method should be reproducible as well as support large area coatings. The total cost of the module/cell should be low. The total cost includes material, fabrication and maintenance costs. The cells also need to be reliable and stable over a long period of time. Finally, the constituent elements should be harmless and environmentally benign.

At present, the dominant photovoltaic technologies are based on single-crystal and polycrystalline Si. The wafers are cut from the boules grown by the Czochralksi

method. Sawing the wafers usually results in material loss. In addition, the wafer thickness exceed 150 microns. The wafers then go through a series of processing steps before being integrated into an array. A set of arrays them make up a module. The best laboratory efficiency of a single-crystal Si solar cell is 24.5% [6]. While the best Si module efficiencies are around 16% the high material costs and processing costs for these modules make the cost of electricity generation to be greater than 10c/kwh. As a result, low cost alternative based on thin-film photovoltaics are being researched widely by the PV groups.

3.2 Thin Film Photovoltaics

Thin film semiconductors based PV technology should have lower costs, as the material cost is significantly reduced, as the films are only a few microns thick. Large area coatings are also possible at high throughput and low costs. Cells can also be fabricated on low cost substrates or on flexible, light-weight substrates depending on the application. In addition, thin film compound semiconductors also support a wide variety of inexpensive processing techniques like evaporation, sputtering, electrodeposition, CVD and CSS to name a few. Thus the cost of thin film solar cells is reduced further in relation to crystalline Si solar cells.

The major problem associated with the thin film technology is that their conversion efficiencies are lower as compared to crystalline silicon. Thin film semiconductors are generally polycrystalline in nature. This means that grain boundaries are inherent in these films. The presence of grain boundaries as well as the complex defect chemistry of these materials lead to increase recombination rates of the generated carriers leading to lower efficiencies. Adhesion of films to the substrate, thickness variations, defects and module stability are the other issues of concern in regard to the thin film solar cells.

The most promising thin film technologies are those based on amorphous Si (a-Si), Cadmium Telluride (CdTe) and Copper Indium DiSelenide (CIS). Laboratory area cells have shown efficiencies greater than than 18% for $CuIn(Ga)Se_2$ [11, 12] and > 16% for CdTe [13]. However, the presence of Cd in both these technologies and the presence of Se in CIGS is a source of concern. $CuInSe_2$ modules have easily passed the EPA's toxicity tests [14]. CdTe, of the other hand, has had more difficulty in passing these tests.

3.3 $CuInSe_2$ Thin Film Photovoltaics

$CuInSe_2$ is a ternary alloy belonging to the I-III-VI class of semiconductors. It has a direct bandgap of 1.0 eV and its absorption coefficient of $3.6 \star 10^5 cm^{-1}$ [15, 16] is one of the highest reported to date. $CuInSe_2$ crystallizes in the chalcopyrite structure as shown in Figure 3.1. It is essentially a diamond like lattice made up of face-centered tetragonal unit cells. This structure is reported to help in the suppression of device degradation due to Cu migration.
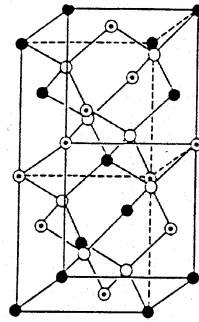
Figure 3.1 Chalcopyrite Structure of CIS

The composition of the ternary alloy CIS, strongly controls its properties. Copper rich material is generally P-type due to acceptor defects (Copper on Indium antisite

defects) and is highly conductive. On the the other hand, In-rich films are highly resistive and can be either n-type or p-type. The higher resistivities are attributed to donor defects (In on Cu antisite defects) and acceptor defects (Cu vacancies) occurring at the same time, leading to compensation. The highly conductive nature of Cu-rich CIS films is due to the presence of copper selenide between the CIS grains. The performance of Cu-rich CIS cells is poor as the Cu_2Se being highly conductive, shorts out the p-n junction. Thus the composition of the $CuInSe_2$ makes it either p-type or n-type and hence an intrinsically doped material. The low formation energy of the Cu vacancies and the existence of a shallow Cu vacancy acceptor level provides the effective self-doping ability for $CuInSe_2$ [17]. Copper poor material is generally P-type due to acceptor defects (Cu Vacancies). The films used in this research belong to the Cu-poor category. Researchers have reported the presence of a thin surface layer of $CuIn_3Se_5$ in high efficiency devices [18]. This is basically a defect chalcopyrite which is known as OVC or ODC. The OVC can be intrinsic or slightly n-type and has bandgap of 1.3 eV. This has also been identified in $Cu(In, Ga)Se_2$ devices [19].The unusual stability of the defect pair $2V_{Cu}{}^- + In_{Cu}{}^{2+}$ leads to the formation of the ODC. A periodic spatial repetition of this pair gives ODC's [17].

$CuInSe_2$ films can be fabricated by various techniques like flash evaporation [20], spray pyrolysis [21], RF sputtering from a compound target [22], electrodeposition [23, 24], and reactive sputtering in an $Ar+H_2Se$ atmosphere [25] and evaporation from elemental sources. Out of these, evaporation from elemental sources is the most widely used technique. Both co-evaporation as well as sequential evaporation of the metals are carried out to form $CuInSe_2$ absorbers. High quality films are obtained by co-evaporation of all the elements onto the substrate. The best CIS cell has been fabricated by the three stage process at NREL [26]. This cell was reported to have a conversion efficiency of greater than 15%. The co-evaporation (or the three-stage

process) requires a very high degree of control as 3 elements are evaporated at the same time. Large area coatings with uniform properties are difficult to achieve with evaporation. This makes the process unsuitable for commercial production.

CIS absorbers are also fabricated by a two stage process. In this process, metals are sequentially deposited in the presence or absence of Se. This is called the precursor formation step. In the second stage, the precursors are exposed to Se vapors at high temperature. The second stage is called the selenization step. The source of Se is either elemental evaporation of solid state Se, or the H_2Se gas. The advantages of this process is that it is much simpler and does not require a high degree of control. The films obtained are generally inferior to that obtained with the co-evaporation technique.

The metal ratio (I/III) has a significant effect on the performance of the CIS absorbers. Stoichiometric films do not necessarily give the best device performance. CIS film composition needs to be slightly In-rich to offer best performance. Metal ratios of 0.85 to 0.99 have been reported to give best device performance. This provides a wide process window for good device quality films. A strong increase in carrier concentration has been observed as the metal ratio approaches unity. This is generally attributed to the formation of Cu_2Se grains. The behavior of CIS absorber can be explained in terms of the Cu-In-Se ternary phase diagram [27] shown in Figure 3.2.

Single crystal growth takes place in a closed system. Any compositional point within the Cu-In-Se phase diagram can be achieved by using the correct amount of the constituent elements in the reaction chamber. The average composition of the resulting material will be the same as the starting ratio of the individual elements. In the thin film growth, all the delivered flux need to be necessarily incorporated into the final film. This is especially true for Se in the Cu-In-Se system. Se does not stick to a substrate at temperatures above 200°C. This in turn limits the possibility
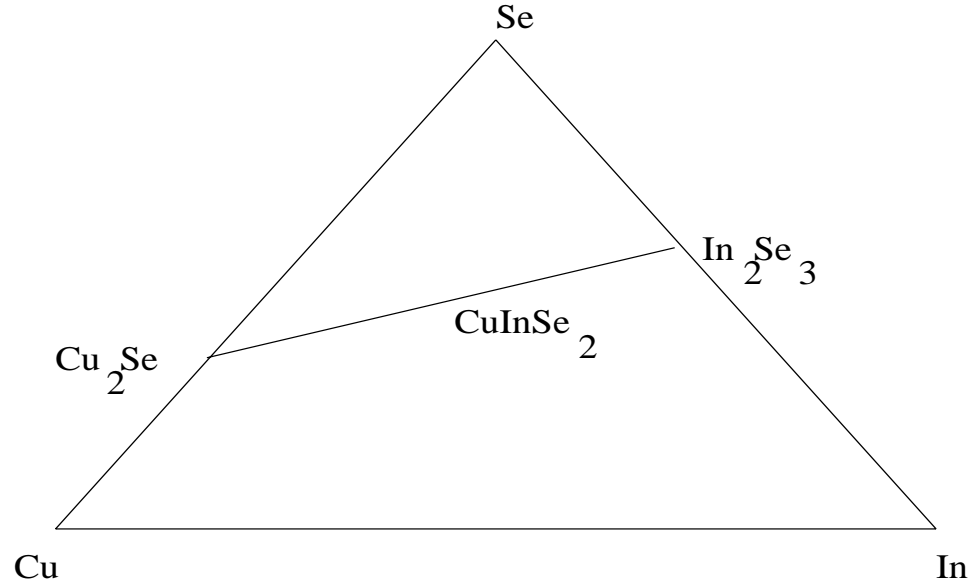
Figure 3.2 A Ternary Cu-In-Se Phase Diagram

of certain compositions in the Cu-In-Se system. Se can only be incorporated into the film at elevated temperatures by either reaction with other species delivered to the substrate or by reaction with elements already present on the substrate.

The line connecting the stable compounds Cu_2Se and In_2Se_3 is known as the pseudobinary tie line. The pseudobinary tie line contains all compositions that are stable at room temperature as well as the composition $CuInSe_2$. The Cu and In present in the film then determine the amount of Se incorporated in the film. Any excess Se is rejected from the film. This self-controlling nature of Se is an advantage in fabrication, as precise control is not needed. Low Se flux can cause removal of In through formation of volatile In_2Se species. So a overpressure of Se is used to avoid removal of material, while fabricating CIS films. Normally a Se flux which is 3 times the stoichiometric amount is used, so as to prevent the removal of In from the film.

Figure 3.3 [28] shows the Pseudobinary Phase diagram of Cu_2Se-In_2Se_3 system. Homogeneous single phase $CuInSe_2$ is seen to extend from the stoichiometric com-
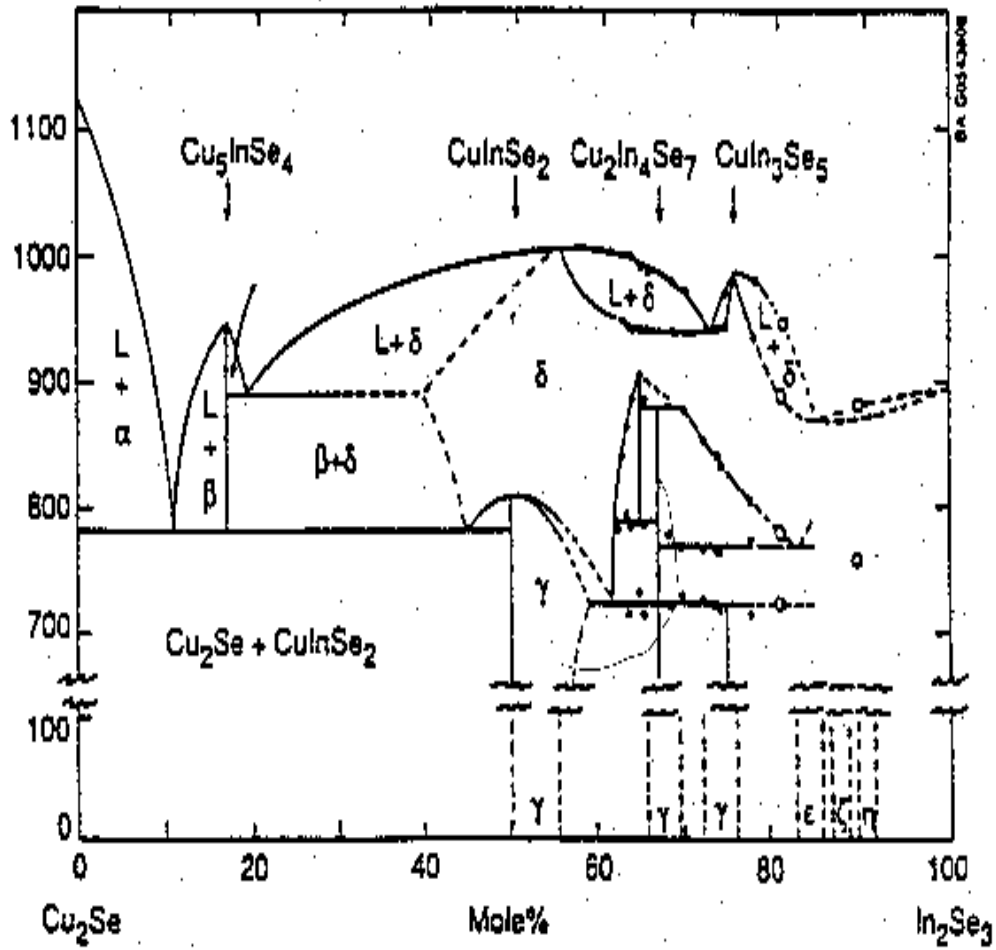
Figure 3.3 Pseudobinary Phase Diagram of Cu_2Se-In_2Se_3 System

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position of 50 mole% In_2Se_3 to a slightly In-rich composition of about 55% In_2Se_3. This corresponds to a metal ratio (Cu/In) ranging between 1.0 and 0.82. The phase diagram also shows the existence of the secondary Cu_2Se phase for Cu/In ratios exceeding unity. In Cu-rich films, the grain size is significantly larger than those of a film grown in a Cu-poor regime. The grain size is also found to be independent of substrate temperature for Cu-rich films. So different growth mechanisms are at work for Cu-rich and Cu-poor films and researchers consider it an advantage to grow films in the Cu-rich region.

Binary Phase diagrams of Cu-Se, Cu-In, In-Se are depicted in Figure 3.4[29]. The phase diagram shows that existence of liquid Cu-Se and In-Se phases at temperatures used for thin film growth. Copper is also known to selenize faster than indium and at high substrate temperatures, the formation of liquid Cu-Se phase is definitely possible [30].

3.4   Cu(In,Ga)Se$_2$ Thin Films Photovoltaics

The performance of CIS solar cells can be improved by varying the material properties as a function of film depth. The performance of CIS solar cells is limited by a comparatively lower V_{oc} due to its small bandgap. This issue can be addressed by alloying $CuInSe_2$ with $CuGaSe_2$ to produce a quarternary alloy with a higher bandgap. The increase in bandgap depends greatly on the Ga/(Ga+In) ratio. The bandgap gives higher V_{oc} as well as better matching to the solar spectrum. The V_{oc} generated by a solar cell is proportional to the band bending and the increase in the bandgap increases the band bending and hence the V_{oc}. However, there is a corresponding loss in the generated photocurrent. This is because, a material absorbs photons of energy greater than the bandgap of the material. As the bandgap increases, fewer photons are absorbed resulting in a loss of photocurrent. Thus there is a voltage-
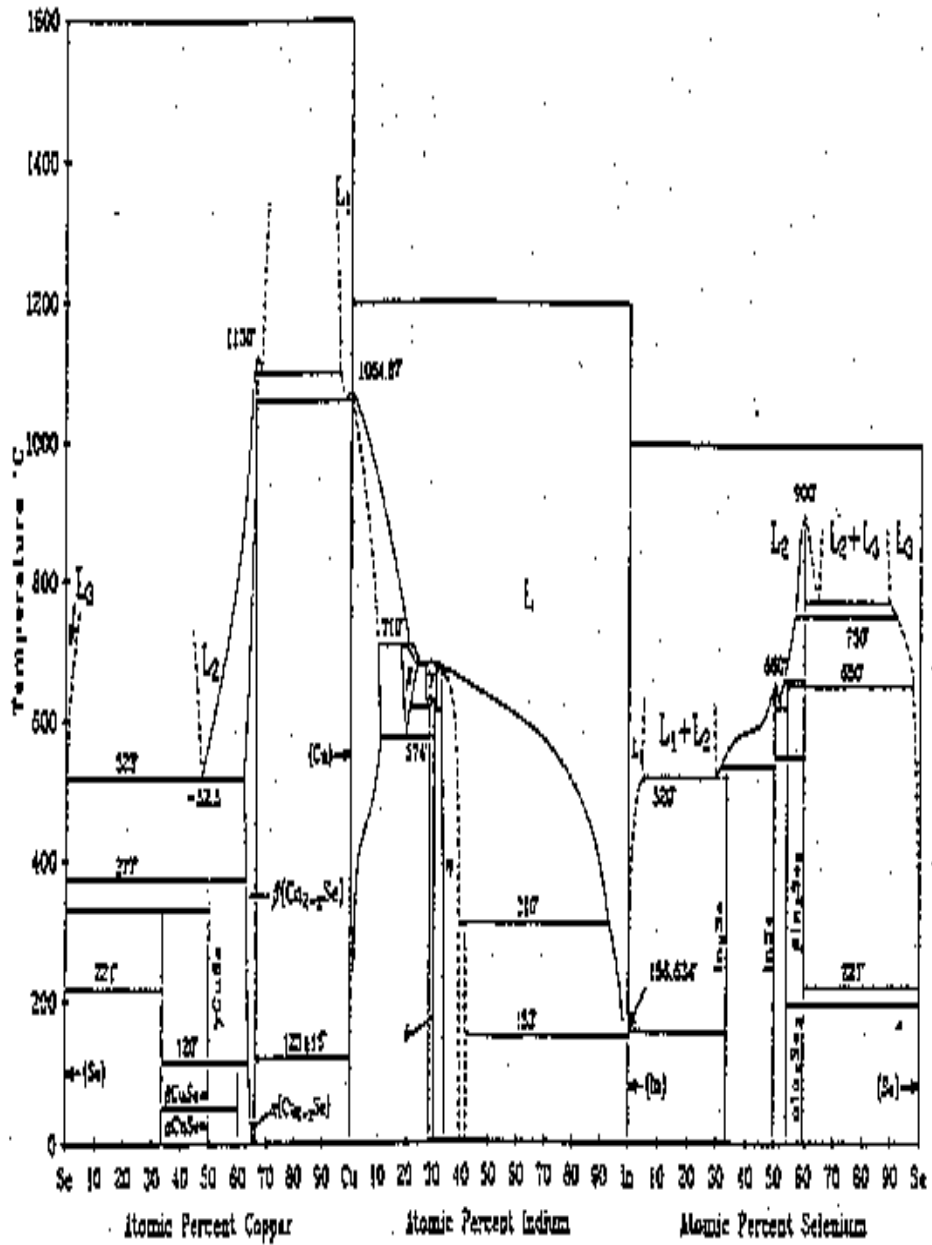
Figure 3.4 Binary Phase Diagrams of Se-Cu, Cu-In, and In-Se

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current tradeoff as the bandgap increases. The best matching to the solar spectrum is obtained for the absorbers with a bandgap around 1.4 eV [9]. Since CIS has a bandgap of 1.0 eV it is advantageous to alloy it with higher bandgap materials.

The band gap of a semiconductor produced by alloying two semiconductors tends to be linear or near linear function of the composition. Albin et al determined the band gap of thin film alloys of CIS with CGS using optical absorption measurements over a full range of composition [31]. The band gap for the composition $CuIn_{1-x}Ga_xSe_2$ is given by

$$E_g = 1.011 + 0.664x - 0.249x(1-x) \qquad (3.1)$$

For Cu-poor films there is a linear relationship given by

$$E_g = 1.0032 + 0.71369x \qquad (3.2)$$

These relations are depicted in Figure 3.5. Elemental co-evaporation has been employed to vary the band gap of $CuIn_{1-x}Ga_xSe_2$ films by changing the Ga content of the films over the entire range of composition [32].
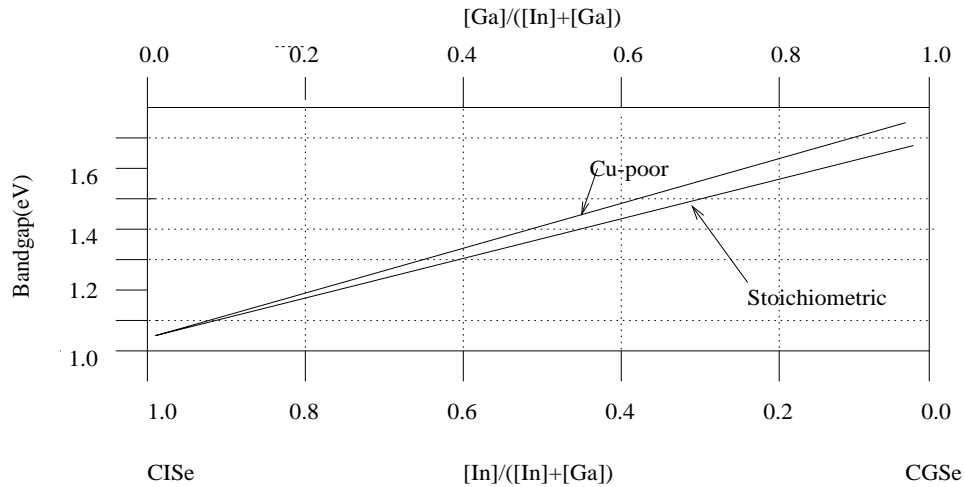
Figure 3.5 Change in Bandgap as a Function of Gallium Content for Cu - Poor and Stoichiometric Films

The addition of Ga to the CIS matrix provides other beneficial effects. It promotes the adhesion of the absorber to the Mo back contact. This has been demonstrated through tape pull tests performed on CIS films with and without Ga [33]. The carrier concentration of the absorber is also reported to increase in the presence of Ga [34]. In addition, the incorporation of Ga in CIS films aids in the carrier transport outside the depletion region through the formation of graded band gap structures. The dark current is also reduced as a result of the addition of Ga to the CIS films.

The addition of Ga to the CIS films, alters other material properties while increasing the band gap. Defect chemistry, carrier concentration, resistivity, defect levels within the gap, lattice constants, electron and hole affinities, and film morphology are all affected by the change in composition. The chalcopyrite phase(1:1:2) becomes more stable with the addition of Ga [35].

As a result of these changes, researchers have found that the there are limits to Ga incorporation, beyond which device efficiencies decrease dramatically. By increasing the band gap beyond 1.25 eV, devices without band gap grading suffer from a loss in short circuit current and fill factors while gaining little in voltage [36]. However, other researchers have fabricated good efficiency devices with high Ga concentrations near the back of the absorber [37]. Thus by engineering the Ga content throughout depth of the absorber, better overall performance can be obtained.

The variations in Ga concentration also result in changes in electron affinity and hence the conduction band offset between the absorber and the CdS also varies with the Ga concentration. Wei and Zunger [38] calculated the conduction and valence band offsets between several compounds. A summary of their results is reproduced in Table 3.1, which depicts the band offsets between these compounds and CIS and with CdS. A positive value of ΔE_c means that the conduction band of the compound is higher than that of CIS or CdS. A positive value of ΔE_v means that the valence

band of the compound is lower than the valence band of CIS or CdS. The CIS band offsets with CGS and CdS are shown in Figure 3.6.

Table 3.1 Band Offsets of Various Compounds With CIS and CdS

Compound	E_g (eV)	CISΔE_C (eV)	CISΔE_V (eV)	CdSΔE_C (eV)	CdSΔE_V (eV)
CuGaSe$_2$	1.68	0.60	0.04	0.26	-1.00
CuAlSe$_2$	2.67	1.37	0.26	1.03	-0.78
CuInS$_2$	1.53	0.21	0.28	-0.13	-0.76
CuInTe$_2$	1.01	0.47	-0.50	0.13	-1.54
CuInSe$_2$	1.04	-	-	-0.34	-1.04
CdS	2.42	0.34	1.04	-	-
ZnS	3.80	1.41	1.20	1.07	0.16
ZnSe	2.82	0.96	0.43	0.62	-0.37
ZnTe	2.39	1.26	-0.30	0.92	-1.00
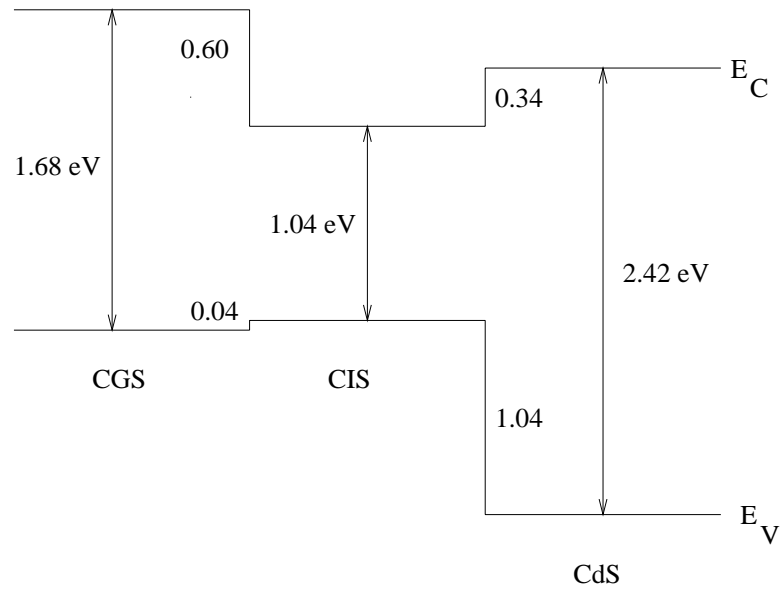
Figure 3.6 Theoretically Determined Band Lineups Between CGS CIS CdS

An expansion for ΔE_c as a function of x is obtained by using the values of ΔE_c for the CIS and CGS with CdS [39]. The relation assumes that there is no optical bowing and is given by

$$\Delta E_c = -0.34 + 0.6x \tag{3.3}$$

This relation is plotted in Figure 3.7. This may be used in the optimization of the Ga concentration at the surface of the absorber.
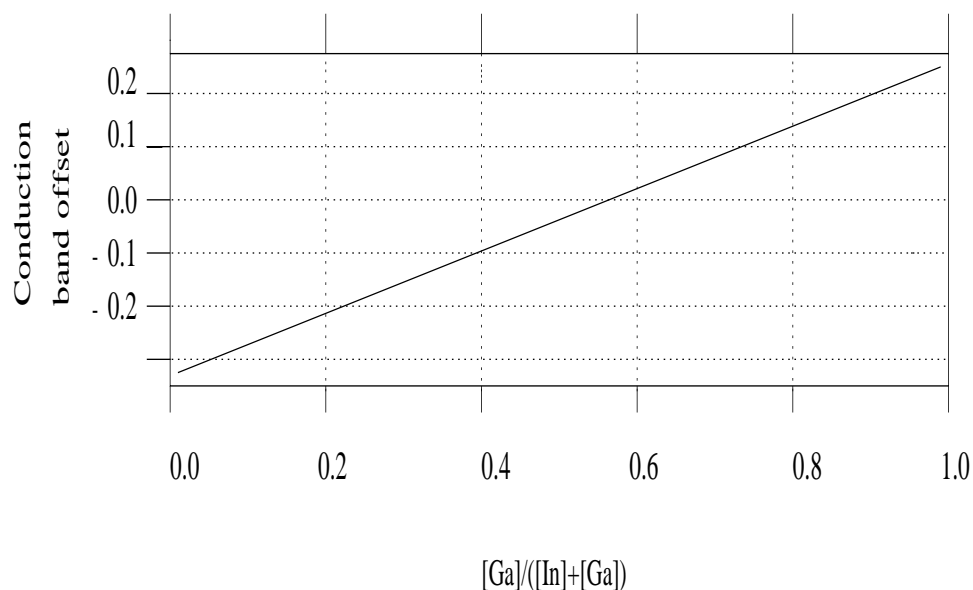
Figure 3.7 Conduction Band Offset of CIGS and CdS as A Function of Ga Content

Theoretical analysis of the effect of the conduction band offset between the CIGS and CdS have been performed by Minemoto et al [40]. They found that the short circuit density, J_{sc} is constant when ΔE_C varies from -0.7 to 0.4 eV. When ΔE_C exceeds 0.4 eV, the J_{sc} decreases abruptly. This is attributed to the fact that the photo-generated electrons cannot surmount the barrier when the barrier height exceeds 0.4 eV. The V_{oc} on the other hand, is nearly constant when ΔE_C is greater than 0 eV as there is no barrier causing recombination between the majority carriers. The

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V_{oc} decreases with increasing absolute value of ΔE_C in the range -0.7 - 0 eV, due to the formation of a "cliff" at the interface. Recombination between majority carriers through defects at the CdS/CIGS interface occurs due to this barrier. Hence V_{oc} decreases with increasing ΔE_C and defect density at the interface. The fill factors are also maximum and constant when ΔE_C is between 0 and 0.4 eV. When ΔE_C exceeds 0.4 eV, the fill factor drops dramatically due to the formation of a barrier against photo-generated electron flow. When ΔE_C lies between -0.7 - 0 eV, the fill-factor decreases due to recombination between majority carriers via defects at the window/OVC interface. So the efficiency of the cell is maximum when ΔE_C is between 0 and 0.4 eV.

The addition of Ga to the CIS matrix also enables the possibility of varying or profiling the bandgap through the depth of the material. This results in the formation of so called graded bandgap absorbers. In most absorbers without graded band gaps, the probability of collecting carriers generated outside the depletion region is pretty low. This is due to the fact that the collection relies purely on diffusion of carriers as there is no drift force acting on them, In such cases, photocurrent density suffers unless the minority carrier diffusion lengths are large. Graded band gap structures aid in improving collection of charge carriers by creating a quasielectric field. This quasielectric field helps in the collection of carriers generated outside the depletion region.

In the case where a single band gap exists throughout the absorber layer, band bending occurs only in the surface of the absorber, where the depletion region is present. The thickness of the depletion region is in turn controlled by the doping level in the absorber. So there is no electric field present in the bulk of the absorber. Hence carriers generated outside the depletion region rely on the diffusion mechanism to contribute to the photocurrent. This is a problem if the minority carrier diffusion
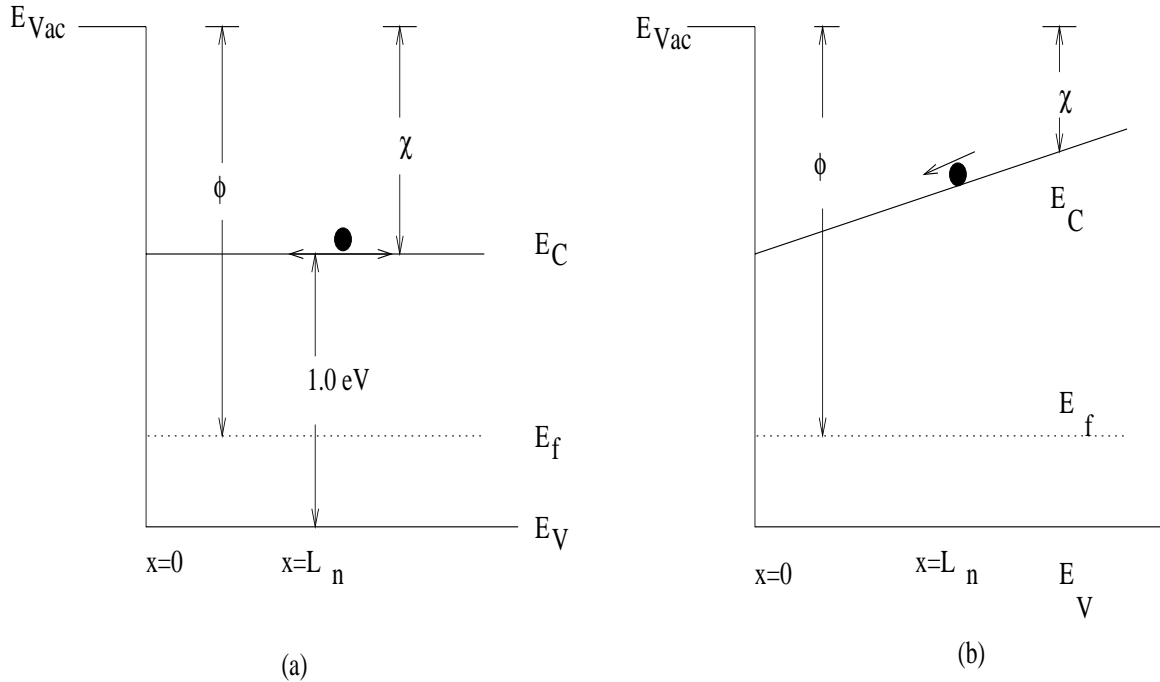
Figure 3.8 Schematic Band Diagram of (a) Homogeneous CIS (b) Graded CIGS

length is much smaller than the thickness of the absorber and can result in poor photocurrents. This case is depicted in Figure 3.8(a).

Figure 3.8(b) shows a energy band diagram of absorber with a graded bandgap. The quasielectric field created due to the bending of the conduction band helps in moving the electrons towards the junction and greatly increases their probability of collection. A bandgap grading done in a reverse direction, where the band gap continually decreases from the surface to the back of the absorber seriously hampers the collection of carriers and severely hurts the current density of the device. The tendency of Ga to segregate towards the back of the device, fortuitously avoids a band gap grading in the reverse direction.

On the other hand, abrupt changes in the band gap at the back of the absorber can result in the formation of a back surface field (BSF). BSF can be created by

highly doping the absorber near the back contact interface. This results in a nn^+ or pp^+ junction which generates an electric field in this region. This electric field can act as a minority carrier mirror and reflect minority carriers towards the pn junction to be collected. The BSF also prevents recombination at the back contact. This has been used by a few research groups [41, 42].

A notch profile has also been investigated by research groups [43], in order to improve cell performances. In the notch profile, shown in Figure 3.9 a uniform layer with a band gap of 1.2 eV is separated by a thin region with a band gap of 1.0 eV. The cell performance was found to be strongly dependent on the position of the notch. The best performance was obtained when the notch was 0.2 microns from the junction.
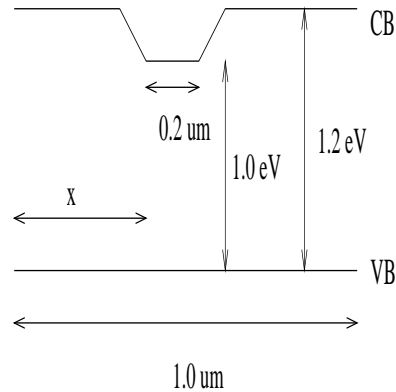
Figure 3.9 The Band Diagram of a Proposed Notch Structure

Schwartz [44] has demonstrated that the intrinsic level of the absorber can be brought below the fermi level at equilibrium as a result of the band bending at the junction. This leads to an inversion of the surface of the absorber from p-type to n-type as shown in Figure 3.10.

As a result of this type inversion, photogenerated electrons become majority carriers as they pass through this region and are thus less likely to recombine. Holes
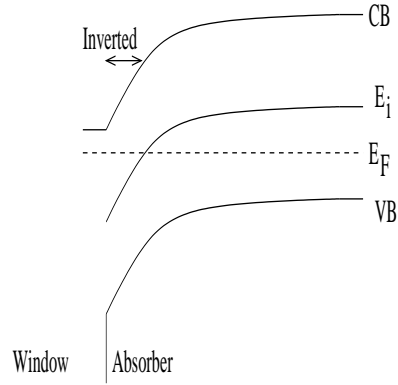
Figure 3.10 Inversion of Surface of Absorber due to Band Bending

generated in the CdS are likely to recombine at the interface and hence hardly contribute to the photocurrent.
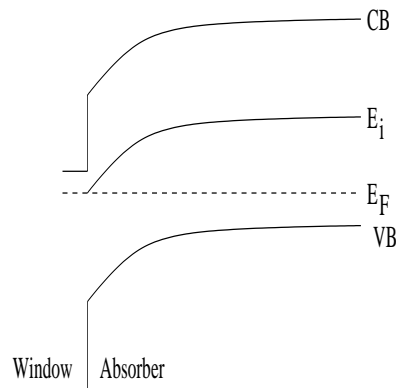
Figure 3.11 Surface Inversion Reduction due to Increased Conduction Band Offset

On the application of the forward bias, the band bending and hence the surface inversion decreases. If the surface inversion is significantly reduced before the V_{oc} point, the photocurrent and hence the fill factor will decrease [44]. Ga is thought to increase the band gap of CIS by moving the conduction band upwards. This in turn leads to larger conduction band offsets. The value of conduction band offset is then directly proportional to the Ga concentration in the film. Large concentrations

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of Ga in the film can lead to higher ΔE_c which causes a reduction in the surface inversion as seen in Figure 3.11. This can then adversely affect recombination. A large and positive ΔE_c can be tolerated if the interface does not have high density of defects. This was shown by simulations performed by Turner [45]. Researchers have also reported that the existence of a higher concentration of Ga makes n-type CIGS less likely. Thus the concentration of Ga near the interface is critical in determining device performance.

CHAPTER 4

DEVICE FABRICATION AND CHARACTERIZATION

4.1   Device Structure

Figure 4.1 shows the basic device structure of a CIGS/CdS/ZnO solar cell. The devices are fabricated by a sequential deposition of various layers that constitute the solar cell. These cells belong to the so called substrate type solar cells where light is incident on the cell through the top (ZnO) layer.

ZnO (0.5 microns)

CdS (0.02 microns)

CIGS(2.0 microns)

Mo(1.0 microns)

Glass (2mm)
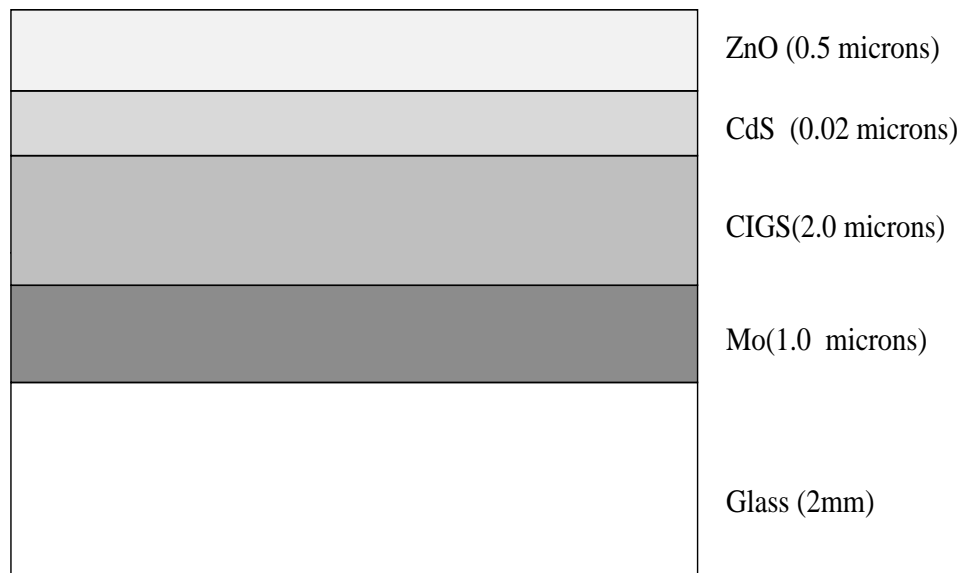
Figure 4.1 Device Structure of a CIGS/CdS/ZnO Solar Cell

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4.1.1 Substrate

Glass substrates find widespread use in CIGS solar cells due to their low costs and corrosion resistance. Defects (scratches) on the substrate can find their way into the back contact and into the absorber layer during subsequent processing, thereby hurting device performance and conversion efficiencies [46]. Higher quality glass and minimal handling are essential to overcome the above problems. Ordinary soda lime glass is the preferred choice, due to its low cost and the hypothesis that the diffusion of Sodium from the glass seems to help in the performance of these cells. The Sodium incorporation into the absorber seems to improve the fill factors and the open circuit voltages [47]. The resistivity of CIGS films deposited on Na free glass is very high for all substrate temperatures, while the resistivity of CIGS on soda lime glass is very low when the film is deposited at high substrate temperatures [48]. It is reported that sodium diffusion is reduced or blocked for temperatures below 450ºC. So the sodium from the glass helps in doping the CIGS films and improve its conductivity. It has also been reported that the absence of Na in the substrate promotes the formation of In_{Cu} compensating donors hurting the V_{oc} and FF of the device [49]. Another research group has shown that the Na impurities are mainly located at the buried CIGS/CdS surface [50] and thus play an important role during the formation of the heterojunction.

Preheating of Mo coated glass substrates have been done in an effort to control the amount of Na diffusion into the CIGS films [51]. Sodium incorporation is also found to increase grain size and P-type conductivity. An increased grain size and a better morphology implies that Na plays an important role during film growth [52]. They have also shown that the incorporated Na is mainly located at the grain boundaries of polycrystalline CIGS films.

Excessive Na is reported to have detrimental effect on the adhesion of CIGS films [53]. Hole density increases dramatically at high Na concentrations (>1 at%) which greatly reduces device performance [54]. Contreras et al. [55] have proposed that Na is incorporating substitutionally in the CIGS lattice. They claim that Na neutralizes donor states by preventing the occurrence of In_{Cu} antisites. They also report that the increase in conductivity due to Na, depends on the Cu content of the film and that the conductivity increase in very poor Cu films is limited. Another research group suggests the capacitance increases with increasing Na concentration. This is attributed due to grain boundary passivation or reduced compensation within the grains [56]. Sodium is also believed to catalyze oxygen-induced Se deficiency passivation along with the minimization of oxygen-induced Cu removal [57]. Sodium is also thought to catalyze the oxidation of In near V_{Cu} [58]. Though favorable, this Sodium diffusion introduces an uncontrollable variable affecting the run to run reproducibility. The processing temperature is also limited as high temperatures ($> 600^o$ C)induce stresses leading to softening and finally warping of the glass.

4.1.2 Back Contact

The most widely used material for the back contact in CIGS solar cells is Molybdenum(Mo). The ability to form good ohmic contacts and a high resistance to Selenium corrosion are the reasons for the widespread use of Mo. A 1 micron thick Mo layer is usually deposited by DC Magnetron sputtering and the film properties are determined by the process parameters. The sputtering pressure determines the electrical resistivity and the adhesion of the film to glass [47]. Films deposited at higher pressures exhibit a rough surface morphology and poor resistivity due to stresses and a large number of voids. However, these films have good adhesion to glass. As the sputtering pressure is lowered, the films exhibit a smoother surface. The grains are more closely

packed with fewer voids resulting in lower resistivities. These films however suffer from adhesion problems due to compressive stresses.

In order to achieve good electrical properties and good adhesion to glass a compromise in sputtering pressure is required. On the other hand, a bilayer process can be used to achieve good adhesion and good resistivity [59]. The first layer is deposited at higher pressure for improved adhesion followed by a lower pressure layer to achieve good resistivity. Surface roughness of the Mo needs to be monitored as this can lead to a rough absorber layer whereby shunt paths are introduced in the junction hurting device parameters.

The absorber layer is then grown on the Mo back contact. The properties of absorber material were discussed in chapter 3.

4.1.3   Cadmium Sulfide

A very thin layer of cadmium sulfide forms the n-type junction partner of CIGS based solar cells. Polycrystalline CdS films have the wurtzite structure as shown in Figure 4.2. CdS is a direct bandgap semiconductor and absorbs high energy photons(blue light) of the visible spectrum due to its relatively large bandgap of 2.4 eV which corresponds to an absorption edge of around 510 nm. These absorbed photons can also contribute to the photogenerated current. The CdS acts as a window layer for low energy photons, which are then absorbed in the absorber layer so as to generate current.

Chemical bath deposition(CBD), closed spaced sublimation(CSS) and RF sputtering are the techniques available for CdS deposition. CBD is the most widely used one as it gives a good uniform film even on rough surfaces. Secondly, it eliminates the need of vacuum equipment as well as the associated damage involved in the CSS and sputtered films.
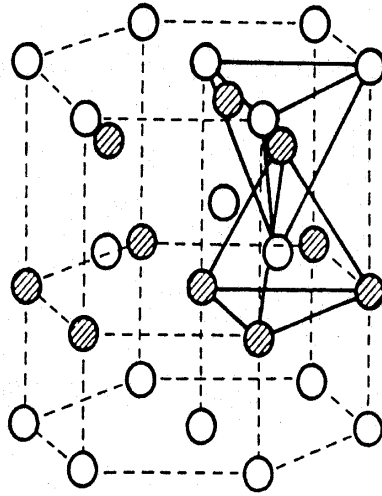
Figure 4.2 Wurtzite Structure of CdS

Solution grown films have a cadmium source like cadmium acetate, a sulphur source like thiourea and a complexing agent like ammonium hydroxide. The deposition temperature and the pH of the solution as well as the absorber surface determine the growth rate of the film [60]. Heterogeneous nucleation of CdS results in good uniform films, while homogeneous nucleation of CdS leads to powdery deposits which is highly undesirable. Homogeneous reaction can be prevented by stirring the solution as well as by controlling the temperature and pH of the solution. It is also observed that CIS is etched by ammonia, resulting in an insitu cleaning of the absorber surface [61]. In addition to forming a n-type partner to the CIGS, the CdS layer also protects the underlying absorber during the subsequent ZnO deposition.

The CdS thickness is believed to control device performance [62]. A sufficiently thick (600-800$\mathring{A}$) layer is required to obtain high V_{oc} and FF values. The mechanism involved in improved device performance is through a reduction in SCR recombination with increased CdS thickness. The V_{oc} was also found to increase with an increase in

the concentration of thiourea used in the CBD bath [63]. They also found an increase in V_{oc} with thicker CdS films. The increase in concentration of the bath constituents leads to the undesirable effect of cross over between the light and dark I-V curves. The good performance of CIGS solar cells with CdS buffer layers has been attributed to the Cd doping of the CIGS film [64]. The diffusion depth of Cd atoms is related to the Cu deficient region in the CIGS thin films [65]. Furthermore, the diffusion of Cd atoms is easier in $CuIn_3Se_5$ than in $CuInSe_2$. The CBD CdS is also reported to restore the band bending at the interface [57].

Since some amount of light is absorbed in the CdS, a current loss of approximat ely 6 mA /cm^2 is estimated for AM 1.5 global spectrum at 100 mW/cm^2 equivalent intensity [66]. Higher bandgap materials are being investigated to replace the CdS buffer layer so as to tap this current in the blue region which can lead to higher device efficiencies. Reasonable success has been reported in this quest. Materials like $Cd_xZn_{1-x}S$, ZnSe, $ZnIn_xSe_y$ hold a lot of promise. A thin buffer layer of large bandgap ternary compound $Cd_xZn_{1-x}S$ together with ZnO is reported for CIGS devices with efficiencies of 12.5 % [66, 67]. Cadmium partial electrolyte experiments have been carried out and good efficiencies have been achieved [62]. In order to eliminate the toxic Cd buffer layer, compounds like ZnSe, $ZnIn_xSe_y$ and In_xSe_y have been explored with efficiencies around 13 % [68, 69]. ZnO by reactive sputtering has also been tried as the window layer and the initial results have been encouraging [70]. CBD ZnS buffer layers also seem to be promising with a highest reported efficiency of around 17% [71, 72]. ZnO buffer layer deposited by ALD has shown an efficiency of 13.2% [73]. Cells employing sputtered ZnMgO buffer layers have recently shown an efficiency of 16.2% [74].

4.1.4 Zinc Oxide

High conductivity and transparency to incident photons are the chief requirements of a material to act as a front contact. ZnO is the most widely used material for this purpose. ZnO is a wide bandgap(3.3 eV) material and exhibits good optical and electrical properties and is typically n-type. It can be deposited by a number of techniques like sputtering, CVD etc.

A thin intrinsic ZnO layer(about 500 $\mathring{A}$) is deposited between the CdS and doped ZnO layer. The undoped ZnO layer is usually deposited by RF sputtering from a ceramic(ZnO) target in an Ar/O_2 ambient. The doped layer is deposited from a mixed ZnO:(2 wt%)Al_2O_3 target in an Argon ambient.

The amount of doping is a tradeoff between the electrical and optical properties. A transmission of 90% in the wavelength range of 400-1000 nm along with a resistivity of $9 \star 10^{-4}$ ohm-cm has been achieved. Transmission drops off at higher wavelengths due to the free carrier absorption which increases with the amount of doping. Usually an anti-reflective coating is deposited on the ZnO to reduce optical reflection losses. A typical transmission curve is shown in Figure 4.3.

4.2 Device Fabrication

A brief description of the sequence followed for device fabrication is presented in this section. A thin layer of Mo is first deposited by DC sputtering followed by the formation of CIGS absorber layer by a two stage process. The first stage is the deposition of the precursors, Cu, In, Ga, and Se followed by a selenization step to finish the absorber layer. A thin layer of CdS is then grown by chemical bath deposition. This is then followed by the deposition of a thin layer of intrinsic ZnO and a thicker layer of Al-doped ZnO by RF sputtering.
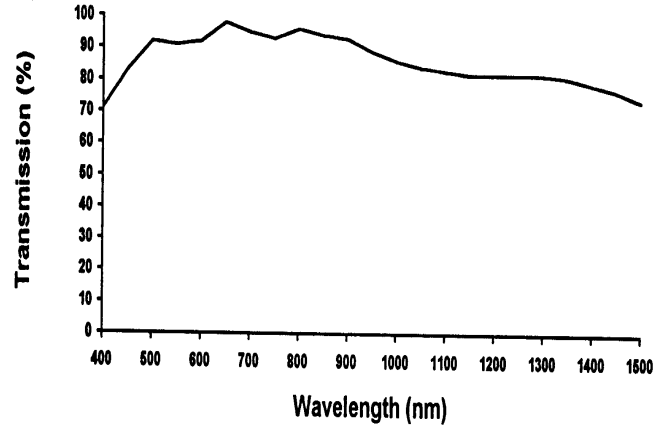
Figure 4.3 Transmission of a ZnO Film

4.2.1 Back Contact Deposition

A 5 cm⋆5 cm⋆ 2mm soda lime glass serves as the substrate. The cleaning of the substrate is very critical to ensure the removal of contaminant molecules. The substrate is soaked in a detergent-DI (deionized) water bath and scrubbed to remove any particulates. This is then followed by several rinses in DI water. To hasten contaminant, organic compound removal and the residual detergent an ultrasonic treatment is done using either trichlorotrifluoroethane or propanol. The substrates are rinsed again in DI water and placed in a hot water bath with Nitrogen gas bubbled through it. The glasses are then blown dry using compressed nitrogen.

A 1 micron thick Mo layer is deposited on the glass by DC magnetron sputtering. The glasses are heated to 150° C, prior to deposition, to remove any moisture. The chamber is pumped down to a base pressure of < 5 μtorr. A bilayer Mo film is deposited at Argon pressures between 2 and 10 mT. The resultant Mo films exhibit a smooth surface and have resistivities of the order of $5\star10^{-5}$ ohm-cm. The sputtering

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pressure, deposition rates and the discharge voltage need to be monitored carefully to produce reproducible films of high quality. These parameters have been found to have a significant impact on device performance.

4.2.2 Absorber Layer Formation

Co-evaporation of metals from elemental sources at high substrate temperatures has been a proven technique for absorber layer processing for small area high efficiency devices. NREL has developed a complex three step process for their high efficiency devices [75]. A high degree of control is needed in such a process as there is a change from (In, Ga) rich phase to a copper rich phase and then to a slightly copper poor phase at high temperatures (560° C). The degree of control in co-evaporation has a direct bearing on the device performance. In our opinion, this technique is limited to small area cells as evaporation from elemental sources is not suitable for large area coatings as composition uniformity cannot be maintained. A more suitable process for commercial production would be a two step process which involves sequential deposition of metal layers from individual sources and a high temperature anneal step in Se vapor.

Large area coatings with a high throughput and compositional uniformity can be obtained by sputtering from metal targets. In addition, only a small degree of control is needed because of the self-controlling nature of the Se flux at high temperatures. This was the main motivation in pursuing a two step process for the absorber layer formation. A precursor is formed at a substrate temperature of 275° C, by the sequential deposition of Cu and Ga followed by the co-evaporation of In and Se from elemental sources. In the past, the Ga was deposited by sputtering which is unique as it is a liquid at room temperature. This ensures easy scalability of the process. The Ga is being evaporated at present. Co-evaporation of In and Se is not essential

and the co-deposition can be carried out by sputtering from a compound target. The substrate temperature is then slowly ramped up to 550 ^{o}C in the presence of Se flux to selenize the precursor and ensure the formation of CIGS.

An ideal CIGS film is single phase with large grains and minimum defects. The grain size of the film depends on the processing details. Stoichiometric or In rich films have a small grain structure if the film was In-rich throughout the entire processing sequence. The small grain size does not hamper the current collection as the carrier mobilities are not affected [8]. However, open circuit voltages and fill factors are affected, as a small grain size implies larger grain boundaries, and leads to an increased interface recombination of the charge carriers. There could also be a segregation of additional phases between the grains around the grain boundaries whereby shunting paths to current flow are introduced.

If the films are processed with slightly Cu-rich compositions, the final film exists as a two phase mixture of CIGS +Cu_{2-x}Se with significantly larger grain size [39]. It is believed that when the film is processed in a Cu-rich regime, the excess Cu exists as a liquid phase at sufficiently high temperatures ($> 500^o$ C) and is believed to aid in mass transfer to CIS grains resulting in a densely packed, large grain structures. The excess Cu_{2-x}Se segregates to the surface and being highly conductive shorts out the junction. This excess Cu rich phase can be removed from the surface of the film by means of a cyanide solution treatment without affecting the CIS matrix [46]. Another study has reported that excess Cu can be dissolved in CIS crystallites and can act as a point defect source within the grains of the film [76]. Hence a Cu rich composition is undesirable and must be avoided to achieve good device performance.

The substrate type and growth temperatures influence the orientation of the CIGS films. CIS normally has a preferred orientation of 112. NREL has fabricated CIGS films with a 220 orientation which has resulted in cell efficiencies reaching 18.8% [11].

The interface between the 220 films and the CdS is believed to have a lower density of defect densities, leading to higher V_{oc}'s and FF's. The 220/204 orientation can be achieved only on selected Mo/SLG substrates. The Mo layer in these substrates is dense, almost free of pinholes and nearly free of sodium in its surface [77]. Sodium, when present at a critical level can hinder the formation of 220 oriented films. The 220/204 preferred orientation is obtained for Cu poor films. Cu rich films under similar growth conditions tend to be randomly oriented. This then suggests that copper selenide phases present during growth of Cu rich CIS hinders the attainment of the (220/204) preferred orientation. In devices with high quality absorbers, diffusion lengths are comparable to the absorber thickness. In such cases, back-contact recombination is a dominant loss mechanism. The presence of a $MoSe_2$ layer between the Mo and CIGS films seems to be essential in the formation of a good ohmic contact [78]. This could be because of the fact the $MoSe_2$ layer provides a back surface field because of its wide bandgap.

A two step process consists of a precursor formation step followed by a selenization step. In the precursor formation step, the metals Cu, In and Ga are deposited with or without Se at low temperatures (275° C). In the selenization step, they are reacted with Se at high temperatures (up to 550^oC). The film is processed throughout in a Cu-poor regime to prevent the formation of the highly conductive Cu-rich phases in the final film. In_2Se and Ga_2Se have a high vapor pressure at all temperatures and the removal of excess In and Ga from the surface of the film can be accomplished if the film is exposed to a low Se flux at high temperatures.

The precursor can be formed with slightly In, Ga rich compositions and then any excess In and Ga can be removed from the surface during the selenization step using a time-temperature profile. The attempt to remove the excess In and Ga from the surface is based on the assumption that if not removed, they may precipitate around

the grain boundaries and hurt the performance of the device. In this recipe the metal ratios are fixed once the precursor is formed. Another approach to resolve the issue of excess In, Ga is to deposit a thin layer of Cu during selenization to convert any excess In, Ga into CIGS compound [79]. This is the approach we have decided to pursue in this research.

4.2.2.1 Precursor Formation-Four Source Evaporator

In order to isolate the metal ratio effects from the Se flux gradient effect, the metal sources were placed on the four sides of the substrate so that two different gradients exist on the substrate along two perpendicular directions as shown in Figure 4.4. The cell numbering on the substrate is also shown in the figure. Shields were introduced between the sources so as to minimize, if not eliminate , the cross contamination of sources during deposition.

The Cu/In ratios change by about 20% along the vertical direction from the top to the bottom of the substrate. The metal ratios can be easily optimized based on the device performance. The Se flux also exhibits a gradient, as the Se boat is placed away from the edge of the substrate. Two quartz crystal thickness monitors are employed, one of which was placed near one edge of the substrate over the Ga source to monitor the metals, Cu, Ga, and In depositions and the second was placed over the Se source to monitor the Se flux. Shields were used on the crystal monitors to minimize the cross-talk during the co-deposition of In and Se.

A Se containing precursor is first formed which is subsequently exposed to Se flux at high temperatures. The efforts were concentrated on the sequence Mo/Cu/Ga/In, Se out of all possible sequences. This precursor maintains the CIS bandgap in the space charge region and results in high current devices. This sequence will be referred to as the Type I precursor. A few experiments were carried out using the sequence

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Cu

```
 1    6   11    16   21
Ga                        Se    Se                        Ga
 5   10   15    20   25
```

In

(a)   (b)

Cu
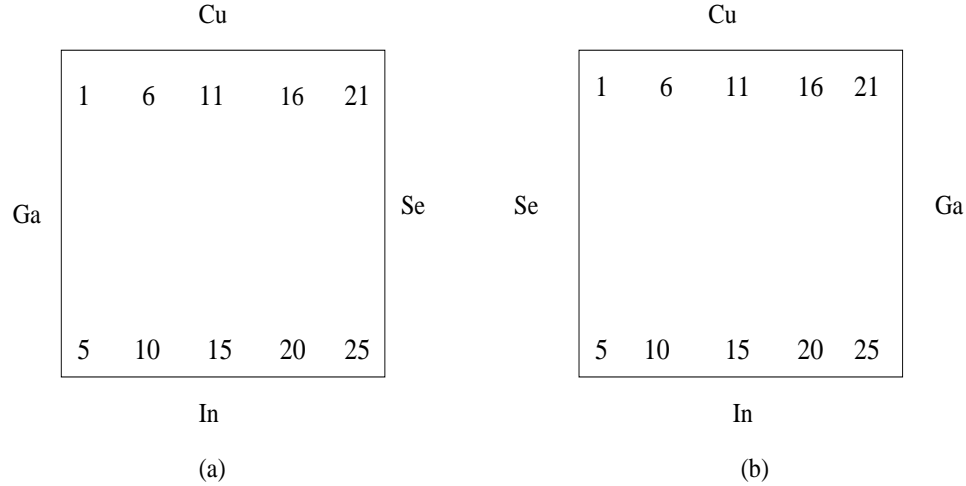
Figure 4.4 Source Arrangement (a) Evaporated Ga (b) Sputtered Ga

$Mo/In_2Se_3/Cu/Ga$. This precursor will be referred to as the Type II precursor. A third type of precursor was fabricated using the sequence $Mo/In_2Se_3/Ga/Cu$. This will be referred to as Type III precursor. Type II and III precursors have a higher bandgap due to the incorporation of Ga in the space charge region.

The metals are deposited at a relatively low temperature of 275° C to complete the formation of the precursor. A constant and high Se flux is maintained during the In_2Se_3 deposition. The substrate temperature ensures that the incorporation of Se is only due to its reaction with In or with Cu and Ga already present on the substrate. Any excess Se just bounces off the substrate at these temperatures. A constant rate of 1.2 $\overset{\circ}{A}$ /sec is maintained during the copper deposition. This corresponds to a rate of 1.3 $\overset{\circ}{A}$ /sec on one edge of the substrate and 1.1 $\overset{\circ}{A}$ /sec at the opposite edge. The In deposition corresponds to a rate of 3.2 $\overset{\circ}{A}$ /sec at the bottom and 2.8 $\overset{\circ}{A}$ /sec at the top of the substrate. This results in Cu/In ratios ranging from 1.18 on the Cu side to 0.9 on the In side. It is observed that a Se flux during In_2Se_3 deposition, which is three times that needed for the formation of stoichiometric films, is essential for good films [80]. It was also determined that any Se flux greater than this amount

was not detrimental to the film properties. Ga was initially deposited by sputtering at a constant rate of 0.6 $\mathring{A}$ /sec in regions near the source and at 0.5 $\mathring{A}$ /sec at the far edge. At present, Ga is evaporated at a constant rate of 1.0 $\mathring{A}$ /sec.

4.2.2.2 Precursor Formation-Inline Evaporator

The system used to fabricate the precursors described in the previous section was sufficient in the initial part of this research. We eventually realized that our experimental capabilities were hampered by the system. The chamber walls and all the chamber structures were coated with selenium. This caused problems during copper deposition, as the Se started to come off from chamber structures surrounding the Cu boat as the boat was heated. The amount of Se varied from run to run and depended on the chamber condition and run sequence. This Se background was an uncontrollable variable, which affected our ability to deposit pure metals. The system also provided only a limited amount of control and hence a new system was built to overcome this problem.

The new system is an in-line evaporator consisting of two vacuum chambers and a load-lock attached to them. Substrate transfer from the load-lock to the chamber is achieved using a magnetically coupled arm. The chambers themselves are fitted with linear drive motors to which two prongs and a thermocouple are attached. The two prongs grab the graphite substrate holder during the transfer process. The presence of the motors gives us the ability to move the substrate during deposition, if needed. This will be useful if we want to have a uniform film without any compositional gradients. Substrate heaters of high purity boron nitride, are attached to the substrate holding mechanism in each chamber. The substrates are radiatively heated. Turbo pumps were used to achieve base pressure of $1\text{x}10^{-6}$T. Dedicated quartz crystal monitors were used to monitor the thickness of each element.

Thermal evaporation is used for deposition of individual elements. Radak evaporation guns were used for this purpose. These give a high degree of control and avoid spitting of the sources. Alumina crucibles were used for Cu, In and Se and quartz crucibles were employed for Ga deposition. Molybdenum crucible liners were inserted into the alumina crucibles used for Cu and Se depositions. The liners were used to protect the crucibles from breakage due to TCE mismatch between the crucible material and the deposition element. Cu and Ga depositions were carried out in chamber 1 which was totally isolated from Se. Chamber 2 had evaporation sources for Cu, Ga and Se. Sources were normally replenished after every 5 runs. Pneumatic shutters were provided over each source to minimize cross contamination when the sources were not being used. A deposition window of 2in x 2in is placed below the substrate holder to protect the chamber walls from excessive coating. A pneumatic substrate shutter is attached below the window to isolate the substrate from the source during the source stabilization. A shield is used to separate the sources in chamber 2. The chamber themselves are double jacketed and water cooled. The entire chamber was built in the lab as part of this research.

Copper and group III sources are placed at the opposite ends of the substrate. The Se source is placed perpendicular to the metal sources. The Se source is at the middle of the substrate while the Cu, In and Ga sources are near the left edge of the substrate as shown in Figure 4.5. The figure also shows the numbering system for the cells fabricated in this system.

The thickness gradient for Cu, Ga and Se follows the source location and is highest near the source and drops off as we move away from the source. The thickness of In is the least near the source and increases as we move away from the In source. Thus the Cu and In thicknesses track each other. This detail is important while analyzing device performance. The thickness gradient results in a metal ratio gradient as shown

Cu

```
┌─────────────────────────────┐
│ 1     6    11      16   21   │
│                             │
│                          Se │
│                             │
│ 5    10    15      20   25   │
└─────────────────────────────┘
```

In,Ga
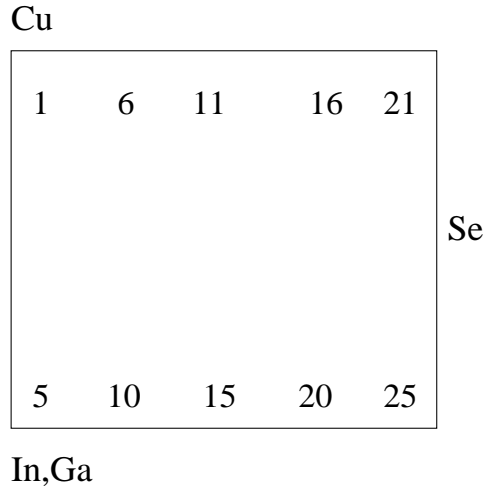
Figure 4.5 Source Arrangement in the Inline Evaporator

in Figure 4.6. These ratios are calculated on the assumption that all the evaporated materials have a sticking coefficient of 1. Metal ratios exceeding unity when the Cu is deposited in chamber 2 is an indication of the following, (a) formation of a secondary $Cu_{2-x}Se$ phase away from the junction; (b) some reevaporation of Cu from the substrate.

Cu

```
┌───────────────────┐
│       0.98        │
│                   │
│       0.94        │
│                   │
│       0.89        │
└───────────────────┘
```

In

(a)

Cu

```
┌───────────────────┐
│       1.08        │
│                   │
│       1.11        │
│                   │
│       1.09        │
└───────────────────┘
```

In

(b)
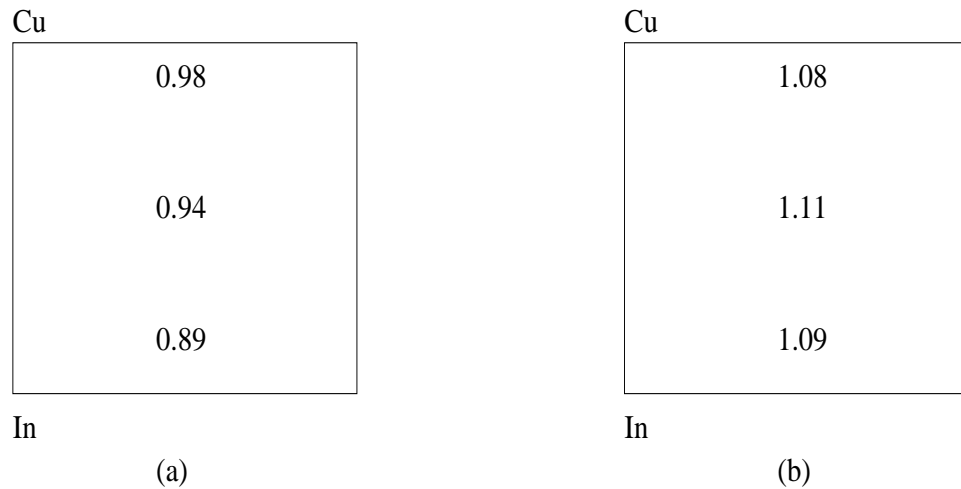
Figure 4.6 Metal Ratio Gradient on the Substrate (a) Cu in Chamber 1 (b) Cu in Chamber 2

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Precursors were deposited in the order $Cu/Ga/In_2Se_3$. The Cu deposition was carried out in both chambers 1 and 2. The runs where Cu was deposited in C1 will be referred to as Type 1A and the runs where Cu was deposited in C2 will be referred as Type 1B. This little detail also seemed to influence device performance in different ways. The optimized evaporation rates from the old system were used for the deposition in the new chamber.

4.2.2.3   Selenization

The substrate temperature is raised up to 450° C in about 3 minutes with an average Se flux of $16 \overset{\circ}{A}$/sec once the precursor formation is completed. The temperature is maintained at 450° C for 7 minutes before it is raised up to 550° C. The temperature is held at 550° C for 7 minutes and a thin layer of Copper(25-100 $\overset{\circ}{A}$) is deposited to neutralize any excess In, Ga present on the surface. The substrate heating is then turned off and the substrate is exposed to the Se flux till it cools down to about 425° C, after which the Se flux is turned off and the substrate is allowed to cool down to room temperature under vacuum. The temperature profile is shown in Figure 4.7.

4.2.3   CdS Deposition

A thin layer of CdS(about 300-500 $\overset{\circ}{A}$) is grown on the absorber by chemical bath deposition. The solution consists of a 0.015 molar cadmium acetate solution for Cd ions, 0.15 molar thiourea solution for Sulfur, 0.15 molar ammonium hydroxide solution and DI water. The substrate is immersed in the solution and the temperature is slowly raised up to 70-80 ^{o}C. The solution is also constantly stirred using a magnetic stirrer. The deposition takes 5-7 minutes approximately.
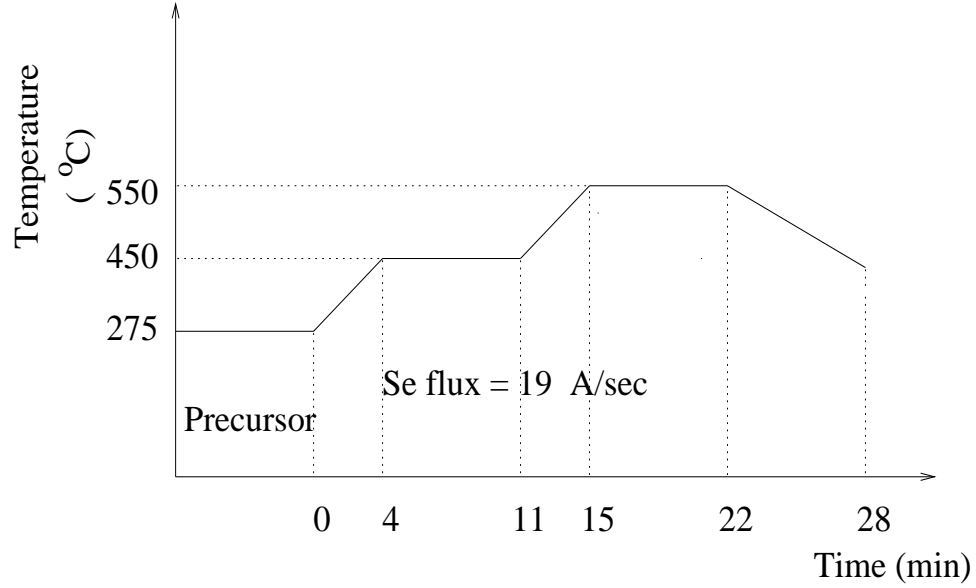
Figure 4.7 Time-Temperature Profile for Absorber Fabrication

4.2.4 Zinc Oxide Deposition

The substrate is blown dry using pure nitrogen gas after the CdS deposition and then loaded in a vacuum chamber to form the window layer by RF sputtering from a ZnO target. A mask is used to form 0.1 cm^2 area dots of ZnO to study the effect of compositional gradients of the metals on the device performance. The substrate is heated to 125° C to remove any moisture absorbed during the CdS deposition and is held constant during the entire deposition. A thin undoped layer (about 400 $\AA$) is deposited in an Argon/ Oxygen ambient followed by a thick Al-doped ZnO (4500 $\AA$)in an argon ambient.

The typical resistivities of the ZnO are of the order of 8-12 $\star$ 10^{-4} ohm-cm and are easily reproducible with nearly 90 % optical transmission over the entire visible and IR region.

4.3 Device Characterization

The fabricated solar cells were routinely characterized by Current-Voltage(I-V) measurements and spectral response measurements. Capacitance-Voltage and Capacitance-Frequency measurements were also done on selected samples to gain further insight into device behavior. The knowledge gained from these measurements was then utilized to modify the fabrication procedure to improve the overall device performance.

4.3.1 Current-Voltage (I-V) Measurements

The current-voltage(I-V) measurements were carried out using either an HP 4145B semiconductor parameter analyzer or a Keithley 2410 sourcemeter. Two-probe and three-probe IV measurements are done with the HP analyzer or a four-probe measurement is done using the Keithley 2410.

In the case where the HP analyzer is used, a two-probe I-V is done on all of the 25 cells on the substrate. One probe is placed on the ZnO contact while the other probe is placed on the Mo back contact. The Mo contact is exposed by physically removing the overlying CIGS and CdS layers using a scalpel. Both dark I-V and light I-V measurements are performed and the V_{oc} and I_{sc} of the cells are noted. The two-probe measurement can suffer from contact resistance problems and hence is not used to determine the fillfactor values. The two-probe I-V is used as a screening measurement to separate the good cells from the bad ones. Silver paint is then applied to the Mo back contact and three probe measurements are done on selected dots. In the three-probe measurement, two probes are placed on the ZnO contact and a third probe is placed on the Ag paint. The maximum power point is determined manually and so are the V_{oc} and I_{sc} values. These are then used to calculate the FF of the

device. The I-V curve can give valuable information about the junction as well as the contacts. A sample three-probe curve is shown in Figure 4.8.
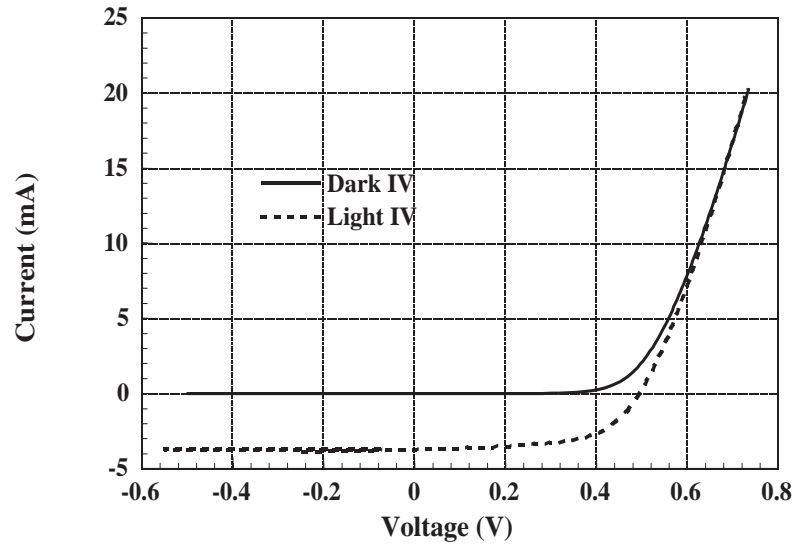
Figure 4.8 A Sample 3- Probe Plot

Midway through this research, the semiconductor parameter analyzer was replaced by a Keithley 2410 sourcemeter. The keithley 2410 was interfaced to a computer and the measurement was performed using a labview program. The I-V measurements performed using this equipment were four-probe measurements where two probes were placed on the ZnO contact and two probes were placed on the Mo contact. This arrangement helps in eliminating the contact resistance between the probe and both the contacts as it is similar to a four-point probe resistivity measurement. The voltage is swept from -0.2 volts to +0.5 volts and both dark and light I-V curves are measured. The labview program outputs the value of V_{oc}, I_{sc} and FF directly.

4.3.2   Spectral Response Measurement

The external quantum efficiency of the sample as a function of wavelength is determined using either a Spex 1704 spectrometer or an Oriel cornerstone 260 monochromator. The measurement setup is calibrated using a standard silicon reference cell(in the wavelength range 400-900nm) calibrated by the National Renewable Energy Laboratory(NREL). A CIS reference standard, again calibrated by NREL is used as the reference cell in the wavelength range of 900-1400nm. The output current of the cell at each wavelength is normalized against the current of the standard at that wavelength. The quantum efficiency is defined as the number of electron-hole pairs collected for every incident photon. The quantum efficiency of the sample at each wavelength is calculated by taking the product of the normalized current and the quantum efficiency of the standard. The quantum efficiency of the sample obtained from the Si standard and the CIS standard are matched at 900nm to get a smooth response from 400-1400nm. The quantum efficiency is integrated to get the short circuit current density J_{sc} of the device. A sample quantum efficiency plot is shown in Figure 4.9.

As the Spex 1704 spectrometer was old it was eventually replaced by a cornerstone 260 monochromator. The only difference in the measurement procedure was that a Ge standard cell was used to calibrate the setup in the 900-1400nm wavelength range, instead of the CIS standard cell used with the older equipment.
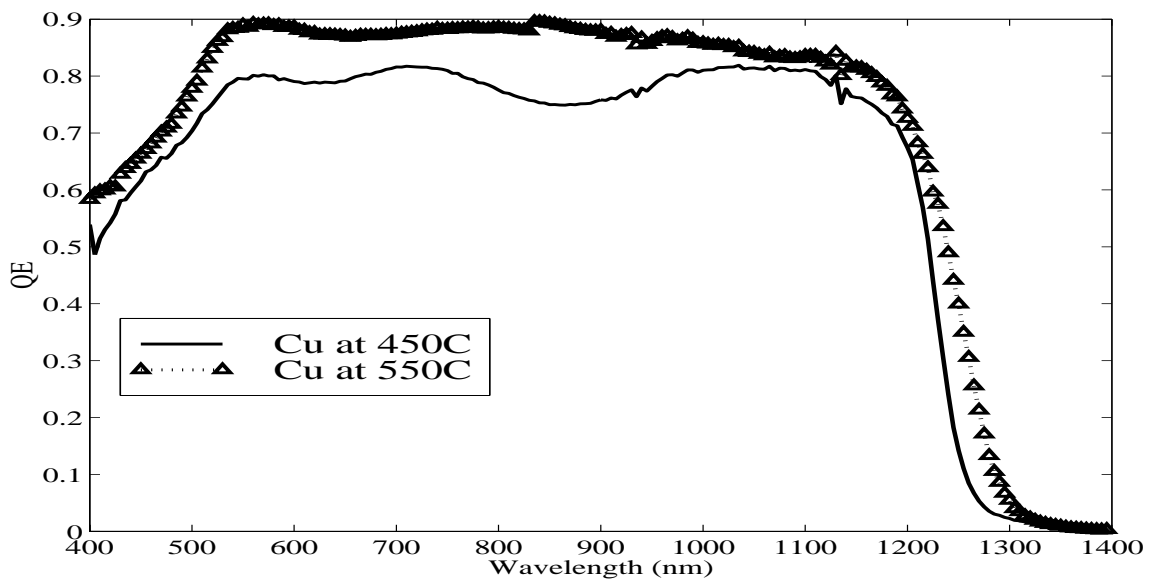
Figure 4.9 A Sample Spectral Response

CHAPTER 5

RESULTS AND DISCUSSION

The performance of CIGS solar cells fabricated by the process described in the last chapter, will be dealt with in this chapter. The objective was to optimize the metal ratios, the top copper thickness as well as the selenization flux.

The devices thus fabricated were analyzed using I-V and spectral response measurements. The open circuit voltages of the devices will be used as the primary parameter in order to study the influence of the processing details on the device performance. The fill factor and short circuit current densities will be used as additional parameters for further verifications. In this research, 25 ZnO dots of area 0.1cm^2 on an average are deposited on a 5cm⋆5cm substrate. In order to determine the J$_{sc}$'s of the devices an accurate measurement of the area of the device is necessary. The spectral response measurement is configured so that it can calculate the area as well as the J$_{sc}$ of the devices. Since these measurements are tedious and time consuming, these were done mainly for better performance devices. Analysis of I$_{sc}$ and V$_{oc}$ data from the I-V measurements was mainly used to design more experiments. The first two sections in this chapter will deal with the performance of the Type I devices fabricated in the four source evaporator. The third and fourth sections will deal with high bandgap devices. The last two sections will deal with devices fabricated in the in-line evaporator.

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5.1 Type I (Cu/Ga/In,Se) - Ga Sputtering

A brief review of the results of the Type I cells, employing sputtered Ga will be presented in this section. This is our baseline process which was developed as part of my Masters thesis. A more detailed analysis can be found in [79].

The typical V_{oc}'s from this process range from 425-475 mV with the current densities of the order of 38-40 mA/cm^2 and 10-12 % routine solar cell efficiencies. V_{oc}'s as high as 495 mV(507mV when measured outdoors) have been achieved with a 64% FF resulting in a device efficiency of 13.0%. Several samples were made by changing the top copper thickness, the selenization flux as well as the metal ratio. In addition, the effect of change in the metal ratio on the same substrate due to the intentional gradients will also be discussed.

5.1.1 Metal Ratio Considerations
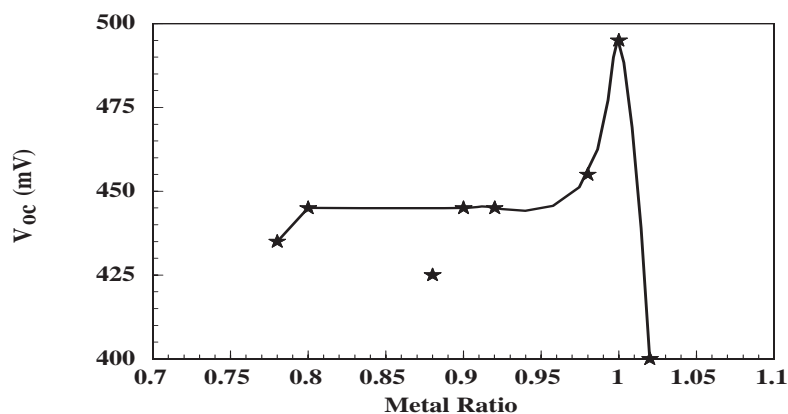
Figure 5.1 Variation of V_{oc} as a Function of Cu/(In + Ga) Ratio on Run 24

Figure 5.1 shows the variation of V_{oc} with metal ratios resulting from the gradient of the metal thicknesses over the substrate. The data is obtained from a substrate where the thickness of the top copper ranges from $91\mathring{A}$ near the Cu source to $77\mathring{A}$ on

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the far edge. The device results are shown for metal ratios ranging from 0.77 to 1.02. It can be seen that the device performance is varying by 95 mV with the changing metal ratios. The V_{oc} shows a peak around Cu/(In+Ga) ratio of 1.00. It falls off on either side of unity. The drop is greater when Cu/(In+Ga) exceeds 1.00. This is thought to be due to the formation of Cu_2Se which being highly conductive, shorts out the junction. The drop in the voltages on the other side is probably due to the fact that not enough top copper is being supplied so as to neutralize the excess In on the surface of the film.

<div align="center">

Cu Source

1.02	1.01	1.00	0.99	0.98
0.97	0.96	0.95	0.94	0.93
0.92	0.91	0.90	0.89	0.88
0.86	0.85	0.84	0.83	0.83
0.80	0.79	0.78	0.78	0.77

Se (left) Ga (right)

In Source

</div>

<div align="center">

Cu Source

400	490	495	455	455
475	475	455	440	445
445	455	445	425	425
455	445	445	435	425
445	430	435	425	X

Se (left) Ga (right)

In Source

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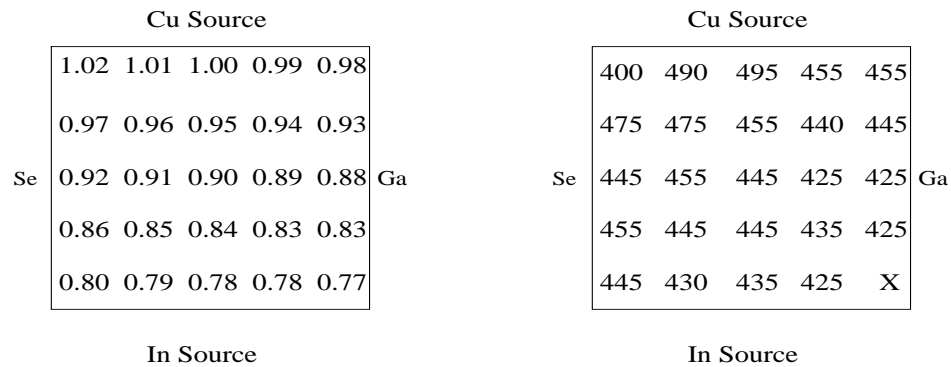
Figure 5.2 The Distribution of Cu/(In+Ga) Ratio and V_{oc}'s on Sample 24

The distribution of metal ratios as well as the corresponding V_{oc}'s on a single substrate are shown in Figure 5.2. V_{oc}'s show a peak around Cu/(In+Ga) ratio of 1 probably because of fewer defects in the CIGS. It drops off on either side of unity. Low V_{oc}'s in other spots where the metal ratio is very close to unity is probably due to the Se flux not being high enough in regions away from the Se source.

Figure 5.3 shows a plot of the variation of V_{oc} with Cu/(In+Ga) for sample 24. Here the effect of selenization flux has been decoupled from the metal ratio effects. Along each column the amount of Se supplied to the substrate is constant while it varies across the substrate and decreases from column 1 to column 5. It is evident

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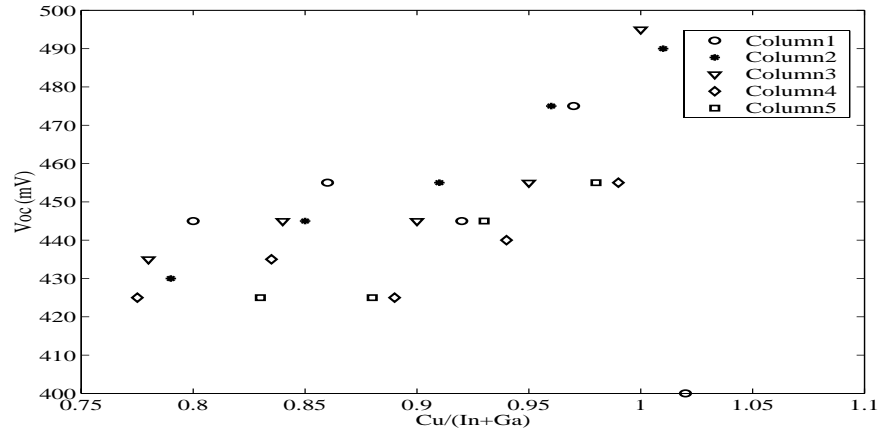
Figure 5.3 Variation of V_{oc} as a Function of Cu/(In+Ga) on Substrate 24 with the Effect of Se Flux Decoupled

from the plot that within a column the V_{oc}'s increase with the metal ratio and tend to show a peak as the metal ratio approaches unity. This is probably because there are fewer defects in the material and a higher quality absorber is being formed. The absolute maximum V_{oc} does not depend just on the metal ratio alone but also on other variables like the top copper thickness as well as the Se flux. This then hints that we need to get the metal ratio and the Se flux right in order to hit the high V_{oc}'s on a run to run basis.
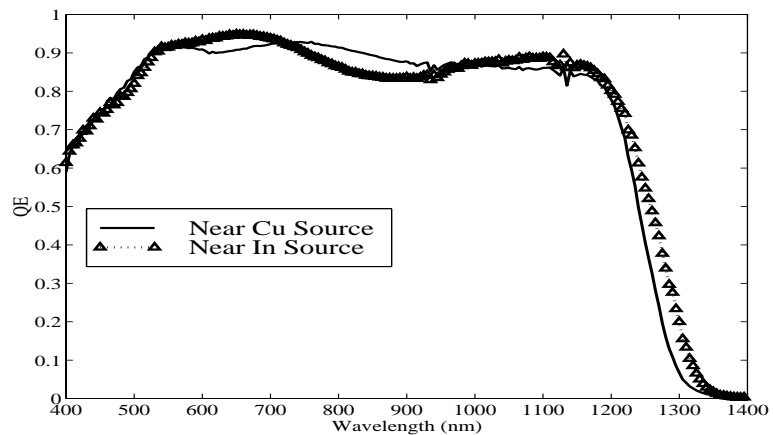
Figure 5.4 Variation of Spectral Response on Sample 23

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Figure 5.4 shows the spectral responses of two devices from run 23, one near the Cu source(Cu/(In+Ga) of 0.99) and the other near the In source(Cu/(In+Ga) of 0.77). There is very little variation in the short circuit current densities, hinting that the J_{sc}'s are not overly affected by the metal ratios provided that the metal ratio is above 0.75. This then hints that the top Cu was enough to neutralize the surface and was probably able to diffuse into the bulk and passivate some defects therein. Another interesting observation from the same figure is that there is a slight shift in the band gap hinting that some amount of Ga is indeed getting into the space charge region. The interference peaks in the curves show that the film is smooth and specular.
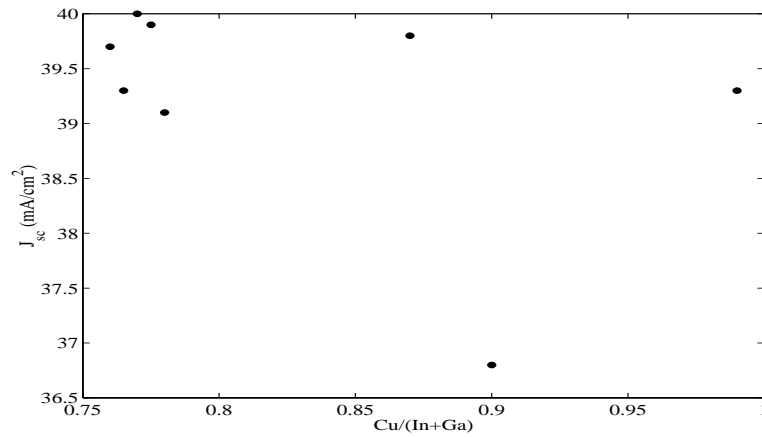
Figure 5.5 Variation of J_{sc} as a Function of Cu/(In+Ga) on Sample 23

Figure 5.5 shows the variation of J_{sc} with Cu/(In+Ga). It can be seen that once we are in a good metal ratio range of 0.8 to 1.00 the J_{sc}'s are not affected too much. The small variations could be attributed to measurement accuracy which can be off by 5-10%. It can be inferred that we can afford to be slightly In rich in the bulk as the currents do not seem to be overly sensitive to the metal ratio as long as the metal ratio is above 0.75. In order to achieve high efficiencies($>14\%$) we need to get the metal ratios close to unity to get high V_{oc}'s as well as J_{sc}'s.

Figure 5.6 shows the I-V curve of our best device. The device showed a V_{oc} of 495 mV, J_{sc} of 40 mA/cm^2 and a FF of 64%. The same device showed a V_{oc} of 507 mV when measured outdoors resulting in a conversion efficiency of 13%. The FF is slightly on the lower side and has the greatest impact on the device efficiency. If the FF is improved to 70% or beyond, device efficiencies can very well exceed 15%.
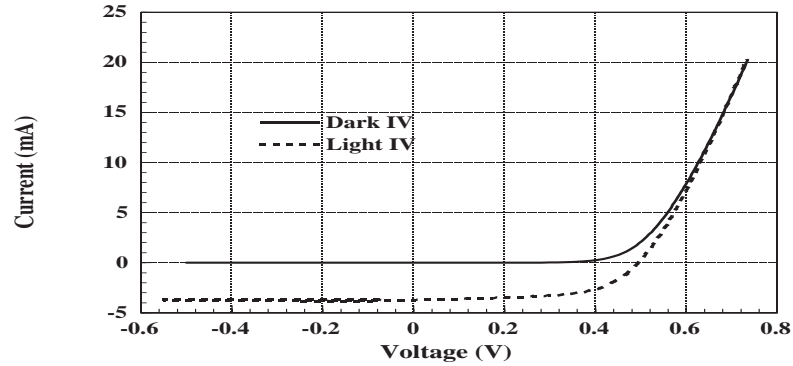
Figure 5.6 I-V Curve of 13.0% Device

5.1.2 Influence of Top Copper on Device Performance

Depending on the starting Cu/(In+Ga) ratio, the surface of the semiconductor can have higher or lower concentration of group III during selenization. This directly determines the amount of Cu needed to neutralize the surface to achieve near stoichiometric film.

Figure 5.7 shows the dependence of V_{oc} on the top Cu thickness. These are the maximum V_{oc}'s from a series of runs. Care was taken to ensure that other details like the starting metal ratios and the Se flux were kept constant while the top Cu thickness alone was varied. The plot shows a spread of data for the same Cu thickness indicating that there might be hidden variables which need to be brought to light so as to further the understanding of the exact effect of the top copper. There could be variations because of the fact that the background Se(Se coming off from the walls of
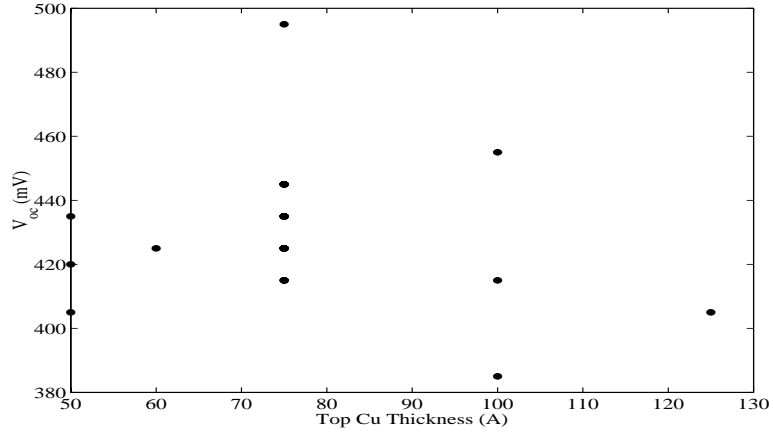
Figure 5.7 Variation of Maximum V_{oc} with the Top Cu Thickness

the chamber) is not constant from run to run. It can be seen that a top Cu thickness of around $75\mathring{A}$ gives us the optimum performance in regions near the Cu source (from Figure 5.2), for our starting metal ratios which range from 0.95 near the Cu source to 0.75 in the regions near the In source. Thicknesses greater than $75\mathring{A}$ pushes the metal ratio over 1.00 in regions near the Cu source leading to poor device performance.

Table 5.1 Effect of Top Cu Layer on Device Parameters

Sample No.	Top Cu Thickness ($\mathring{A}$)	Top Copper Dep Temp (^oC)	V_{oc} (mV)	J_{sc} mA/cm^2
04-17	50	450	410	35.1
17-08	50	450	457	36.1
19-07	60	450	455	34.4
16-10	54	450	432	35.5
20-21	50	550	420	39.0
23-21	50	550	435	39.3
24-11	75	550	495	39.9
25-06	75	550	445	40.0
27-07	100	550	455	39.0
31-07	75	550	445	40.0
65-01	50	550	405	-
66-02	60	550	425	35.0

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Table 5.1 shows the dependence of cell parameters on the top Cu thickness as well as its deposition temperature. It is evident from Figure 5.8 that the short circuit current densities are lower when the top Cu is deposited at 450° C. This is probably due to the fact that the film is not completely homogenized at these temperatures. The lower currents are due to a lower blue response as it is believed that the top Cu reacts only with the surface and hence has maximum influence on the front of the device. The copper deposition at 550 ^{o} C gives better performance in terms of J_{sc}'s. This could be because not enough Se has been supplied to the film at the intermediate 450° C step during selenization before the deposition of the top Cu. Another hypothesis is that this improved performance is a temperature driven effect and the higher temperatures could alter the reaction kinetics favorably.
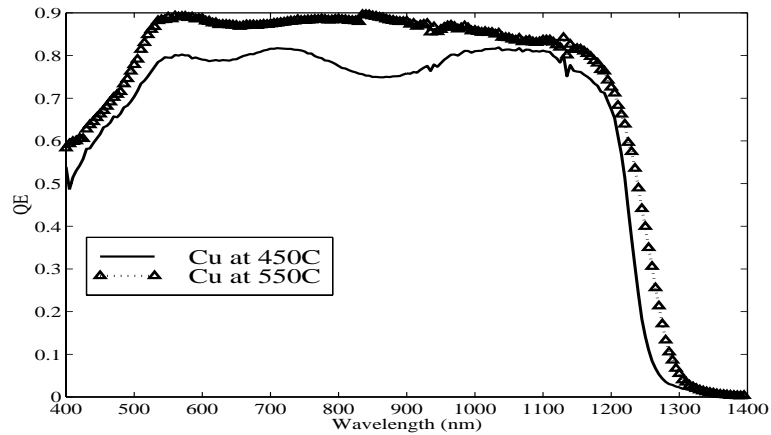
Figure 5.8 Spectral Responses of Two Devices with the Top Cu Deposited at 450° C and 550° C

5.2   Type I - Ga Evaporation

During the course of this research, the magnet of the sputtering gun used to deposit Ga became weak and it was decided to replace the gun by an evaporation source for Ga. The Se source was moved to the opposite side, where the Ga sputtering gun was originally located. So all the process parameters had to be optimized again.

5.2.1 Effect of Ga Thickness

Table 5.2 Effect of Ga Thickness on Device Performance

Sample No.	Ga Thickness ($\mathring{A}$)	V_{oc} (mV)	$J_{(sc)}$ (mA/cm^2)
120-13	950	365	20.5
122-12	950	405	27.8
145-11	875	385	33.5
155-18	800	385	40.0
137-11	750	385	38.1
153-13	725	385	39.9

Table 5.2 shows the V_{oc} and J_{sc}'s of different samples for different Ga thicknesses. The V_{oc}'s seem to be independent of the Ga thickness in the film while the J_{sc}'s show a strong dependence. This could be due to the formation of defects in the bulk which act as recombination centers thereby hurting the J_{sc}'s. The change in Ga thickness does not result in any noticeable change in the bandgap. This then indicates that there is no properly bonded Ga available in the space charge region. Thus the V_{oc}'s are almost constant. This is one of the major differences between Ga evaporation and Ga sputtering, where there is a small bandgap shift leading to slightly higher V_{oc}'s without any loss in J_{sc}. Figure 5.9 shows the effect of Ga thickness on QE profiles.

5.2.2 Effect of Undoped ZnO Thickness on Type I Evaporated Ga Devices

A series of experiments were carried out on Type I devices where the undoped ZnO thickness was systematically varied from $300\mathring{A}$ to $700\mathring{A}$. The device performance for these samples is shown in Table 5.3.

These experiments with the intrinsic ZnO were carried out because of the presence of kinks and crossover between the light and dark I-V curves. A sample curve is shown in Figure 5.10. In simulation studies it was determined that the electron affinity of ZnO is an important parameter in the device performance. The V_{oc}'s and FF's were
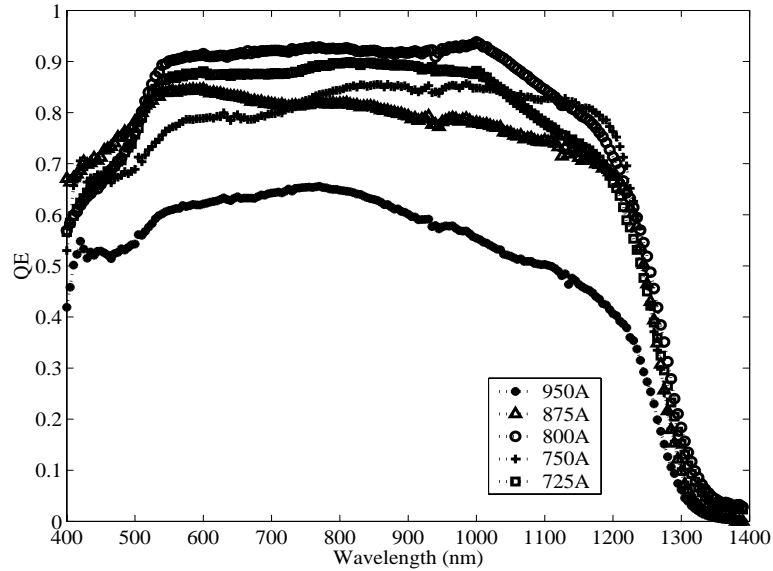
Figure 5.9 Effect of Ga Thickness on QE

Table 5.3 Correlation Between ZnO Thickness and Performance

Sample No.	Undoped ZnO Thickness ($\mathring{A}$)	V_{oc} (mV)	FF (%)
151-23	700	385	34.68
150-23	500	395	45.97
152-22	400	415	60.29
155-21	300	425	57.06
153-22	300	375	50.11

very sensitive to any change in the electron affinity of the ZnO. This then hinted that the undoped ZnO is an important region which needed to be carefully looked at.

The observance of kinks in the I-V curve hints at the possibility of the presence of a junction at the front electrode. If indeed a junction is present, this could then be attributed to the intrinsic ZnO. The behavior of the I-V curve should change as the intrinsic ZnO thickness was varied. It was indeed found that the V_{oc}'s responded to the reduction in the iZnO thickness and increased as the iZnO thickness was reduced from $700\mathring{A}$ to $300\mathring{A}$. However, repeatability was a concern with an iZnO thickness of $300\mathring{A}$. There was a wide performance spread in terms of V_{oc}'s and hence an intrinsic

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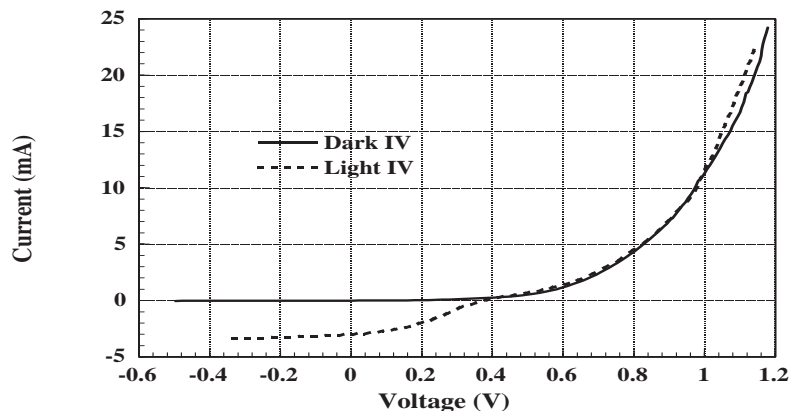
Figure 5.10 I-V Curve Depicting Kinks and Crossover

ZnO thickness of $400\mathring{A}$ was chosen, which seemed to have good reproducibility and performance. The fillfactors also increased, as the iZnO thickness was reduced from $700\mathring{A}$ to $400\mathring{A}$. However, the FF started decreasing when the iZnO thickness was reduced to $300\mathring{A}$.

In the course of this work, it was found that the Type I devices were pretty sensitive to the Se background in the vacuum chamber. Due to the large amounts of Se used in the absorber fabrication, the chamber walls and fixtures get coated with Se, leading to a build-up of Se inside the chamber. The chamber gets very hot during the evaporation of Cu, and Se evolves from the walls of the chamber and the fixtures inside the chamber. This Se is defined as the background Se and is an uncontrollable variable, as it depends on the condition of the chamber prior to the run. This background Se can affect the metal ratio of the film or lead to formation of secondary phases, thus affecting the reproducibility of results. The Type I devices were therefore temporarily abandoned. At this time we decided to fabricate some higher bandgap devices and the next two sections will deal with these devices.

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5.3 Type II Precursors (In$_2$Se$_3$/Cu/Ga)

5.3.1 Effect of Ga Thickness on Type II Devices

Runs 174, 177, 178, 179, and 181 were processed under standard Type II conditions, except for the fact that the Ga thickness was varied for these samples. The Se flux was fixed at 25Å/s for all of these runs. The Ga thickness and the corresponding device performance of various samples is shown in Table 5.4.

Table 5.4 Effect of Ga Thickness on Device Performance

Sample No	Ga Thickness (Å)	V$_{oc}$ (mV)	J$_{sc}$(mA/cm^2)
174	800	445	27.9 - 31.2
177	800	435	29.6 - 32.8
178	600	345	31.6
179	400	415	32.5 - 33.6
181	200	255	—

As seen from the table, V$_{oc}$'s seem to increase with increasing Ga thickness. The data point with a Ga thickness of 600Å appears to be an anamoly. This was not repeated and there is no other way of explaining the sudden drop in performance. At a Ga thickness of 200Å the open-circuit voltage drops dramatically. This could be because of the fact the Cu/In+Ga ratio is probably greater than one leading to the formation of highly conductive Cu$_{2-x}$Se phase which deteriorates the device performance.

On the other hand, the J$_{sc}$'s seem to prefer a lower level of Ga in the film. It was observed that the bandgap of the absorber does not change significantly with the changing thickness of Ga. This then suggests that the excess Ga either does not bond or probably bonds improperly in the space charge region. This then detrimentally affects the electronic transport properties of the film. The poor transport properties can be explained in terms of the bandgap profiling in the device. Ga is known to

increase the bandgap of CIS films by moving the conduction band upwards. By having higher amounts of Ga near the surface of the film, the bandgap at the surface is higher than that of the back of the device. This then creates a barrier to the collection of charge carriers thus hurting the J_{sc}'s. The increase in the bandgap should improve the V_{oc}'s. This effect, though not dramatic, is still observed in the devices as the V_{oc}'s seem to slowly increase with increasing Ga thickness, as can be seen from Table 5.4. The bandgap of sample 179 is lower than the other samples. This explains the slightly lower V_{oc} for this sample. However, the J_{sc}'s are higher due to the lower bandgap. The effect of Ga levels on QE's is shown in Figure 5.11. The slope of the spectral response increases with increasing Ga thickness leading to loss of current.
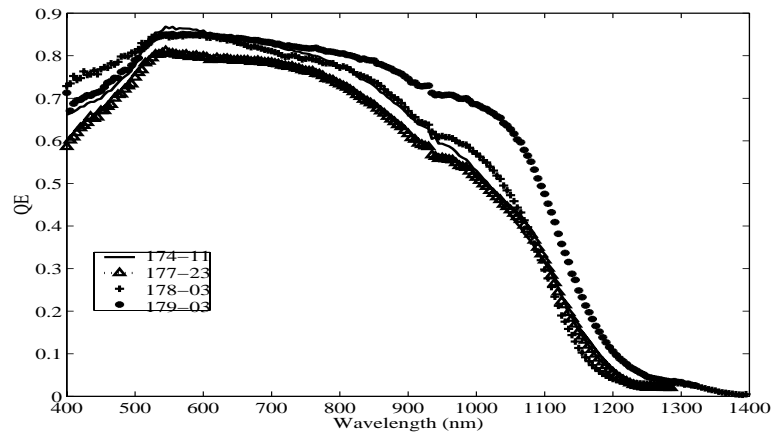
Figure 5.11 Effect of Ga on QE

5.3.2 Effect of Se Flux on Device Performance

Samples 173, 174, 175, 176 and 177 were standard Type II devices in which the Se flux during the selenization was varied from $30\mathring{A}/s$ to $20\mathring{A}/s$. The Se flux during the In$_2$Se$_3$ was kept constant at $30\mathring{A}/s$. The Ga thickness was fixed at $800\mathring{A}$ for these runs.

Table 5.5 Effect of Se Flux on Device Performance

Sample No.	Se Flux ($\mathring{A}$/s)	V_{oc} (mV)	J_{sc} (mA/cm^2)
173	30	415	28 - 31.5
174	25	445	27.9 - 31.2
175	20	385	30.2 - 32.8
176	20	395	—
177	25	435	29.6 - 32.8
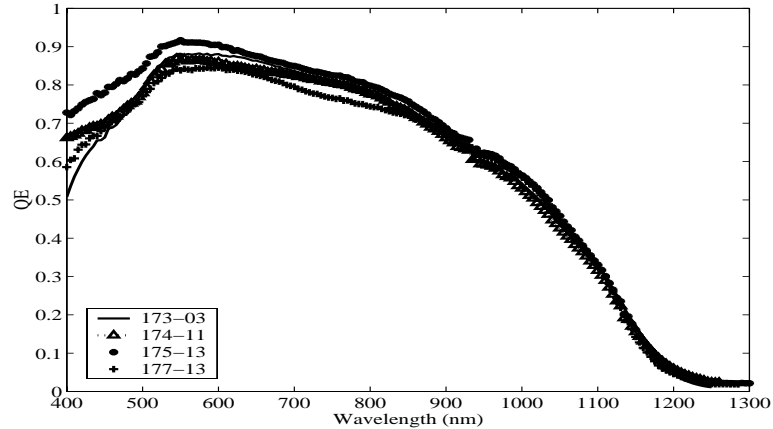
Figure 5.12 Effect of Se Flux on J_{sc}

From Table 5.5, it can be inferred that the device performance (in terms of the open-circuit voltage) seems to show a peak around a Se flux of 25$\mathring{A}$ /s. The V_{oc}'s fall off on either side of this Se flux. The Se flux determines the final metal ratio of the film. Low Se flux causes removal of In and Ga in the form of In$_2$Se and Ga$_2$Se which have high vapor pressures at standard processing temperatures. On the other hand, a very high Se flux could lead to the formation of Se-rich CIGS material whose defect chemistry could be detrimental to device performance. In other words, a very high Se flux seems to produce a poorer photovoltaic grade CIGS film. Since the variation of the Se flux was done at the end of the run the Se flux should not have a strong effect on the J_{sc}, which is believed to be a property of the bulk of the film. This can

be inferred from Figure 5.12 where the J_{sc}'s are, to a first order, the same for various Se fluxes.

5.3.3   Temperature Effects on Device Performance

5.3.3.1   Effect of Higher Selenization Temperature

In an effort to improve the homogeneity of the CIGS film, a top selenization temperature of 575° C was chosen for sample 183, which had $400\mathring{A}$ Ga and a Se flux of $25\mathring{A}$/s. This sample could be directly compared to sample 179 processed under identical conditions with a top selenization temperature of 550° C. The open-circuit voltages on these samples were identical (415 mV) hinting that the higher temperature did not detrimentally affect the surface, though it didn't improve it either. The J_{sc}'s on the other hand, improved a little, but more importantly the slope of the QE curve became squarer, when a higher top temperature was used. This effect is depicted in Figure 5.13.
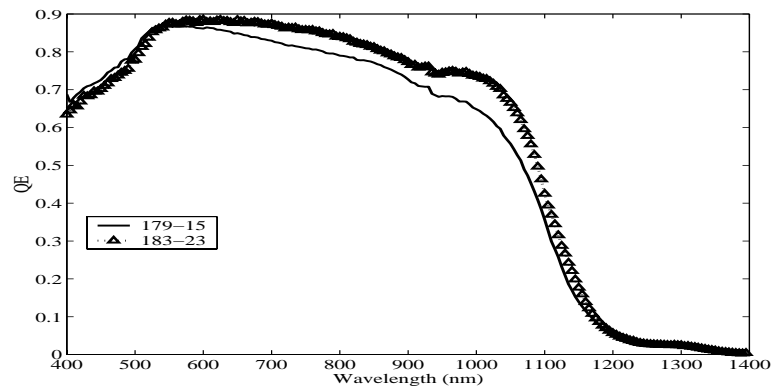
Figure 5.13 Effect of Higher Selenization Temperature on J_{sc}

5.3.3.2   Effect of Longer Selenization Time

Sample 190 was processed using a standard recipe, but the time of stay at 550° C was doubled. The sample showed a remarkable improvement in terms of both V_{oc}'s and J_{sc}'s. A maximum V_{oc} of 465 mV was achieved on this sample along with a J_{sc} of 34.1 mA/cm^2. It is worth noting here that this sample has a larger bandgap than the standard sample. This probably explains the higher V_{oc} of this sample. The V_{oc}'s seem to prefer the Se side and drop off dramatically as we move away from the Se source. The V_{oc} distribution is shown in Figure 5.14. The difference in V_{oc} could be due to the fact that we may be removing some group III materials from the film or it could be a combination of lack of Se and time of stay at 550° C. The longer time of stay seems to improve the bulk of the film and helps in increasing the bandgap as well.

<div align="center">

Cu Source

345	365	395	375	465
375	355	395	395	425
365	385	415	415	455
395	385	385	415	435
405	405	365	385	405

In Source

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Figure 5.14 V_{oc} Distribution of Sample 190

The spectral responses of sample 190 and a standard sample (174) are shown in Figure 5.15. The spectral responses are square and also show a bandgap shift indicating the incorporation of Ga into the film. So the longer time of stay at 550°

C has enabled better reaction among constituent elements resulting in the formation of a good quality absorber.
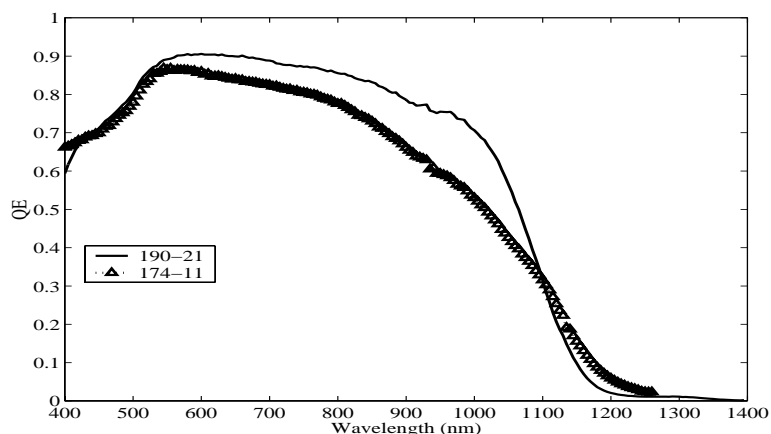
Figure 5.15 Effect of Longer Selenization Time on J_{sc}

The time of stay at 550° C was tripled for sample 191. The V_{oc}'s and J_{sc}'s became very poor. The V_{oc} distribution for this sample is shown in Figure 5.16 and the spectral responses are shown in Figure 5.17. The results hint that both the surface and bulk are affected detrimentally by a very long stay at 550° C. The spectral responses do not exhibit as strong a slope as the standard runs. However, the QE is low overall at all wavelengths. The curve is shifted down when compared to the 14 min sample. This also indicates that the film is poorer thereby hurting the V_{oc}'s and J_{sc}'s. This then suggests that there is an ideal time of stay at 550° C which may be between 7 and 14 minutes, in order to improve the V_{oc}'s without hurting the J_{sc}'s.

5.3.4   Split Ga Runs

In order to study the incorporation of Ga in these films, the Ga layer was split into two parts. An initial layer of $600\mathring{A}$ was deposited at 275° C and a final layer of $200\mathring{A}$ was deposited at 550° C during selenization. This Ga layer was deposited instead of the top copper layer. The Ga deposition was carried out between the

Cu Source

285	305	395	305	315
255	345	325	310	345
240	285	305	335	355
275	285	355	345	285
295	295	335	345	305

In Source

Figure 5.16 V_{oc} Distribution for Sample 191
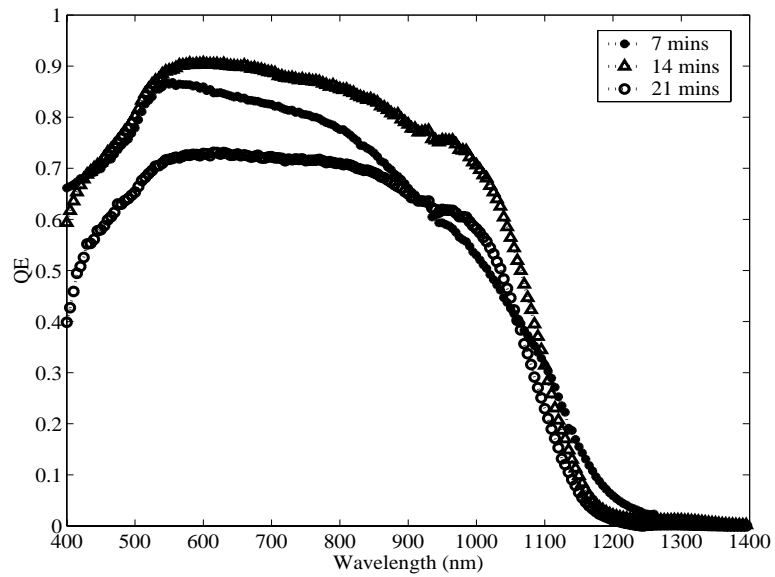
Figure 5.17 Spectral Responses for Longer Time of Stay at 550° C

16th and 18th minute of selenization. The sample showed a V_{oc} of 465mV and J_{sc} of 29.7mA/cm^2. The spectral response had a rounded appearance and there were some hints of secondary phases. Figures 5.18 and 5.19 show the V_{oc} distribution and the spectral response of sample 196 respectively. The split Ga seems to help in improving the V_{oc} probably due to better incorporation of Ga at higher temperatures.

Cu Source

295	285	435	405	325
445	465	465	465	345
405	425	425	405	315
395	355	430	280	335
255	265	375	240	245

In Source

Figure 5.18 V_{oc} Distribution of Sample 196

A small variation of the above run was tried in sample 197 where the 450° C step during selenization was eliminated. The top Ga layer was deposited at 550° C. The deposition was carried out between the 14th and 16th minute of selenization. The idea here was to be Cu-rich at 550° C for a few minutes to enhance grain growth. The Ga was also deposited slightly earlier to give it enough time to react completely before the sample was cooled from 550° C. This recipe had a maximum V_{oc} of 485 mV and a maximum J_{sc} of 32.8 mA/cm^2. The V_{oc} distribution and the spectral response are shown in Figures 5.20 and 5.21 respectively. It can be seen that the V_{oc} increases as we move away from the Cu source. These split Ga runs show some promise as we get improved V_{oc}'s with decent J_{sc} values for bandgaps of 1.1 eV. More efforts have to be focussed on improving the V_{oc}'s of these samples toward the 600 mV mark.

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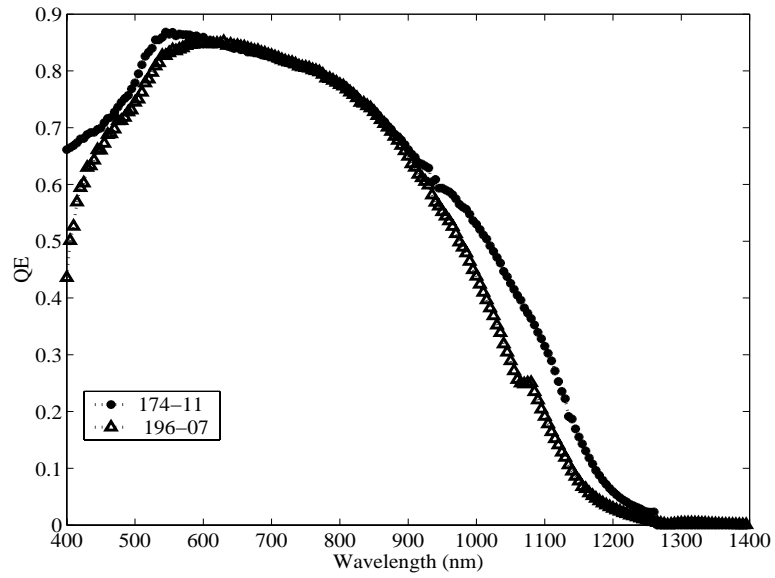
Figure 5.19 Spectral Response of Sample 196

Cu Source

405	395	375	395	455
405	415	425	425	435
415	285	415	420	465
405	435	425	445	485
455	455	475	475	445

In Source

Figure 5.20 V$_{oc}$ Distribution for Sample 197
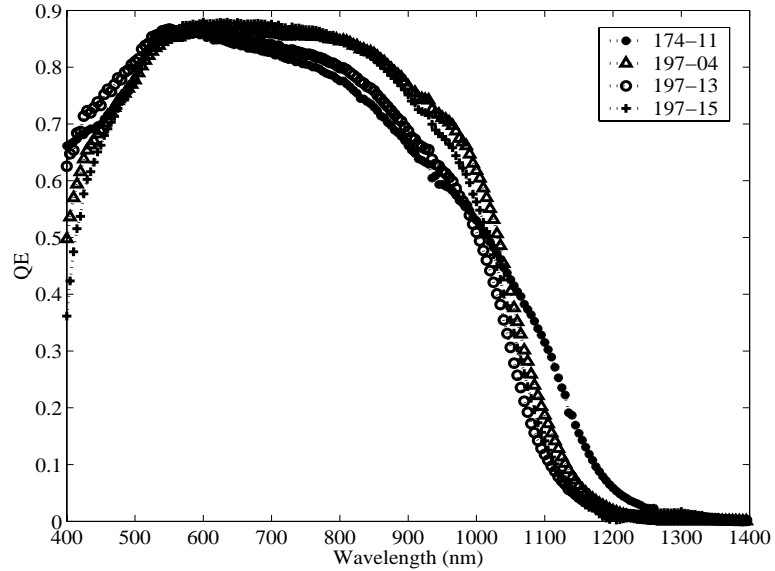
Figure 5.21 Spectral Responses for Sample 197

5.3.5 Split In

Having seen the effect of split Ga, we wanted to see if we could improve the overall device performance by splitting In into two depositions. Sample 198 was a split In run where $2750\mathring{A}$ of indium was evaporated during the In_2Se_3 layer and the remaining $150\mathring{A}$ of In was deposited at 550° C during selenization. The 450^oC step during selenization was eliminated and the In was deposited at the 14th minute of selenization. There was no top copper layer and the sample was Cu-rich at 550° C for about 6 minutes before the In deposition.

The V_{oc} distribution is shown in Figure 5.22. The results indicate that the order of In/Ga deposition controls the V_{oc}. This could be due to the fact that In and Ga compete for the same lattice sites and the presence of In normally prevents the Ga incorporation. Since there is less In at the back of this device, we can expect more Ga to segregate to the back of the device. This then leaves very little Ga in the space charge region thereby hurting the V_{oc}'s which have gone down by nearly 70 mV. This

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Cu Source

285	335	335	355	365
365	365	365	365	385
345	325	385	345	405
315	355	395	415	375
385	385	405	255	275

In Source

Figure 5.22 V$_{oc}$ Distribution of Sample 198
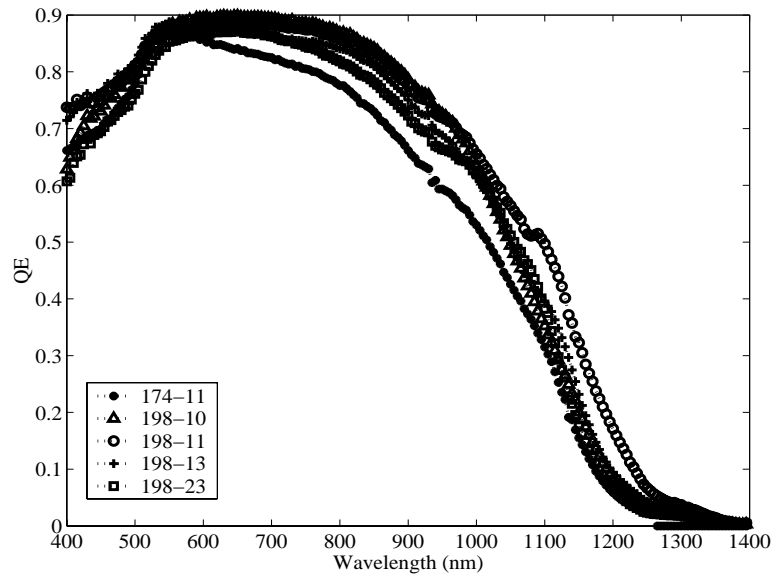
Figure 5.23 Spectral Responses of Sample 198

loss in V_{oc} can be attributed to a reduction in the bandgap of the absorber. On the other hand, the J_{sc}'s are higher, with the highest being 35 mA/cm². There is still a current loss in the red region due to the slope in the QE response which is indicative of collection losses. The spectral responses are shown in Figure 5.23.

5.4 Type III Precursor (In₂Se₃/Ga/Cu)

5.4.1 Effect of Ga Thickness

In order to improve the Ga incorporation efficiency in CIGS films, the order of Cu and Ga depositions were reversed. We believed that, putting the Cu down before the Ga, made some Ga unavailable as the Cu reacts with the Ga to form a Cu-Ga alloy. This probably led to formation of secondary phases and detrimentally affected the film quality. So In₂Se₃ was deposited first, followed by the Ga and finally by Cu. This precursor will henceforth be referred to as the Type III precursor. Initial efforts were focussed on varying the Ga level in the film while holding the Se flux constant at $25\mathring{A}$/s during selenization. Sample 184 was processed with $800\mathring{A}$ of Ga while sample 186 had a Ga thickness of $400\mathring{A}$. The V_{oc} distributions of these two samples are shown in Figure 5.24.

From the above Figure we can see that the V_{oc}'s are pretty uniform for sample 184 with $800\mathring{A}$ Ga while sample 186 is exhibiting Cu-rich behavior. It is worth mentioning here that this effect was not observed with the standard Type II precursors with $400\mathring{A}$ of Ga. This effect can be explained by the location of the Cu-rich phase. In the standard Type II precursor the Cu-rich phase is probably formed at the back of the device (bulk), thus not affecting the junction as much as it does in the case of the Type III precursor, where the Cu-rich phase would be expected to be near the surface as the Cu layer is put down after the In₂Se₃ and Ga layers. The current densities

Cu Source				
395	415	425	425	435
415	405	435	405	455
425	425	435	435	415
405	425	375	430	415
415	425	405	425	425
In Source				

Cu Source				
X	95	X	X	X
145	145	135	155	145
225	215	275	235	265
X	215	280	X	255
305	335	355	355	345
In Source				
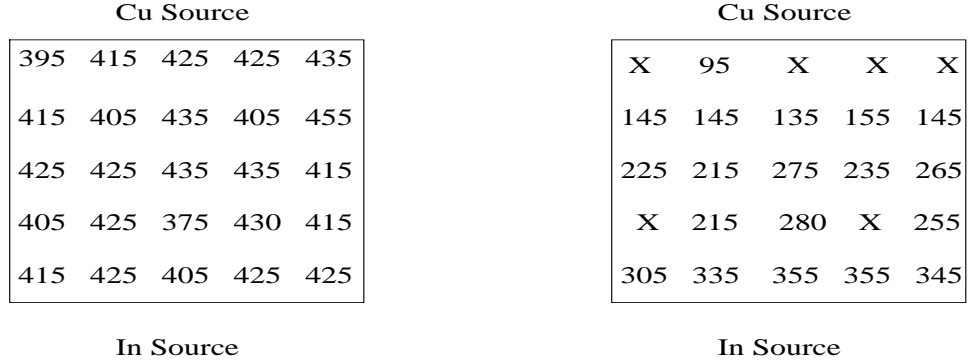
Figure 5.24 V_{oc} Distribution of a) Sample 184 b) Sample 186

for the Type III precursors is also higher than the current densities for the standard Type II precursors.

5.4.2 Effect of Argon Annealing

In order to study the effect of an anneal step on the absorber chemistry, a standard Type III absorber was fabricated as described in chapter 4. The absorber was cooled down to 200° C and then reheated to 575° C in an Argon ambient. Sample 187 was annealed for 10 minutes in Argon at this temperature. Equipment considerations prevented us from going further in anneal time. The V_{oc}'s seemed to be poor in this run. They were around 385 mV to begin with and improved to 405 mV after light soaking. This then hints that the surface is poor. This could be because the anneal was probably not complete and there could have been some secondary phase segregation at the surface, thus hurting the V_{oc}'s.

The J_{sc}'s, on the other hand, seemed to improve with the annealing and the spectral responses were squarer than that of the standard Type II runs as can be seen from Figure 5.25. A J_{sc} of 35.4 mA/cm^2 was achieved for this sample.
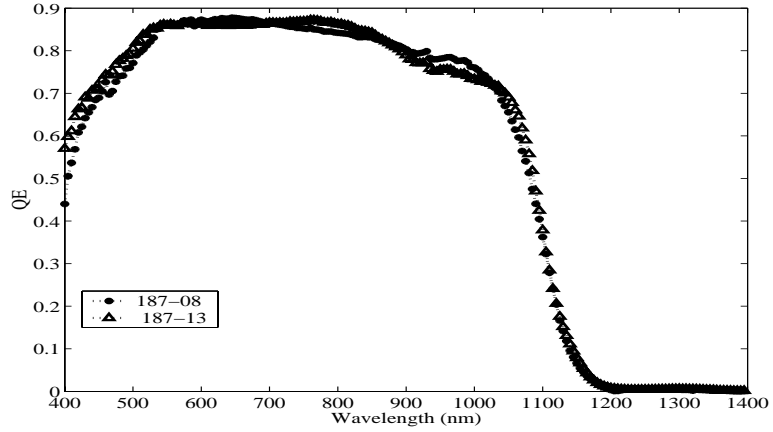
Figure 5.25 Effect of Argon Annealing on J$_{sc}$

5.4.3   Split Ga

Sample 200 was processed using the split Ga recipe developed for the Type II precursor. The 450° C step during selenization was also eliminated and the top Ga was deposited at the 14th minute of selenization. Figure 5.26 shows the V$_{oc}$ distribution of sample 200.

Cu Source

445	460	535	535	435
545	525	525	515	525
545	545	545	555	515
545	505	555	555	545
525	545	555	545	545

In Source

Figure 5.26 V$_{oc}$ Distribution of Sample 200

V$_{oc}$'s as high as 555 mV were measured in this sample. These were some of the highest V$_{oc}$'s achieved for our high bandgap devices. The increase in V$_{oc}$ can

be attributed to the bandgap increase as seen in the spectral response depicted in Figure 5.27. The spectral responses still show a pronounced slope in the long wavelengths, indicating collection losses. Sample 184 shown here is a standard Type III run.
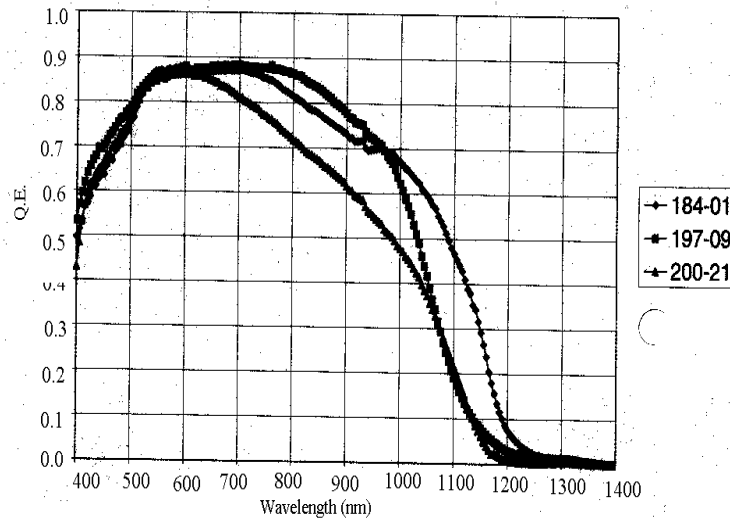
Figure 5.27 Spectral Responses of Sample 200

Sample 202 was processed identically to sample 200 with the only difference being that the top selenization temperature was increased to 575° C. The V_{oc} distribution for this sample is shown in Figure 5.28.

The V_{oc}'s have gone down by as much as 100 mV, indicating that the surface has been damaged. However, the J_{sc}'s showed an improvement but the spectral responses still showed a slope in the long wavelength region as seen in Figure 5.29.

Sample 201 also employed the same recipe as sample 202. However, the Ga level was lower. An initial layer of $400\mathring{A}$ was used along with a top layer of $200\mathring{A}$. This lower Ga content had a detrimental effect on the V_{oc} as shown in Figure 5.30.

Cu Source

345	395	435	255	395
385	425	435	435	425
355	375	425	425	X
415	435	425	435	435
435	455	X	435	415

In Source

Figure 5.28 V_{oc} Distribution of Sample 202
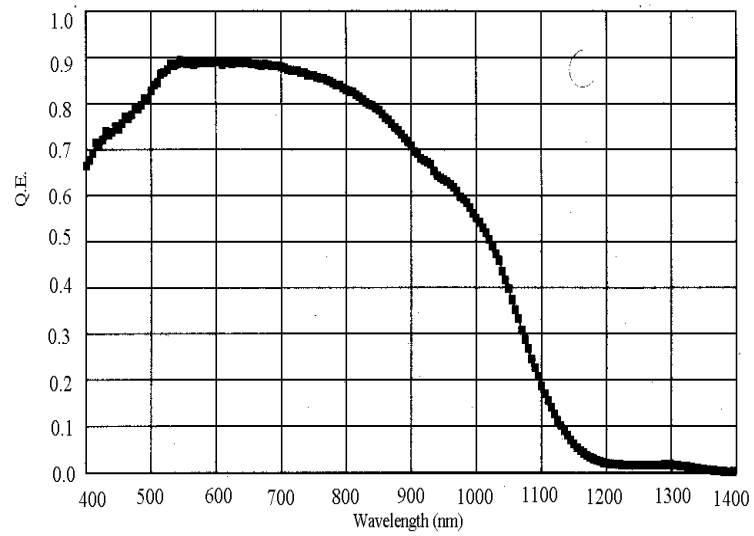
Figure 5.29 Spectral Response of Sample 202

345	345	325	335	335
335	355	345	325	345
435	405	395	405	255
435	395	385	395	425
425	435	420	425	435

In Source

Figure 5.30 V_{oc} Distribution of Sample 201

The J_{sc}'s on the other hand, improved and the slope in the long wavelengths was reduced. So a combination of a lower Ga level and a higher selenization temperature was helpful in reducing the collection losses. There is still an increase in bandgap indicating that some amount of Ga is still bonded in the space charge layer. However, this increased bandgap did not translate into higher V_{oc}'s. This could be due to the formation of defects at the surface of the film leading to an increased interface recombination thereby hurting the V_{oc}'s. The spectral responses of this sample are shown in Figure 5.31.

The split Ga Type III runs gave us higher V_{oc}'s while the longer selenization time used in Type II runs gave us higher J_{sc}'s. The next logical step was to combine the two so as to benefit from the advantages of both these experiments. Sample 204 was processed using a split Ga recipe. The time of stay at 550° C was doubled. The 450° C step was also included. The Ga deposition was carried out at the 21st minute. Figure 5.32 shows the V_{oc} distribution of this sample.

The V_{oc}'s seem to be systematically increasing towards the In source. This suggests that the longer selenization time is probably hurting the surface by removing some Group III (In,Ga) elements. Since the last row has a higher In (Group III)
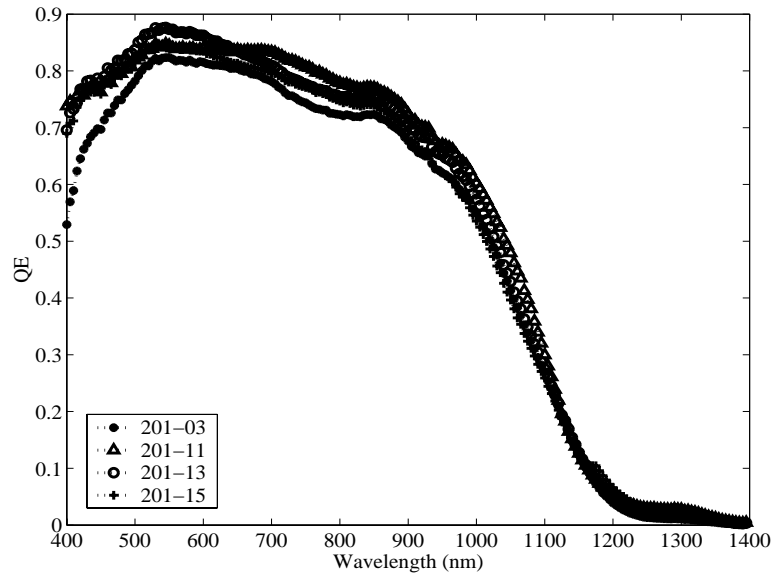
Figure 5.31 Spectral Responses of Sample 201

Cu Source

435	455	455	445	485
485	485	495	495	495
495	505	475	515	515
530	535	535	545	525
555	560	560	555	555

In Source

Figure 5.32 V_{oc} Distribution of Sample 204

level, the V_{oc}'s are not affected by this Group III removal. The spectral responses for this sample are shown in Figure 5.33. The SR's indicate big bandgap shifts but suffer from collection problems. .
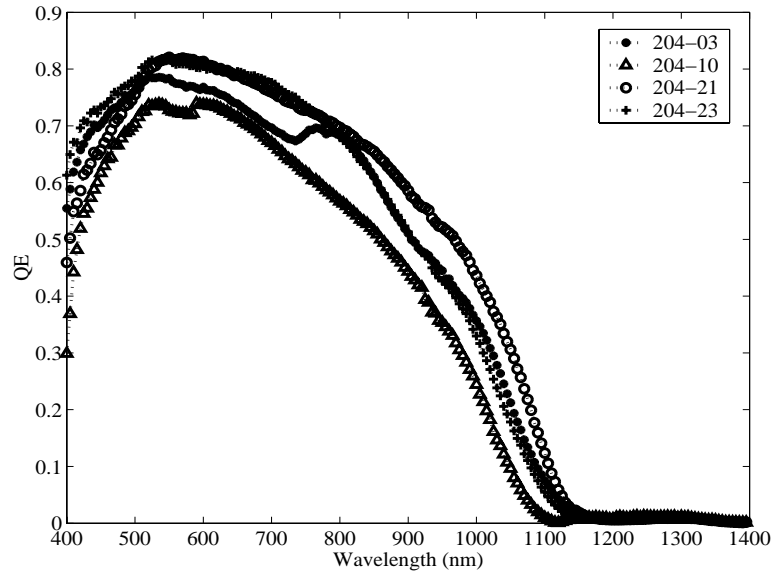
Figure 5.33 Spectral Responses of Sample 204

5.5   Light Soaking

Type II and Type III devices were subjected to some light soaking experiments. Samples were soaked under AM 1.5 (one Sun) light for 10 minutes. They were then allowed to cool down for 30 minutes and then remeasured. Figure 5.34 shows the V_{oc} distribution of sample 184 before and after light soaking.

It can be seen from Figure 5.34 that light soaking seems to improve the V_{oc}'s of the devices, while the J_{sc}'s are largely unaffected by light soaking. Figure 5.35 shows the V_{oc} distribution of sample 180 processed with an In_2Se_3 buffer layer instead of the standard CdS buffer layer.

Since the V_{oc} does not improve for the In_2Se_3 buffers after light soaking, the improvement in V_{oc}'s of standard devices after light soaking could be attributed to

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Cu Source

395	415	425	425	435
415	405	435	405	455
425	425	435	435	415
405	425	375	430	415
415	425	405	425	425

In Source

Before Light Soaking

Cu Source

425	435	445	445	445
405	435	445	435	465
425	445	455	455	435
425	445	425	445	440
X	445	445	445	445

In Source

After Light Soaking

Figure 5.34 V_{oc} Distribution of Sample 184 a) Before b) After Light Soaking

Cu Source

365	375	365	365	345
365	355	355	350	325
445	465	465	465	445
485	485	485	485	445
465	475	475	465	425

In Source

Before Light Soaking

Cu Source

385	375	365	375	335
X	235	365	345	335
445	385	425	465	425
445	455	465	455	425
465	445	455	465	425

In Source

After Light Soaking

Figure 5.35 V_{oc} Distribution of Sample 180 a) Before b) After Light Soaking

the improvement of the CIGS/CdS interface. This could be due to the passivation of the interface states leading to a reduction in the recombination center density, resulting in improved V_{oc}'s of the devices. These results have been found repeatable and the same effect has been observed in Type II devices as well. This concludes the discussion of the high bandgap devices.

5.6 Type IA Precursor (Cu in Chamber 1)

Devices based on the Type IA precursor were fabricated in the new inline evaporator system described in Chapter 4. The Cu and Ga were sequentially deposited in a Se-free environment in Chamber 1. In and Se were co-evaporated in Chamber 2 to complete the precursor. The selenization and top copper deposition were also carried out in Chamber 2. Initial efforts were focussed on adapting our standard Type I process to the new system. Thickness calibration runs were carried out for Cu and Se sources. Thicknesses were chosen such that the final thicknesses on the substrate were identical to the thicknesses in the old system. The In and Ga thicknesses were not calibrated as we assumed that the sources were placed symmetrically in the chamber, and hence the calibration factor would be a constant. The calibration factor for the Cu source was used for the In and Ga sources as well.

The cells showed a spotty behavior in terms of V_{oc}'s. The V_{oc}'s were also very poor. The V_{oc} distribution for sample 218 is shown in Figure 5.36. There were also problems of adhesion. A lot of films peeled off from the underlying Mo substrate.

In order to overcome the poor performance, Ga levels were varied and these experiments did not produce the desired results. Cooling experiments were carried out at the end of the Ga deposition. The reasoning was that Ga being a liquid at room temperature could easily move about on the substrate when the hot substrate was being transferred from Chamber 1 to Chamber 2. The substrate transfer was an

X	X	255	X	X
235	X	255	215	X
X	X	X	275	265
X	X	X	275	155

In Source

Figure 5.36 V$_{oc}$ Distribution of Sample 218

additional detail which was not an issue in the old chamber. These experiments did not improve the device performance either.

Vacuum break experiments were designed to isolate the root cause of the problem. The precursor formation step was split into two halves. In one experiment, Cu and Ga were deposited in the new chamber and the In$_2$Se$_3$ deposition and selenization were carried out in the old chamber. The results were still poor but we had some working devices. Another experiment was done where the Cu/Ga depositions were carried out in the old chamber and the sample was finished in the new chamber. The device was Cu-rich and all the cells were shorted. So based on these two experiments, the problem seemed to lie either in the In$_2$Se$_3$ deposition or the selenization step in the new chamber.

The precursor Cu/Ga/In,Se was deposited in the old chamber for sample 255. The precursor was then selenized in the new chamber. The sample exhibited good V$_{oc}$'s. The baseline Type I V$_{oc}$'s in the old chamber were around 425 mV. Figure 5.37 shows the V$_{oc}$ distribution for sample 255. Based on these results, it is safe to conclude that the selenization step was not a problem in the new chamber. So the problem must lie in one or more layers in the precursor.

Cu Source

285	405	415	415	435
415	0	425	415	425
410	415	385	425	435
405	395	0	425	425
405	405	0	265	415

In Source

Figure 5.37 V_{oc} Distribution for Sample 255

In and Ga thickness calibrations were carried out and it was found that the In thickness calibration was off by a big amount. The problem was that the In source was being blocked by the source separator shield and we were actually making Cu-rich CGS devices instead of CIGS devices. Having fixed the source separator shield, an experiment was carried out where Cu/Ga depositions were done in the old chamber while In_2Se_3 deposition and selenization were carried out in the new chamber. The new thickness calibration for the In was used for this run. Figure 5.38 shows the V_{oc} distribution for this sample. The V_{oc}'s are slightly lower than the previous case. This could be because the Ga surface probably oxidized due to the vacuum break during the substrate transfer from the old chamber to the new chamber. At this time, it was decided to fabricate the entire absorber in the new chamber as thickness calibration issues were resolved.

5.6.1 Effect of Ga Level on Device Performance

The Ga thickness was systematically varied from $450\mathring{A}$ to $250\mathring{A}$. There was no top Cu deposition for these samples . All other process parameters were kept constant. Table 5.6 shows the effect of Ga thickness on device performance. The V_{oc}'s are

Cu Source

365	345	275	195	215
330	350	355	355	375
260	175	X	045	315
245	305	345	305	345
X	X	X	X	X

In Source

Figure 5.38 V_{oc} Distribution of Sample 259

Table 5.6 Effect of Ga Thickness on Device Performance

Sample No.	Ga($\AA$)	V_{oc} (mV)	I_{sc}(mA)
262-21	450	365	1.6
266-06	350	425	2.5
266-11	350	425	2.2
267-21	300	425	2.7
270-21	250	435	2.3
270 01	250	415	3.6

independent of the Ga thickness as long as the Ga thickness is between 350 and 250$\AA$. At a Ga thickness of 450$\AA$, the V_{oc}'s drop probably due to increased defects in the film. The I_{sc}'s also follow the same trend. The spectral responses are shown in Figure 5.39. The J_{sc}'s increase when the Ga thickness is reduced from 450$\AA$ to 300$\AA$. However, the J_{sc} drops off slightly when the Ga thickness is reduced to 250$\AA$. In these experiments, the selenization temperatures were 420 and 520° C instead of the normal 450 and 550° C steps.

The Ga thickness was in turn reduced from 250$\AA$ to 200$\AA$. A top selenization temperature of 550° C was used in both these runs. There was no top copper deposition in either of these runs. Samples 281 and 282 had a Ga thickness of 250$\AA$ and 200$\AA$
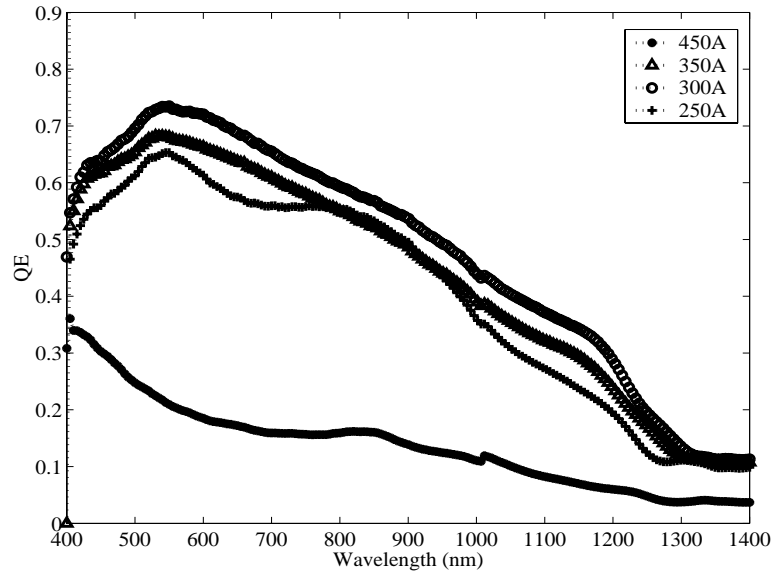
Figure 5.39 Effect of Ga Thickness on J$_{sc}$

respectively. The V$_{oc}$ distribution of these two samples is shown in Figure 5.40. It is interesting to note that the V$_{oc}$'s and J$_{sc}$'s are largely unaffected by the reduction in the Ga thickness. The spectral responses for these samples are shown in Figure 5.41.

<div style="display: flex;">

Cu Source

415	425	415	405	415
405	415	415	405	405
420	425	425	425	425
405	405	405	405	415
405	395	375	385	405

In Source

(a)

Cu Source

435	435	405	435	435
435	435	435	425	435
435	425	415	415	425
425	415	415	425	425
425	425	435	435	435

In Source

(b)

</div>
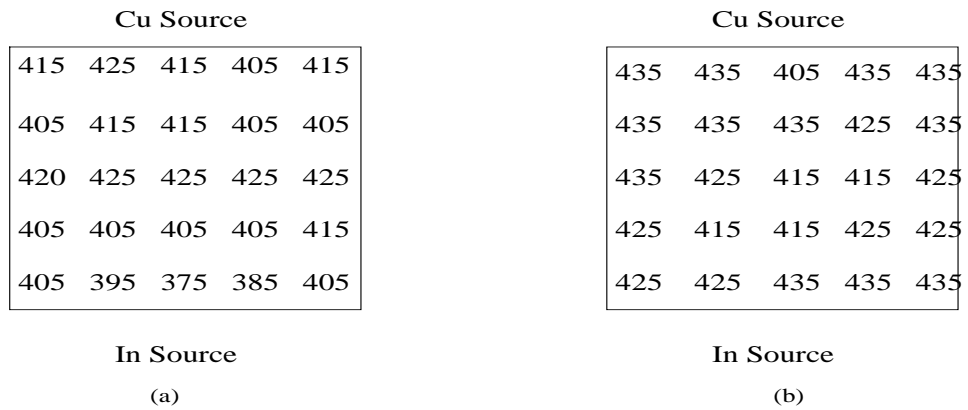
Figure 5.40 V$_{oc}$ Distribution of Samples (a)281 and (b)282
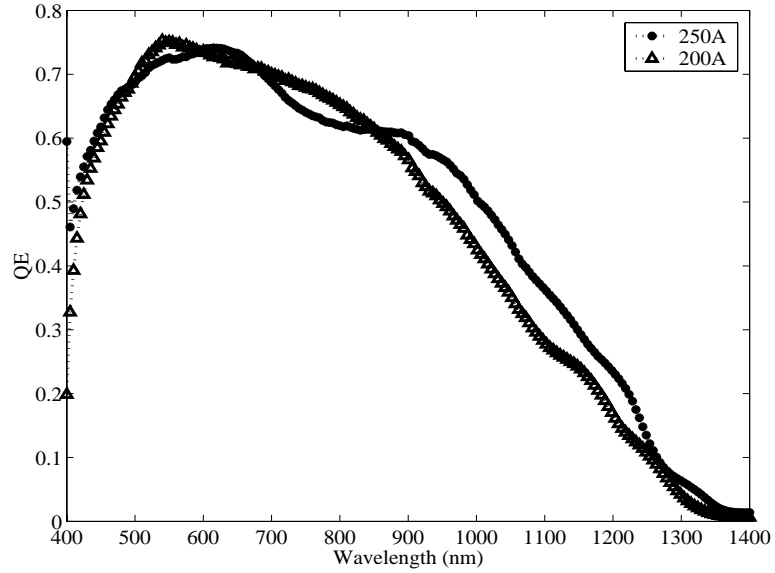
Figure 5.41 Spectral Responses for Samples with Ga Thicknesses of 250$\mathring{A}$ and 200$\mathring{A}$

Table 5.7 Effect of In Thickness on Device Performance

Sample No.	In($\mathring{A}$)	V$_{oc}$ (mV)	I$_{sc}$(mA)
270-01	7000	415	3.6
270-21	7000	435	2.3
271-01	7300	415	2.2
271-21	7300	425	1.1
272-01	6750	385	3.2
272-16	6750	395	1.8

5.6.2   Effect of In Level on Device Performance

The In thickness was varied from 6750$\mathring{A}$ to 7300$\mathring{A}$ with other processing details being the same. There was no top copper deposition and lower selenization temperatures of 420° C and 520° C were used instead of the standard 450 and 550° C temperatures. The effect of the In thickness on device performance is shown in Table 5.7. The V$_{oc}$'s drop off by 30 mV when the In is lowered below 7000$\mathring{A}$. The I$_{sc}$'s reduce when the In thickness is increased to 7300$\mathring{A}$. The J$_{sc}$'s seem to prefer a lower

level of In in the film. The J_{sc}'s increase when the In thickness is reduced from $7300\mathring{A}$ to $6750\mathring{A}$ as shown in Figure 5.42.
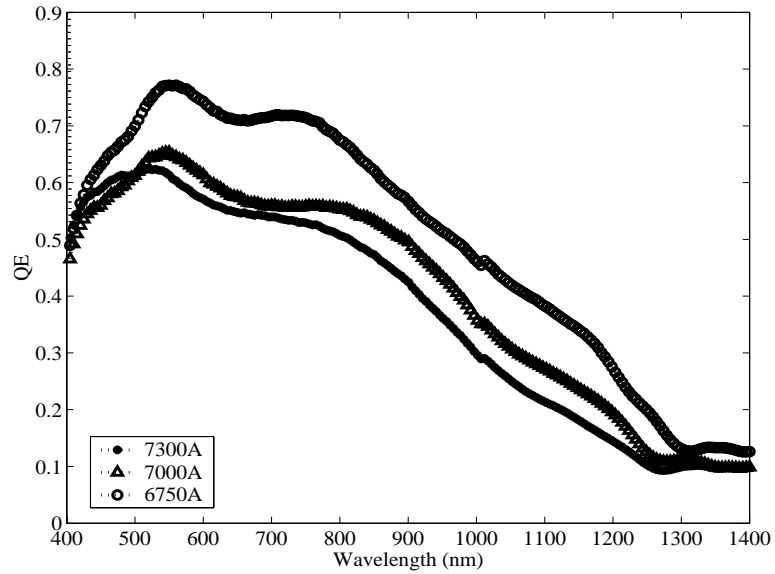
Figure 5.42 Effect on In Thickness on J_{sc}

The In level was further varied to find optimum performance. The Ga level was fixed at $250\mathring{A}$ and a 550° C top selenization temperature was used. There was no top copper deposition. Figure 5.43 shows the V_{oc} distribution of samples 280 and 281 which had In thickness of $6750\mathring{A}$ and $6500\mathring{A}$ respectively. The idea here was to push the metal ratios as close to unity as possible. There is a slight drop in the V_{oc}'s when the In thickness is reduced. The spectral responses for these two samples are shown in Figure 5.44. It is worth mentioning here that there is no bandgap shift indicating that the Ga is segregating to the back of the device. The In level will be fixed at $6500\mathring{A}$ and Ga level at $200\mathring{A}$ for the rest of the discussion in this chapter, unless mentioned otherwise.

415	425	415	405	415
405	415	415	405	405
420	425	425	425	425
405	405	405	405	415
405	395	375	385	405

In Source

(a)

425	425	425	415	405
425	435	435	435	425
425	445	445	435	425
405	425	445	430	425
370	405	425	415	415

In Source

(b)

Figure 5.43 V$_{oc}$ Distribution of Samples (a)281 (b)280
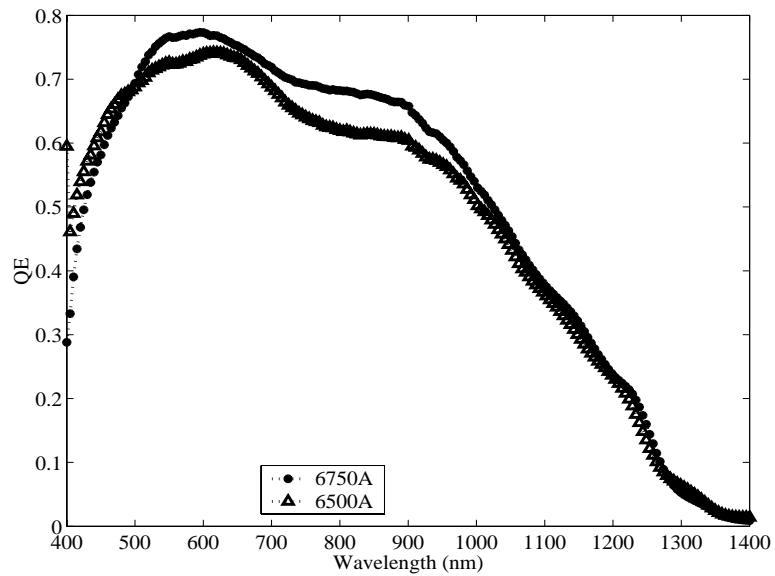
Figure 5.44 Spectral Responses for Samples with In Thickness of 6750$\mathring{A}$ and 6500$\mathring{A}$

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5.6.3 Effect of Top Selenization Temperature

The top selenization temperature was varied between 520° C and 575° C . There was no top Cu deposition for these samples and an In of $6750\AA$ and a Ga thickness of $250\AA$ were used for these runs.

Table 5.8 Effect of Top Selenization on Device Performance

Sample No.	Temp (^{o} C)	V_{oc} (mV)	I_{sc}(mA)
272-01	520	385	3.2
272-16	520	395	1.8
277-24	550	435	3.0
277-13	550	425	3.2
278-01	575	440	0.1
278-05	575	445	0.1

It can be seen from Table 5.8 that the V_{oc}'s increase when the top selenization temperature is increased from 520 to 575° C, indicating a better surface. However, the I_{sc}'s are extremely low, when a top temperature of 575° C is used. So a 550° C top selenization temperature gives a optimum results in terms of I_{sc}'s and V_{oc}'s. The effect of the top selenization temperature on the spectral response is shown in Figure 5.45. The J_{sc}'s are slightly higher for the 550° C sample. The J_{sc}'s from sample 278 could not be measured as the currents were extremely low.

5.6.4 Impact of Top Cu on Device Performance

Table 5.9 Effect of Top Copper on Device Performance

Sample No.	Top Cu($\AA$)	V_{oc} (mV)	I_{sc}(mA)	FF (%)
282-01	0	435	3.9	-
282-03	0	435	4.4	-
286-01	25	450	3.1	62.4
286-03	25	450	4.0	62.4
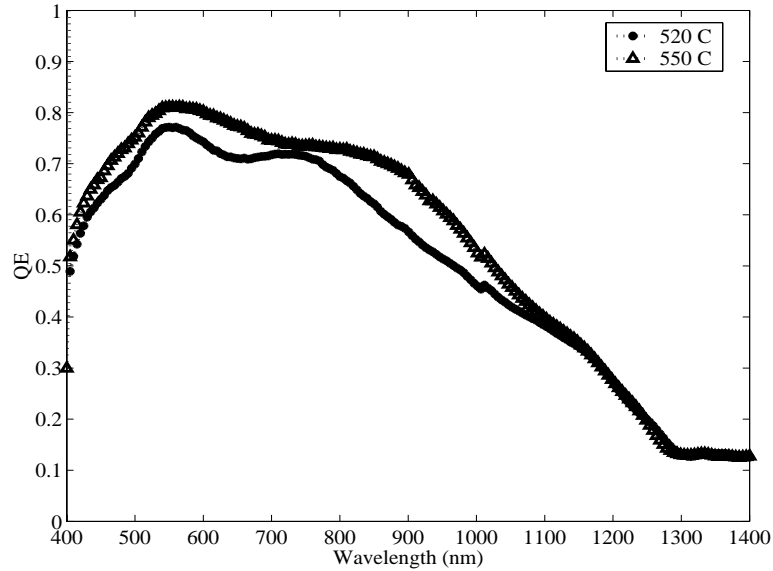
Figure 5.45 Effect of Top Selenization Temperature on the J$_{sc}$

Samples 282 and 286 were processed identically except for the fact that sample 282 had no top Cu while 286 had 25$\overset{\circ}{A}$ of top copper. We can see from Table 5.9 that the V$_{oc}$'s have increased a little. The fill factor values are also good for the sample with top copper. The J$_{sc}$'s also show a little improvement as seen from Figure 5.46.

5.6.5   J$_{sc}$ Dependence on Chamber Conditions

The inline evaporator is equipped with a vent valve in the load lock chamber only. The Se source needs to be replenished after approximately five runs. This meant that we have to vent Chamber 1 in order to vent Chamber 2. It was found that the J$_{sc}$'s are usually the lowest in the run after venting. The J$_{sc}$'s then increase progressively as we move further into the run sequence. This effect is depicted in Table 5.10.

A plausible explanation could be that the water vapor is causing the lowering of J$_{sc}$'s. The level of water vapor is possibly reducing as we move further into the run sequence leading to a increase in J$_{sc}$. The spectral responses for these samples
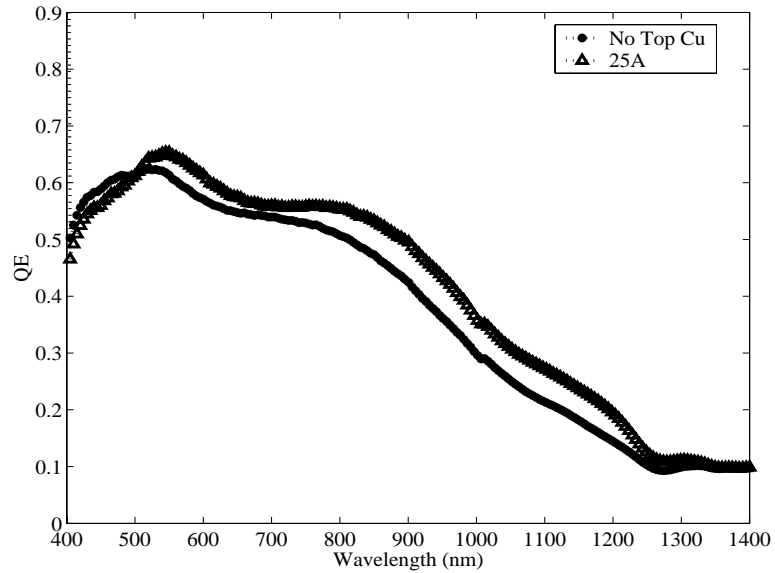
Figure 5.46 Effect of Top Copper on $\mathbf{J}_{sc}$

Table 5.10 Effect of Venting on $\mathbf{J}_{sc}$

Sample No.	Run No.	$\mathbf{J}_{sc}$ (mA/cm^2)
289-03	1	30.5
290-25	3	40.7
291-15	5	38.7

are shown in Figure 5.47. This effect is repeatable and probably has the maximum effect on Ga deposition in Chamber 1. Chamber 1 does not have a cold trap unlike Chamber 2 and may thus take a longer time to pump out any residual moisture. Chamber 2 was modified to incorporate a vent valve so that Chamber 1 need not be vented unless necessary.

The same effect is depicted in Table 5.11 and Figure 5.48. The V_{oc}'s are however unaffected by the run sequence.
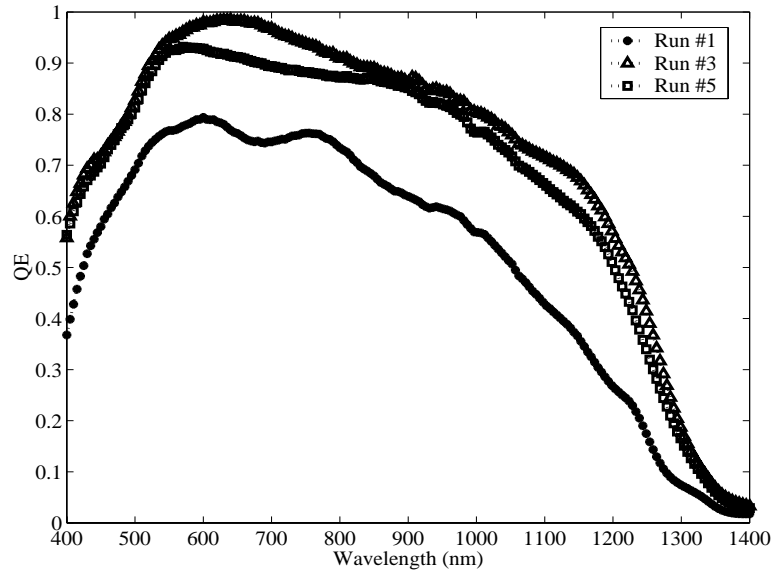
Figure 5.47 Effect of Venting on J$_{sc}$
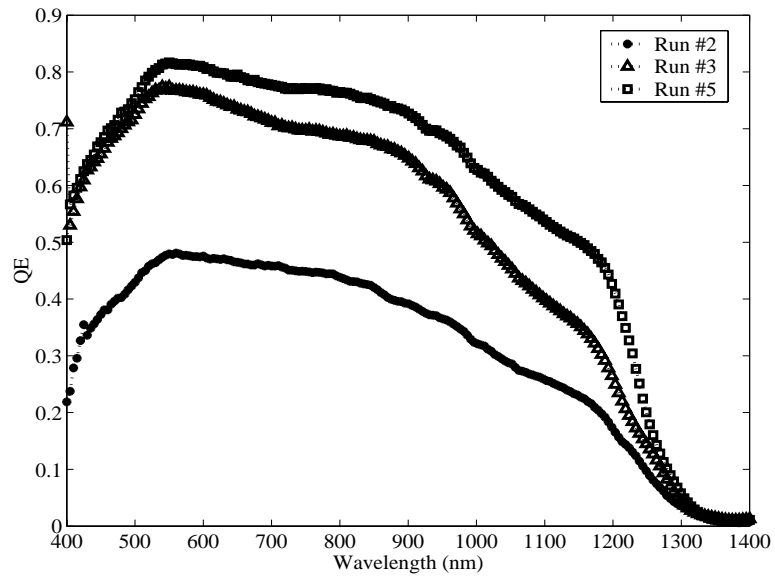
Figure 5.48 Verification of the Effect of Venting on J$_{sc}$'s

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Table 5.11 Effect of Venting on Cell Parameters

Sample No.	Run No.	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)
293-18	2	18.6	440	54.7
294-23	3	29.7	450	60.6
295-12	5	33.3	440	58.8

5.6.6 Effect of Increased Cu Level

Figure 5.49 shows V_{oc} distributions for samples 335 and 336. Sample 335 is a standard sample while the Cu level is increased by about $150\overset{\circ}{A}$ for sample 336.

Cu Source

430	420	410	390	350
410	400	380	410	430
440	420	400	400	410
430	420	420	420	410
420	420	380	410	400

In Source

(a)

Cu Source

50	X	X	X	X
350	320	350	310	330
350	360	360	370	350
330	290	350	350	330
230	320	290	240	250

In Source

(b)
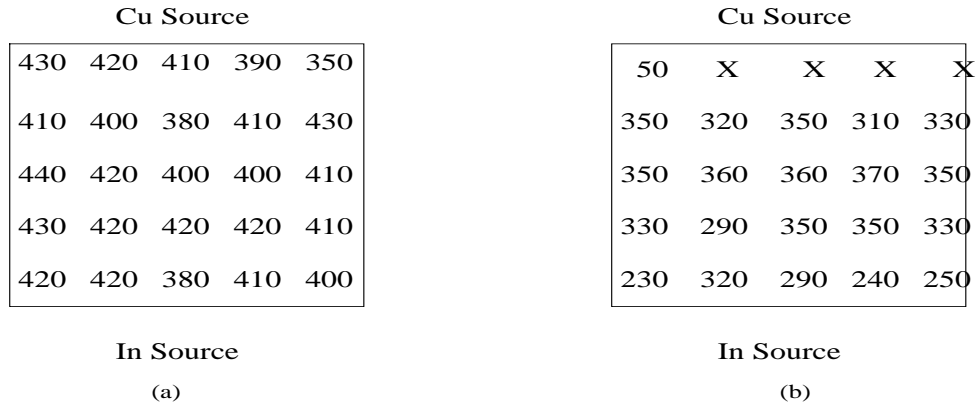
Figure 5.49 V_{oc} Distribution of Samples (a)335 and (b)336

It can be seen that the sample has become Cu-rich and the V_{oc}'s have dropped by 80 mV. The devices on the first row are shorted out due to the excess Cu. The J_{sc}'s on the other hand, show a considerable improvement as seen in Figure 5.50. The increased Cu level has led to the formation of a film with better transport properties.
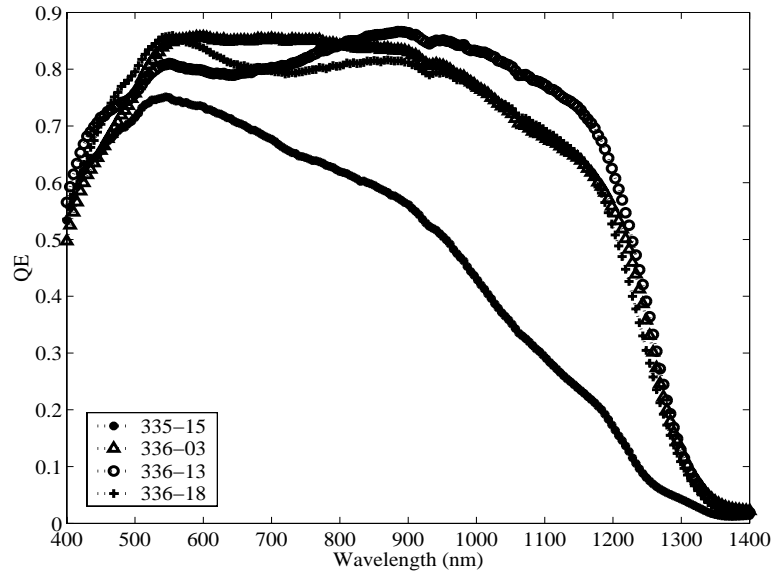
Figure 5.50 Effect on Increased Bulk Copper Thickness on J_{sc}

5.7   Type IB Precursor (Cu in Chamber 2)

In these precursors, the Cu deposition is carried out in Chamber 2 followed by the Ga deposition in Chamber 1. The precursor is then completed by the deposition of In_2Se_3 in Chamber 2. The precursor is then selenized in Chamber 2.

5.7.1   Run Sequence Effects

5.7.1.1 V_{oc} Variations

It can be seen from Table 5.12 that the V_{oc}'s are affected dramatically whenever C1 is vented before a run. The V_{oc} is not affected as much when C2 alone is vented. This then suggests that the Ga deposition is adversely affected due to venting of C1. This could be either due to water vapor in the Chamber or could possibly be due to oxidation of Ga source. The same effect is depicted in Figure 5.51.

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Table 5.12 Effect of Chamber Conditions on Open Circuit Voltage

Sample No.	Chamber Condition	V_{oc} (mV)
312	C1,C2 Vented	Peeled
313	Run 2	330
314	Run 3	440
315	Run 5	440
316	C1,C2 Vented	370
317	Run 2	370
318	C1,C2 Vented	390
319	Run 2	450
320	C2 vented	430
322	Run 3	440
323	Run 2	470

5.7.1.2 Bandgap Variations

Chamber venting also has an impact on the bandgap of the absorber. The first run after venting C1 and C2 has a low (CIS) bandgap while there is a pronounced bandgap shift as we proceed further in the run sequence. The bandgap shift could be again be attributed to the water vapor in C1 affecting the Ga deposition. The shift in the bandgap also explains the spread of V_{oc}'s as we proceed from Run 1 to Run 5. The spectral responses of these samples depicting this effect is shown in Figure 5.52. It is also interesting to note that higher bandgaps were not achieved when Cu was deposited in C1 in a Se-free environment.

The same effect is shown in Figure 5.53. A comparison of spectral responses is done in the case where C2 alone is vented, as in sample 320. There is still a bandgap shift, however a secondary low bandgap phase is also evident from the plot. Based on these plots it can be concluded that venting of C1 prior to the run, has a greater impact on the bandgap shift as opposed to venting C2.

Figure 5.54 shows the effect of background Se on Cu deposition. The Cu deposition is done in C2 for sample 315 while the Cu is deposited in C1 in a Se-free environment

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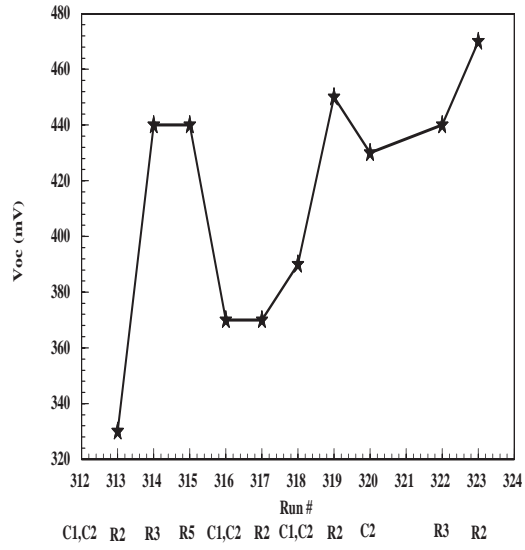
Figure 5.51 Effect of Chamber Conditions on V$_{oc}$
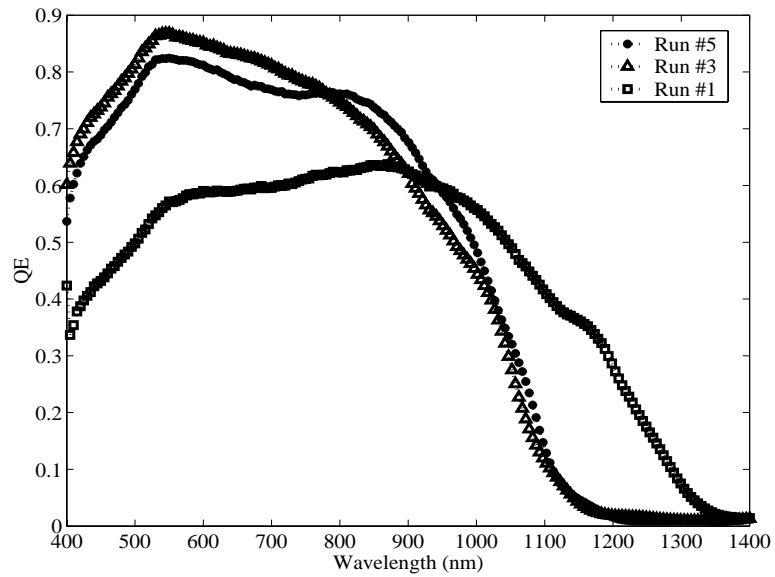
Figure 5.52 Spectral Responses Showing Bandgap Variations
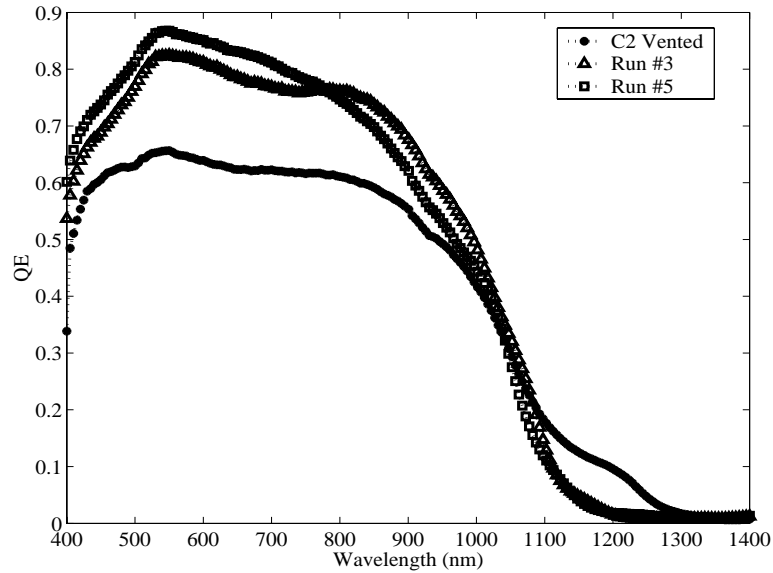
Figure 5.53 Verification of the Spectral Responses Showing Bandgap Variations

for sample 290. Both runs were well into run sequence where the effect of moisture, if any is minimal. A dramatic shift in the bandgap is seen when the Cu is deposited in the Se chamber. This then suggests that the presence of Se in the Cu film leads to a better incorporation of Ga, resulting in increased bandgaps.

Figure 5.55 shows the V_{oc} distribution of samples 323 and 294. Sample 323 is a standard Type IB device while sample 294 is a standard Type IA device. The V_{oc}'s are pretty uniform for sample 294, while sample 323 exhibits a spotty behavior. The Cu thickness used in Type IB results in metal ratios exceeding unity. Since these devices are not shorted out, some of Cu is probably tied up as $Cu_{2-x}Se$ species, away from the junction and not fully converted into CIGS. This could explain some of the spotty behavior of these samples.

So the higher bandgaps of Type IB samples could be due to a combination of higher Cu/In ratios and the presence of Se during Cu deposition. In order to evaluate the performance of the devices with metal ratios close to unity, sample 337 was processed

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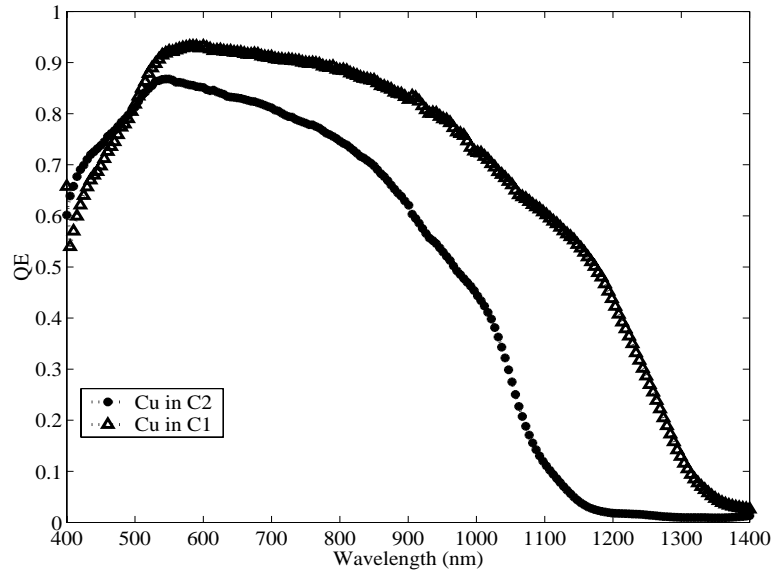
Figure 5.54 Effect of Presence of Se During the Copper Deposition on J_{sc}'s

Cu Source

410	430	420	400	390
430	440	440	450	430
440	440	400	450	330
0	320	410	400	470
270	200	240	290	330

In Source

(a)

Cu Source

440	440	420	440	430
450	440	440	450	460
460	440	430	450	450
450	450	450	X	430
0	450	440	450	450

In Source

(b)
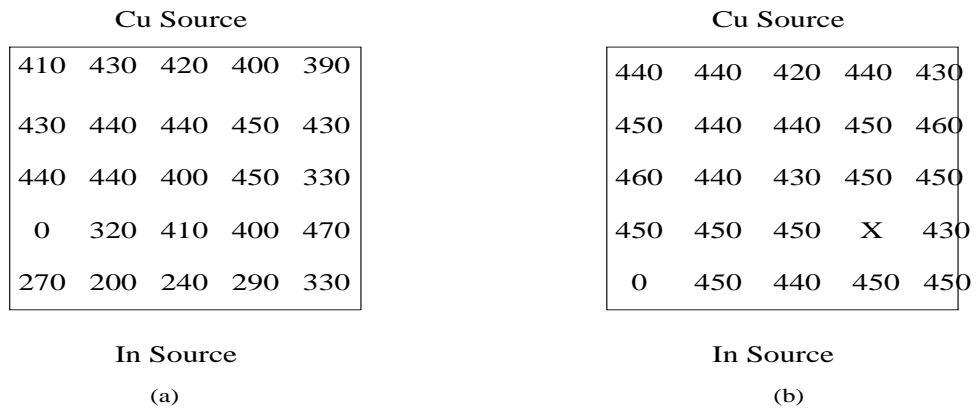
Figure 5.55 V_{oc} Distribution of Samples (a)323 (b)294

with a lowered Cu level. The performance of the device was very poor as seen in Figure 5.56. This confirms that all the copper is not converted into CIGS and hence, a higher Cu level than that is required for metal ratios of 1, is needed to get good performance.

Cu Source

100	290	210	300	220
240	270	270	320	090
270	100	200	160	150
320	250	220	220	070
140	050	110	060	X

In Source
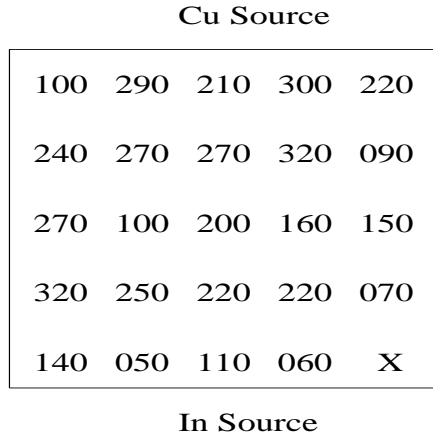
Figure 5.56 V_{oc} Distributions of Sample 337

5.7.2 Effect of Ar Annealing

Table 5.13 Effect of Ar Annealing

Sample No.	Ar Anneal	Cool Down Temp (^oC)	V_{oc} (mV)	J_{sc} (mA/cm^2)
324-23	NO	-	450	-
324-12	NO	-	430	35.1
325-15	NO	-	430	-
326-17	YES	250	140	-
327-23	YES	150	470	28.8
328-16	YES	200	360	-
330-12	NO	-	480	-
330-23	NO	-	450	30.8
331-23	YES	150	450	28.5
331-14	YES	150	400	30.0

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A series of experiments were carried out in which the absorber was annealed in an Ar ambient at the end of the run. The sample was cooled down to various temperatures and then reheated to 500° C in an Ar ambient. The partial pressure of Ar is maintained at 2.5mT. The time of stay at 500° C is 10 minutes. Table 5.13 shows the effect of Ar anneal conditions on the V_{oc}. When the sample is cooled down to 250° C and then reheated to 500° C the device performance is very poor. The V_{oc}'s increase as the sample is cooled down to 200° C and then to 150° C. When the sample is cooled down to 150° C before the Ar anneal, the V_{oc}'s are comparable to the standard devices. The Ar anneal was done in order to improve the homogeneity of the film. Spectral responses of standard samples showed the presence of secondary phases. These were subsequently removed by the Ar anneal. This effect is depicted in Figure 5.57. This experiment was repeated and the results were verified.
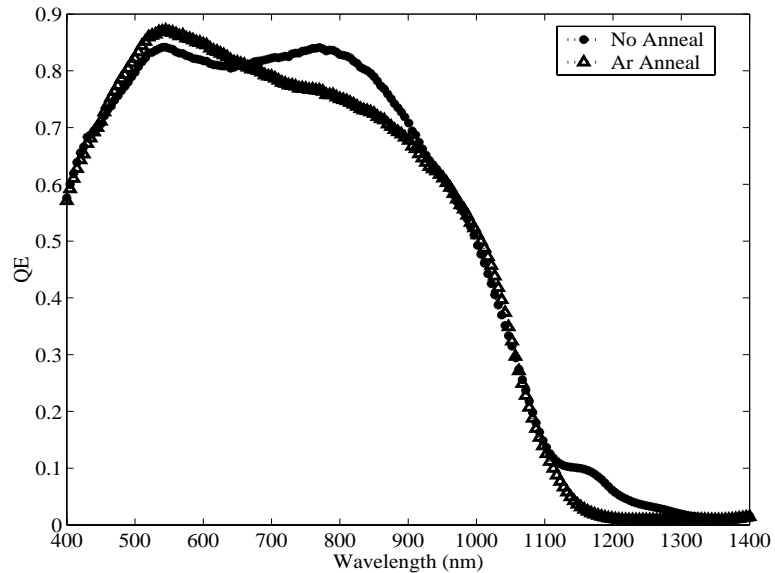
Figure 5.57 Effect of Argon Anneal on J_{sc}'s

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5.7.3 ZnSe Buffer

Sample 332 was cut into two halves after the CIGS deposition. CBD CdS was then deposited on one half while a ZnSe buffer was evaporated onto the other half. The substrate temperature during the ZnSe deposition was 200° C. The thickness of the buffer layer was $300\mathring{A}$. A bilayer ZnO was then deposited on both halves in a single run. The V_{oc}'s of both halves are comparable as seen in Figure 5.58. However, the short circuit currents were extremely low for the ZnSe buffer layer. This could be because of the high resistivity of the ZnSe buffer. The substrate temperature of 200° C during the ZnSe may have also had a detrimental effect on the I_{sc}'s. These results were repeatable.

CdS   ZnSe

390	340	330	310	350
330	270	340	320	360
360	340	350	370	360
360	310	330	370	360
300	230	270	380	350

Figure 5.58 V_{oc} Distribution of Sample 332

5.7.4 Impact of Substrate Cleaning Solvents

The substrate cleaning solvent predominantly used in our lab was 1,1,2- trichlorotri-fluoroethane (TCFE). This solvent was extremely expensive and also required EPA approval. So different solvents were tried to replace the TCFE. The substrate for sample 352 was cleaned using a combination of trichloroethylene (TCE) and TCFE. This sample had a performance which was comparable to our standard runs as seen

from Figure 5.59. From this experiment, it can be deduced that TCE does not affect device performance.

Cu Source

420	420	410	410	370
430	430	410	390	410
440	430	400	420	420
420	430	350	400	390
340	360	260	270	130

In Source

Figure 5.59 V_{oc} Distribution of Sample 352

The TCFE was then replaced by methanol for sample 354. The Moly appearance was bad and it had visible spots on its surface. The device performance took a turn for the worse as seen in Figure 5.60. So the use of methanol was discontinued.

Cu Source

320	270	270	340	340
300	300	290	300	200
290	330	250	320	310
290	330	300	250	260
210	320	290	200	210

In Source

Figure 5.60 V_{oc} Distribution of Sample 354

The TCE and TCFE combination was eventually replaced by propanol for sample 357 which showed a good performance in terms of V_{oc}'s. The V_{oc} distribution for

this sample is shown in Figure 5.61. The V_{oc}'s are similar to those obtained with the standard cleaning process.

Cu Source

440	440	440	420	320
430	430	430	420	420
330	420	410	410	410
330	360	270	340	310
120	160	300	230	220

In Source

Figure 5.61 V_{oc} Distribution of Sample 357

5.7.5   Influence of Moly Deposition Conditions

Sample 360 used a Mo coated substrate deposited from a new Molybdenum target. The sputtering voltage of the Mo deposition is a critical parameter controlling the stress in the film. Good Mo films are prepared by maintaining a sputtering voltage of 450V. However, the new target had a discharge voltage of 600V probably leading to excessive compressive stress in the film. The deposition rate also dramatically reduced to 1.3 $\mathring{A}$/s, while the standard Mo runs have depositions rates of 3.0$\mathring{A}$/s. This resulted in poor performance of the device as seen in Figure 5.62. The high sputtering voltage combined with the lower deposition rates could have affected Na diffusion from the glass, thereby affecting the V_{oc}'s.

The Mo thickness was reduced to 6000$\mathring{A}$ for sample 369. The first layer thickness was left unchanged at 3000$\mathring{A}$, while the low pressure layer thickness was reduced from 7500$\mathring{A}$ to 3000$\mathring{A}$. The V_{oc}'s of this device was comparable to that of a standard one

Cu Source

330	380	380	380	380
360	370	370	370	370
340	360	380	380	370
370	360	370	370	370
360	360	340	370	310

In Source

Figure 5.62 V_{oc} Distribution of Sample 360

fabricated on the standard Mo (sample 368). This can be seen from Figure 5.63. The J_{sc}'s on the other hand, have considerably reduced as seen in Figure 5.64.

Cu Source

420	420	410	400	440
420	410	400	410	430
420	400	400	420	420
360	420	420	420	420
420	410	420	410	390

In Source

(a)

Cu Source

420	420	430	430	440
420	410	420	430	440
420	420	410	410	430
420	420	400	410	420
430	420	410	430	430

In Source

(b)

Figure 5.63 V_{oc} Distributions of Samples (a)368 (b)369

The I-V curves shown in Figure 5.65 exhibit kinks as well as crossover between the light and dark curves. This could be due to the presence of a back contact diode instead of a true ohmic contact between the Mo and CIGS. This could also explain the lower J_{sc}. This experiment needs to be repeated to verify the results.
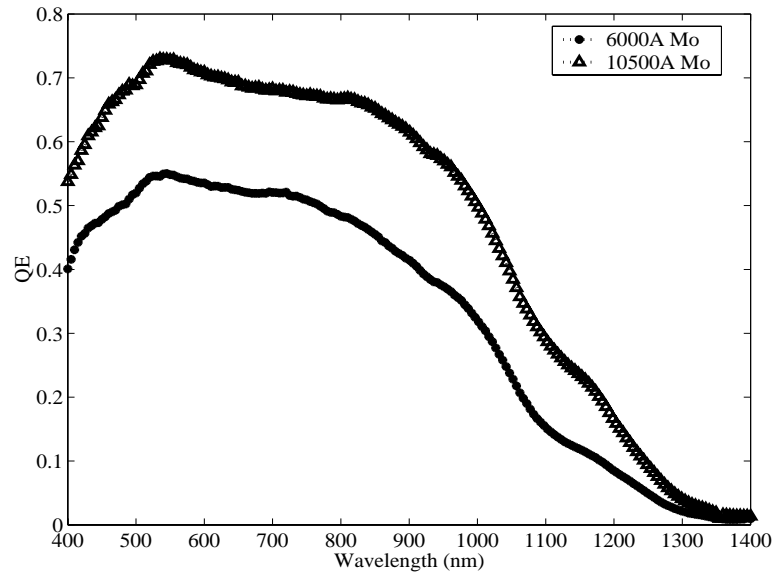
Figure 5.64 Effect of Moly Thickness on J$_{sc}$
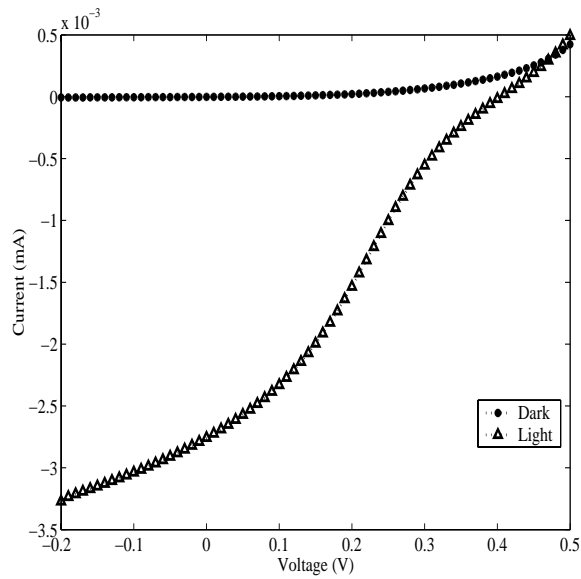
Figure 5.65 Dark and Light I-V Curves of Sample 369

5.7.6 Effect of Selenization Time on Device Performance

Sample 364 was a Type IB device where the selenization time was increased by 4 minutes at the end of the run. The V_{oc} distribution for this sample is shown in Figure 5.66. The V_{oc}'s have decreased by nearly 100 mV when compared to a standard run. So the excess selenization time has hurt the device performance probably by forming some Se-rich species on the surface of the film.

Cu Source

340	320	280	320	310
320	330	320	270	270
340	230	330	260	240
320	330	330	310	230
320	320	290	270	210

In Source

Figure 5.66 V_{oc} Distribution of Sample 364

The selenization time was reduced by 4 minutes at the end of the run for sample 366. The V_{oc} distribution for this sample is shown in Figure 5.67. The V_{oc}'s dropped a little, however, the sample exhibits spotty behavior. In this case, we are probably removing some Group III material from the film as the substrate temperature is 500° C when the Se is shut off. These experiments have shown that the 28 min profile used in the standard runs is optimal.

Cu Source

420	410	280	240	220
360	360	410	410	380
310	340	410	280	390
390	330	370	320	360
140	220	180	220	190

In Source

Figure 5.67 V$_{oc}$ Distribution of Sample 366

CHAPTER 6

CONCLUSIONS AND RECOMMENDATIONS

The research has demonstrated that high quality CIGS films can be fabricated by a simple two-step manufacturing-friendly process of selenizing a metal precursor. The effective bandgap of the devices is not significantly increased even by depositing as much as 20% Ga in the Type I(Sputtered Ga) precursor. The Ga tends to segregate to the Mo interface and hence there is very little alloying in the space charge region. The presence of Ga, however, improves the properties of the resulting film. The Ga helps in passivating point defects and also creates a graded bandgap structure aiding in the collection of carriers by means of a back surface field. In addition, Ga improves the adhesion of the CIS layer to the Mo back contact. The ability to deposit Ga by sputtering was also demonstrated.

The Type I process provides good control as well as good reproducibility of results. A thin layer of top Cu(50 to 75 $\mathring{A}$) during selenization improves the device performance. The Se flux is maintained constant making the process relatively simple. Significantly high short circuit current densities(40 mA/cm^2) are routinely achieved with the highest conversion efficiency of 13%. The typical V_{oc}'s are 450 mV with the highest at 495 mV. The FF's are typically around 65% with the highest at 68%. V_{oc}'s seem to show a peak around a Cu/(In+Ga) ratio of 1.00. Additional variables also have an influence on the V_{oc}'s, the most prominent among them being the Cu/In ratio. In addition, the V_{oc}'s depend upon the Se flux, provided the metal ratio is in a good range. In cases where the Se flux is constant the V_{oc}'s seem to show a direct

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dependence on the metal ratio. The J_{sc}'s, on the other hand, do not seem to be overly sensitive to the metal ratio provided that the metal ratio is above 0.75. There is a minimum amount of Se flux that needs to be delivered to the substrate below which the device performance is poor. Lack of Se also leads to peeling of films. Films generally tend to be rougher in regions away from the Se source. This can be inferred from the absence of interference peaks in the spectral responses of the devices away from the Se source.

There is not much room for improvement in J_{sc}'s, however, the V_{oc}'s can be increased by another 40 mV. This increase in V_{oc} is also expected to result in an increase in FF. The results indicate that losses in the space charge region limit the cell efficiency. This then hints that further improvements are needed to optimize the surface properties of the film. A top Cu thickness of around $75\mathring{A}$ gives us optimum performance in regions near the Cu source. It is found that depositing the top Cu at 550° C resulted in better performance as opposed to the top Cu deposition at 450° C. This could be either due to the selenization details or it could just be a temperature effect. It may be necessary to deposit the top Cu at a lower temperature during cooldown to separate the two effects. Experiments need to be done to improve the fill factors of the devices. Optimization of the junction and window layers also need to be done.

The performance of Type I evaporated Ga films showed a strong dependence on Ga thickness. When the Ga thickness exceeded $800\mathring{A}$, current densities suffered as a result of poor transport properties of the film. At a Ga thickness of $800\mathring{A}$, current densities comparable to Type I sputtered Ga films were achieved. The V_{oc}'s on the other hand, were not overly sensitive to the Ga thickness. In general, the V_{oc}'s of the evaporated Ga films were lower than that of sputtered Ga films by about 40mV. This is due to the fact that the bandgap of these films is not increased as opposed to the sputtered Ga films, where there is a small increase in bandgap leading to higher V_{oc}'s.

Higher substrate temperatures need to be employed during Ga deposition in order to achieve higher bandgaps. The Ga layer can also be split into two parts to achieve this. This may lead to higher V_{oc}'s without any significant loss in J_{sc}'s thereby improving overall device performance.

The Type I evaporated Ga devices were also sensitive to the intrinsic ZnO thickness. The I-V curve shapes and the fill factors suffered when intrinsic ZnO thickness exceeded $400\mathring{A}$. The intrinsic ZnO thickness of $400\mathring{A}$ gave good reproducible results. The junction layer (CdS) has to be optimized to improve the overall performance of these devices.

Type II devices showed a dependence on the Ga thickness. The best V_{oc}'s were achieved for a Ga thickness of $800\mathring{A}$, while the V_{oc}'s are extremely poor at a Ga thickness of $200\mathring{A}$. However, the J_{sc}'s increase as the Ga thickness is lowered. This then indicates that the excess Ga is improperly bonded or does not bond at all leading to poor electronic properties. The current densities of Type II devices were improved by using a higher selenization temperature of 575° C, without any loss in V_{oc}. Longer selenization times (14 min at 550° C) resulted in a remarkable improvement in device performance. The bandgap of the absorber increased leading to higher V_{oc}'s. The current densities also increased. J_{sc}'s of $34.1\mathrm{mA/cm^2}$ were measured, which are the best for our Type II devices. Spectral responses were square indicating good current transport properties. The V_{oc}'s however showed a preference to the Se side and were generally poor in regions away from the Se source. The optimal time of stay at 550° C may be between 7-14 mins. Experiments have to be done in order to establish the optimal time where improved J_{sc}'s can be obtained along with uniform V_{oc}'s.

The V_{oc}'s of Type II devices were improved by modifying the base process and splitting the Ga layer into two parts. This led to V_{oc}'s of 485mV which were the best V_{oc}'s achieved for Type II devices in this research. This improvement could

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be attributed to the better Ga incorporation at higher substrate temperatures. The split Ga and selenization experiments have to be combined in order to improve device performance further. Device efficiencies exceeding 14% are possible if V_{oc}'s of 600mV and J_{sc}'s of 34mA/cm^2 and FF's of 70% are obtained. The order of In/Ga depositions seemed to control the V_{oc}. V_{oc}'s were lowered when In deposition followed the Ga deposition while the V_{oc}'s were higher when the Ga deposition followed the In deposition.

Type III precursors were not overly sensitive to the Ga thickness. Ar annealing of these films resulted in J_{sc}'s of 35.4mA/cm^2. However, the V_{oc}'s suffered as a result of anneal indicating that the top surface of the film was probably damaged due to the anneal. The time and temperature of the anneal have to be varied to fully understand the role of the anneal.

The split Ga Type III devices showed an increase in V_{oc} of around 100mV. These were the best V_{oc}'s achieved in this research. The higher V_{oc}'s are a result of an increased bandgap. The J_{sc}'s on the other hand, suffer from poor transport properties probably due to some improperly bonded Ga.

Split Ga Type III runs employing longer time of stay at 550° C resulted in devices with V_{oc}'s of 560mV. The J_{sc}'s however did not improve. This could be due to the fact the Ga was not given enough time to react completely as it was deposited between the 21st and 24th min of selenization. Further experiments have to be done where the 450° C step during selenization is eliminated and deposition of Ga has to be carried out around the 14th min to give it enough time to react completely. Light soaking of Type II and Type III samples resulted in improvement of V_{oc}'s. This indicated the presence of defects at the interface which were passivated by the light soaking.

Type IA devices fabricated in the new in line evaporator system showed a strong dependence on the Ga thickness. The V_{oc}'s increased as the Ga thickness was var-

ied from $450\AA$ to $350\AA$. Ga thicknesses between $350\AA$ and $200\AA$ did not have any significant effect on the V_{oc}'s. The J_{sc}'s increased as the Ga thickness was lowered from $450\AA$ to $200\AA$. The Ga level was finally optimized at $200\AA$. The device performance was found to be optimized when Ga thickness of $200\AA$ was used along with an In thickness of $6500\AA$, a top selenization temperature of 550° C and a top copper of $25\AA$. The J_{sc}'s in these devices depended strongly on the chamber conditions and improved considerably as we moved further into the run sequence. There is no bandgap increase in these devices indicating the absence of Ga in the space charge region. The highest V_{oc} achieved in these samples was 460mV and the highest J_{sc} was 40.7mA/cm^2, though not on the same substrate. The V_{oc}'s are pretty reproducible while there is a spread in the J_{sc}'s. Top Cu thickness and time of top Cu deposition have to be varied to further improve device performance. Cu and Ga coevaporation as well as Ga and Se coevaporation have to be tried to fully understand the mechanisms controlling device performance.

We thought that the absence of Se during the Cu and Ga depositions would aid in improving the V_{oc} of our Type I devices. This indeed turned out to be true since the V_{oc}'s were about 30mV higher in the in-line evaporator (with the Cu and Ga being deposited in Chamber 1 in a Se-free environment), as compared to Type I evaporated Ga devices fabricated in the four source evaporator. There was no evidence of a bandgap shift in both these cases. The absence of a bandgap shift in the four source evaporator could be attributed to the presence of moisture/oxidation of the Ga source since the chamber is vented after every run.

The sputtered Ga films in the four source evaporator showed a slight increase in bandgap. This indicates that the sputtering process ensures better removal of the oxide from the surface of the Ga source as opposed to the evaporation process. The slight increase in the bandgap helped in increasing the V_{oc}'s without affecting the

J_{sc}'s. On the other hand, absence of Se during the Cu deposition in Type IA devices prevent the increase in bandgap of the films fabricated in the in-line evaporator. The V_{oc}'s in the in-line evaporator are higher than the V_{oc}'s of the Type I evaporated Ga films fabricated in the four source evaporator. However, the J_{sc}'s are generally lower in the Type IA devices except for a few cases. The Type I evaporated Ga devices consistently had high values of J_{sc}'s (as high as $42mA/cm^2$). This indicates that the current transport properties of the Type IA films are inferior to that of the Type I evaporated Ga films. More experiments are required to explain the mechanisms that limit J_{sc}'s.

Type IB devices were sensitive to the chamber conditions as well. The bandgap and V_{oc} are adversely affected whenever Chamber 1 is vented prior to a run. The loss in performance is either due to the presence of water vapor during Ga deposition or could be due to the oxidation of the Ga source itself. The V_{oc}'s increase as we go further in the run sequence. This increase in V_{oc} can be attributed to the bandgap increase. However, the V_{oc}'s are not significantly affected when Chamber 2 alone is vented prior to a run. The spectral response indicate a thin low bandgap phase along with a dominant higher bandgap phase. The increase in bandgap of these devices can be attributed to the presence of Se during copper deposition and higher Cu/In ratios. Ar annealing of these samples resulted in improved homogeneity of the film without any loss in V_{oc}. The best V_{oc}'s achieved for Type IB devices were 480mV and the best J_{sc}'s were $35.1mA/cm^2$ and the best fill factors were 66%. These values are the best values obtained from different substrates. A 28 min selenization time for these devices was found to be optimal.

The presence of Se during the Cu deposition in the Type IB resulted in bandgaps of around 1.1eV. This corresponds to an increase in bandgap of 150meV from the CIS bandgap of 0.95eV. This increase in bandgap does not translate into a substantial gain

in the V_{oc}'s. It was found that the V_{oc}'s improved by only 20mV when compared with the Type IA devices (with bandgaps of 0.95eV). This loss in V_{oc} of Type IB devices can be attributed to recombination due to point defects in the space charge region. The increase in bandgap is also detrimentally affected by the moisture/oxidation of the Ga source. An interesting observation is that the evaporated Ga produces either a dramatic shift in the bandgap or does not result in a bandgap shift at all. On the contrary, the sputtered Ga films are capable of producing a continuum of small bandgap shifts. Based on the observations, an atomic level model is proposed. The presence of Cu-Se and non-oxidized pure Ga are essential to produce bandgap shift in Type I devices. Furthermore, presence of Se in the Cu film probably results in a better bonding of the Ga to the Cu.

ZnSe buffer layers were studied. The V_{oc}'s of the devices with buffer layers were comparable to the CdS control samples. However, the I_{sc}'s of these devices were extremely poor. The substrate temperature during ZnSe deposition as well as the ZnSe buffer thickness have to be varied so as to improve I_{sc}'s and the cell efficiency. Device performance was also found to be sensitive to the solvent used for substrate cleaning. Propanol did not affect the V_{oc}'s while methanol severely limited device performance. The molybdenum sputtering voltage, sputtering rate and the thickness had significant influence on device performance. These parameters control the Na diffusion from glass and the stress in the molybdenum film. If these parameters are not at optimum value, then device performance can be significantly hampered. More experiments have to be done to isolate the effect of each of these parameters on the device performance.

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