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Synthesis of Nanoscale Structures in Single Crystal Silicon Carbide
by Electron Beam Lithography

by

Jay A. Bieber

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Engineering Science
Department of Electrical Engineering
College of Engineering
University of South Florida

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Keywords: nanotechnology, scanning electron microscopy, NEMS, SiCNDs, low
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Synthesis of Nanoscale Structures in Single Crystal Silicon Carbide

by Electron Beam Lithography

Jay A. Bieber

ABSTRACT

Nanostructures were formed on diced specimens of several silicon carbide polytypes and silicon using electron beam lithography. A general introduction to nanostructure synthesis and electron beam lithography, are presented. A scanning electron microscope was retrofitted with a commercially available electron beam lithography package and an electrostatic beam blanker to permit nanoscale lithography to be performed.

A process was first developed and optimized on silicon substrates to expose, poly-methyl-methacrylate (PMMA) resist with an electron beam to make nanoscale nickel masks for reactive ion etching. The masks consist of an array of nickel dots that range in size from 20 to 100 nm in diameter. Several nanoscale structures were then fabricated in silicon carbide using electron beam lithography. The structures produced are characterized by field emission Scanning Electron Microscopy.

Chapter 1

Introduction

1.1 Nanotechnology

The prefix nano comes from the Greek word for dwarf. The term is commonly used in mathematics and is a short notation used when we want to divide a unit by one billion. In terms of a power of ten it is denoted by 10^{-9} and is a number so small it is very difficult to conceptualize. As an example, lets assume a technology where discovered which allowed a telescope to be built with enough resolving power to see a coin the size of a quarter dollar on the surface of the moon. The moon, which has a diameter of 3,474 kilometers, subtends an arc of 0.5 degrees in the sky as observed from the surface of the earth. A quarter, which has a diameter of about 2.5 cm, on the moons surface will then subtend an angle of 3.6×10^{-9} degrees, or 3.6 "nano" degrees as seen from earth. This is the scale of nanometers (nm). Nanotechnology, then, as its name implies, is the science of making and manipulating structures, which are measured on a scale of 10^{-9} meters. These "nanostructures", are defined as groups of atoms or molecules, having dimensions between 1 and 100 nm in size.

On the nanoscale, the smallest structural units of matter are atoms and molecules. As we approach the nanoscale, entirely new physical properties emerge which are governed by quantum mechanics. Once we are able to control matter on the nanoscale to take advantage of these new properties, the commercial applications are limitless. One example of a device, which is currently in large-scale production, is the giant

magnetoresistive (GMR) sensors used in modern computer hard disks. GMR sensors were developed from the field of magnetoelectronics, which is the study of how the spin of electrons can influence electronic properties and transport. GMR sensors, also known as spin valves, are comprised of alternating layers of ferromagnetic and non-ferromagnetic layers several nanometers thick. When exposed to a magnetic field these layers exhibit an increase in resistance as much as 10% due to a split in the density of states available for spin up and spin down electrons [1].

In the last few years, the U. S. government has recognized the potential of nanotechnology to help the economy and for national security, by supporting the National Nanotechnology Initiative (NNI). This is a federal R&D program established to coordinate the multi-agency efforts in nanoscale science, engineering and technology. The 2005 budget for this initiative provides over $1 billion dollars, which is double the amount in 2001, which was the first year of its inception. Miniaturization of electronic components also continues to be a major driver of work in this area. Since the 1960s, much of the work toward the development of tools and techniques to build small structures has been done by the semiconductor industry during the development of integrated circuit technology. As long as the demand for smaller personnel computers and electronic gadgets such as digital cameras and cell phones continues to increase, so will funding in nanoscale R&D.

1.2 Research Objective

In order to manipulate and build structures with nanometer dimensions, we must first have a device which can image objects on this size scale. The scanning electron

microscope, or SEM, is one of the first tools developed that is capable of viewing and measuring nanometer size structures. Early work describing the construction of the scanning electron microscope was performed in Germany (Knoll, 1935; von Ardenne in 1938) as referenced by P.J Breton in "From Microns to Nanometres: Early Landmarks in the science of Scanning Electron Microscope imaging", [2]. Modern SEMs using aberration corrected electron optics are capable of producing images magnified to 2,000,000 times, (2,000,000X) and have a resolution of 0.6 nm [3].

It is the subject of this thesis research to develop an electron beam lithography (EBL) process to fabricate structures with dimensions less than 100 nm using an electron beam from a modern SEM. A JEOL model JSM-840 SEM was retrofitted with a commercially available electron beam lithography package and an electrostatic beam blanker to permit nanoscale lithography to be performed. A process was developed and optimized first on silicon substrates to expose poly-methyl-methacrylate (PMMA) resist with an electron beam to make nanoscale nickel masks for reactive ion etching of semiconductor crystals. The masks consist of an array of dots, which range in size from 20 to 100nm in diameter. Several of these nanoscale structures were then fabricated in single-crystal silicon carbide substrates. The structures produced were characterized by field emission scanning electron microscopy (FE-SEM).

1.3 Nanosynthesis of Silicon Carbide

Recently there has been intense interest in carbon nanotubes (CNTs), silicon nanowires (SiNWs) and silicon nanodots (SiNDs) because of their unique properties. Prototype nanodevices such as transistors, diodes, switches, light-emitting diodes, lasers,

chemical and biological sensors, etc. have been fabricated from SiNWs and SiNDs [4]. Silicon nanotechnology is of particular interest since these structures would be compatible with and take advantage of, the large existing silicon microelectronics knowledge base. One of the main reasons silicon has dominated as a semiconductor material, is its ability to form a high quality oxide of SiO_2. Since SiC also forms this stable oxide, many of the processes and techniques, which have been developed for nanofabrication in silicon, can in principle be applied to SiC. Thus, as SiC matures as a semiconductor material, it is expected it will also begin to be used more in the manufacturing of microelectronic and nanoscale devices.

1.3.1 Silicon Carbide Overview

Silicon carbide (SiC) is an emerging semiconductor material that possesses high thermal, chemical and mechanical stability. SiC is a indirect wide band gap (WBG) ($E_G > 2eV$) semiconductor, with a range of single crystal polytypes which are now commonly available in 2 and 3 inch wafers. The polytypes include fully cubic (3C-SiC), fully hexagonal (Wurtzite) (2H-SiC) forms, aa well as free-standing substrates of 4H- ad 6H-SiC which have mixed crystal symmetry. These different polytypes arise from a number of combinations of stacked Si-C layers, with partially hexagonal and cubic structure, defined with a hexagonal unit cell (such as 4H, 6H, 8H etc.), or with a Rhombohedral unit cell (such as 15R, 21R, 33R etc.) with a defined degree of hexagonality [5]. Except for the cubic form (3C-SiC) all the remaining polytypes have uniaxial properties. Table 1.1 compares the properties of SiC with silicon and other WBG materials [6]. The SiC nanodots for this work were fabricated on die cut from a 2

inch 4H-SiC wafer manufactured by CREE Inc. [7]. This material has a band gap of 3.26 eV, breakdown voltage of 2.2 x 10^6 V/cm, thermal conductivity of 3-3.8 Watt/cm · K, and a saturation electron drift velocity of 2 x 10^7 cm/sec [8]. Because of the WBG it is possible to operate SiC devices at temperatures as high as 650 °C (glowing red hot!), as opposed to 350 °C for silicon without degradation in electrical performance.

Table 1.1 Comparison of properties of several common semiconductors with SiC [6].

Property	3C–SiC	6H–SiC	Si	GaAs	Diamond
Bandgap (eV)	2.2	2.9	1.1	1.4	5.5
Max. Temperature (C)	873	1240	300	460	1100
Melting point (C)	1800	1800	1420	1240	?
Physical stability	excellent	excellent	good	fair	very good
Electron Mobility (cm^2 /Vs)	1000	600	1400	8500	2200
Hole Mobility (cm^2 /Vs)	40	40	600	400	1600
Breakdown voltage (10^5 V/cm)	4.0	4.0	0.3	0.4	10
Thermal cond. (W/cm C)	5.0	5.0	1.5	0.5	20
Sat. velocity (10^7 cm /s)	2.5	2.0	1.0	2.0	2.7
Dielectric constant	9.7	10.0	11.8	12.8	5.5

1.3.2 Silicon Carbide Nanotechnology

As of the writing of this thesis, the work presented here on the synthesis of silicon carbide nanodots (SiCNDs) by EBL is the first reported. Most of the work involving SiC has been in making microelectromechanical (MEM) systems in the form of micromechanical resonators for RF devices, SiC high power electronics and high temperature gas sensors [9]. Silicon carbide (SiC) is currently under investigation as both

a coating and a structural material for MEMS in harsh environments, due to its superior mechanical strength, chemical stability and excellent performance in high-temperature, high-power electronic components [10]. Figure 1.1 shows an SEM micrograph of a thin polycrystalline SiC coating on silicon using chemical vapor deposition (CVD). These coatings can be used to coat existing MEMS and NEMS devices for use in high temperature applications at 800–1000 °C, or harsh chemical environments. An example of the use of this coating to protect a silicon based mechanical resonator is shown in Figure 1.2. Images a and b show a silicon resonator coated and uncoated, respectively, after being dipped in KOH. As can be seen here the uncoated silicon resonator has been dissolved away while the SiC coated device remains intact.

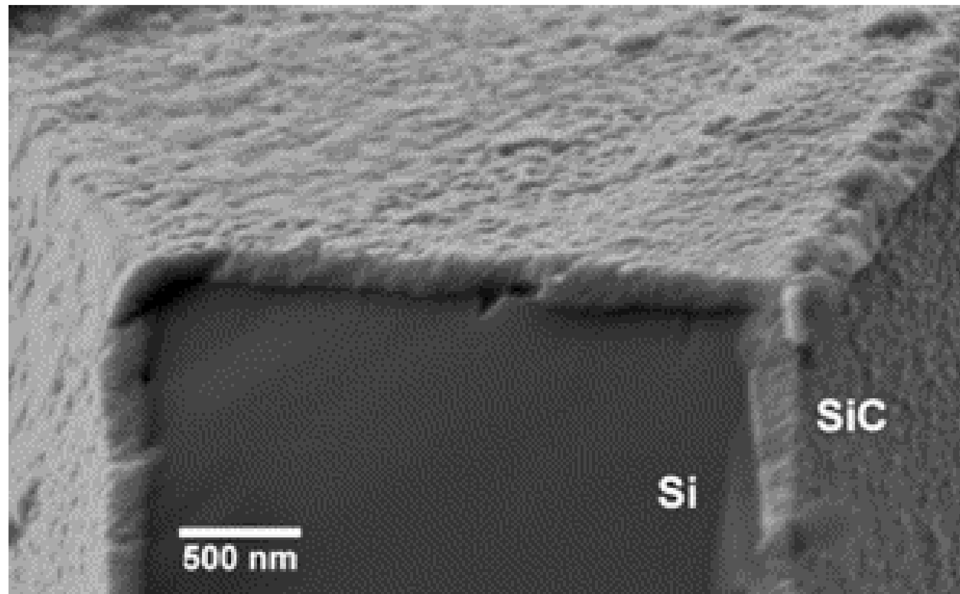

Figure 1.1 SEM micrograph of the cross-section of a thin SiC film deposited on a Si cantilever beam at 800 °C [10].

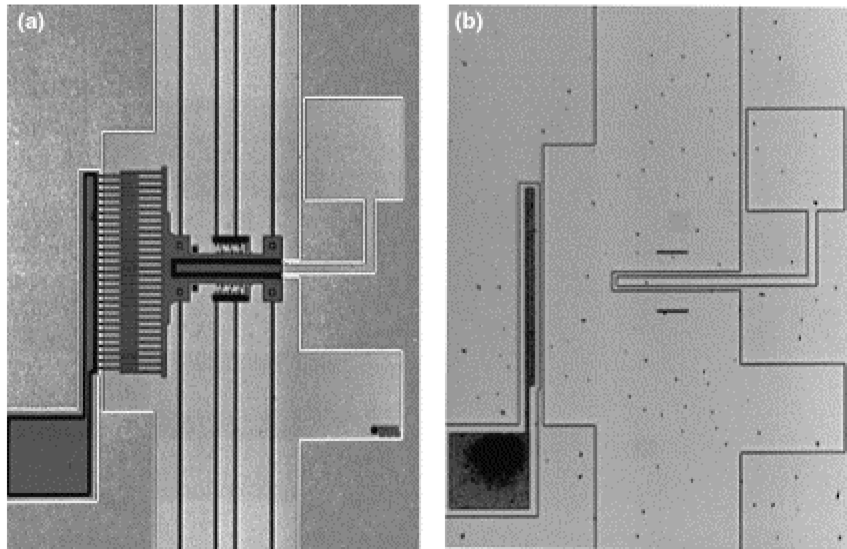

Figure 1.2 Optical images of (a) SiC-coated and (b) uncoated poly Silicon micromachines following immersion in hot KOH solution [10]. Note the SiC resonator is still intact.

1.3.3 Emerging Silicon Carbide Nanotechnology and Devices

SiC based devices are currently being developed which take advantage of the many properties which make it superior to silicon based technologies. Because of its high strength and high acoustic velocity it is being developed for used in high frequency resonators [9]. These include the growth of nanowires or nanotubes for ultra-sensitive detection of chemical and biological species. Adding a coating, which is sensitive to a particular biological or chemical substance, may functionalize cantilevers made from these materials. These substances can be detected by a change in resonator frequency as a result of the mass added to the cantilever when they react with the coating.

The anisotropic properties of low-dimensional nanomaterials such as nanowires, nanorods, nanowhiskers, nanotubes, etc. are highly desirable attributes in the design and fabrication of nanodevices. Nanoelectronic devices such as transistors, logic gates, tweezers, sensors, etc. have already been built from CNTs [4]. Once SiC nanotechnology

matures, it is expected that these same devices will be fabricated in SiC. Work is currently underway to produce SiC nanotubes [11], [12]. SiC nanotubes can also be functionalized and may find use in hydrogen storage applications.

1.4 Summary

As discussed above, to build a materials base for nanotechnology, one needs to control or manipulate the properties, size and shape of materials at the nanometer level. This will be the first topic discussed in Chapter 2 on "Nanopatterning of Semiconductors". A brief summary of the various techniques used in nanopatterning of semiconductors is presented. Optical Lithography is presented in order to provide the background for discussion of EBL. An overview of the SEM and the conversion of the SEM into an EBL system, is also presented in Chapter 2.

In Chapter 3," Synthesis of Nanoscale Structures by Electron Beam Lithography", the details of the nanopatterning technique used in this work are presented. In this chapter the process used to prepare samples for EBL is presented. Work done to develop the reactive ion etch (RIE) process for SiC which is used in this research, is also described.

Because of the highly desirable properties of SiC, as discussed above, this was the material of choice for this work. Chapter 4 "Synthesis and Characterization of Nanoscale Structures in Silicon Carbide" will then focus on work performed at the University of South Florida and will cover the experiments which were performed to optimize the process on silicon, followed by EBL work on SiC to produce SiCNDs. Chapter 5 will present conclusions and future work.

Chapter 2

Nanopatterning of Semiconductors

2.1 Nanopatterning of Semiconductors

In this chapter some of the various methods, which are used to create nanometer size structures, will be reviewed. Most of the techniques outlined here have come about through developments in microelectronics, particularly in silicon integrated circuit technology, which have taken place since the early 1960's. Recent advancement in the areas of microelectromechanical systems (MEMS) and nanoelectromechanical systems (NEMS), have spawned the development of new micromachining and patterning techniques. Some of these emerging techniques are discussed in the sections to follow.

MEMS and NEMS are now used to describe almost any miniaturized device ranging in size from millimeters to the nanometer size scale. These devices may be made from a variety of chemical, electrical and mechanical processes. While most MEMS devices contain some type of micron size mechanical actuator, some may only have a moving charge, such as in a chemical sensor. The structures are made by repeated application of one or more of the basic processes listed in Table 2.1 and, in the order necessary to yield the desired device.

Electron beam lithography (EBL) and reactive ion etching (RIE) are the main processes used in this work. At the present time EBL has proven to be one of the best methods to rapidly build nanoscale device prototypes in semiconductors.

Before we begin, a brief introduction to optical lithography will be presented to outline the motivation for the development of higher resolution technologies. In addition, many standard techniques and technical terms have been carried over to EBL from optical lithography, after many years of development from optical lithography, so this review serves a second important function.

Table 2.1 MEMs processing techniques.

Oxidation [13], [14]	Optical lithography [23]
Wet and Dry Etching [15], [16]	Chemical Mechanical Polishing [24]
Diffusion [17]	Ion beam milling [25]
Physical vapor deposition [18]	Electrochemical deposition [26]
Chemical vapor deposition [19], [20]	Nanotemplating [27]
Ion implantation [21]	Electron beam lithography [28]
Epitaxy [22]	Nanoimprinting [29]

2.2 Optical Lithography

Optical Lithography is a process very similar to photography in which light is used to copy a pattern or image onto another medium. It involves coating a substrate with a liquid "resist", called photoresist, which is a photoactive polymer. Light is then passed through a mask onto the coated substrate. The substrate then undergoes a development process to produce a copy of the mask image onto the substrate. Photo-resists have been used for more than a century to make printing plates for reproducing

text and illustrations. Their current use in the semiconductor industry evolved from their use in the printed circuit board industry since the 1920's.

The most widely available optical lithography system is the contact printer. Many of these instruments have been donated to universities by local industry as they upgrade their equipment to the latest microelectronic fabrication technologies. In contact printing the mask is in direct contact with the substrate during exposure. Contact printing in semiconductor and NEMS fabrication can produce structures down to about 1μm. First the substrate on which the image is to be copied is placed on a turn table and spun at several thousand revolutions per minute. Resist is dripped on to the wafer and wets the substrate as it is spun out to the edge, forming an even layer, typically on the order of 1 to 2 μm thick. The actual thickness of the resist depends on its viscosity, which is a function of the amount of solvent it contains and is inversely proportional to the square root of the spinning speed. The spinning speed and time for a given thickness is specified by the manufacturer of the resist [30].

After spinning, the substrate is then baked to remove the solvent, thus hardening the resist. The term resist applies because the polymer is resistant to chemical reaction when the wafer is put through the subsequent chemical processing steps necessary to produce device structures. When the resist is irradiated with a certain wavelength of light, it becomes soluble in a solvent called a "developer." The developer is commonly an aqueous base such as tetra-methyl-ammonium hydroxide (TMAH). We call the resist "positive" when areas exposed to light energy rinse away to produce openings in the resist. A resist in which all areas except the exposed area rinse away in the developer are termed "negative".

The resist is used to form a pattern which is used to create complex electrical circuits, micro-mechanical devices and structures. The pattern is created by passing light of a particular wavelength through a template or “mask”, which has the desired pattern etched into it. The openings etched in the mask material delineate where the resist is irradiated thus producing a copy of the circuit or microstructure desired. The mask material is typically made from a thin metal film such as chromium deposited on glass, but any material opaque to the light may be used.

In optical lithography the minimum feature size, or resolution, is determined by the diffraction limit and is given by the equation;

$$W = k(\lambda)/NA$$

Where λ and NA are the exposure wavelength and numerical aperture of the optical lithography tool, respectively and k is a process dependant factor that incorporates variables in the system that are not a function of the numerical aperture or the wavelength. The numerical aperture is equal to nsinA, where n is the refractive index, usually 1.0 for air and 2A is the acceptance angle of the mask-imaging lens, as shown in Figure 2.1.

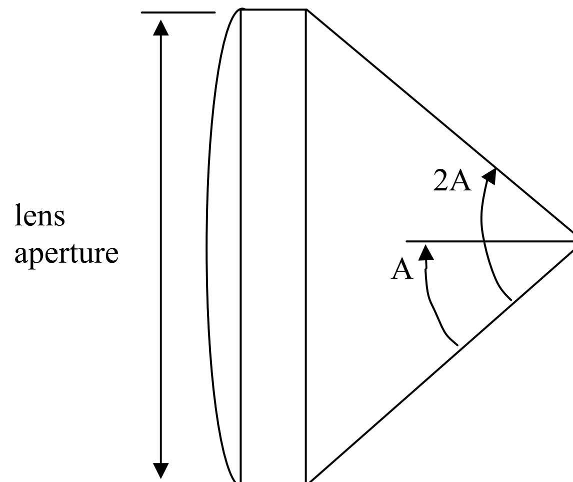

Figure 2.1 Schematic of a lens aperture for a optical system.

The latest optical lithography systems use proximity printing in which the mask pattern is optically projected onto the substrate. The latest proximity systems also use a step and scan approach in which only a small area of the mask is exposed at one time [31]. These systems are capable of resolution just under 200nm. Most integrated circuit manufacturing is currently done in the range of 250 to 350 nm. Optical lithography is considered a high through-put technique since many devices can be made in parallel on the same substrate. The main disadvantage lies in the difficulty of focusing light smaller than the optical wavelengths used due to diffraction limitations.

2.3 Electron Beam Lithography

One way to get resolution below the limits of optical lithography is to use electrons instead of light to expose the resist. Electron beam lithography (EBL) was derived from the Scanning Electron Microscope (SEM), which has been used for many years to define surface features below the limits of optical techniques. The first SEM based EBL systems were developed in the 1960s, shortly after the discovery that the common polymer poly(methyl-methcrylate) (PMMA), or common Lucite Plexiglas TM made an excellent electron beam resist.

The spot size of an electron beam can be less than 5 angstroms, but the resolution is limited due to scattering of the electrons in the resist. Sub-100nm features are routinely produced using this technique. The main problem, however, is that it is a serial process, which limits it use in manufacturing. To write an entire integrated circuit using a scanning electron beam could take hours, as opposed to a few minutes of exposure using mask-based optical lithography systems. Similar to optical lithography systems, EBL

systems are also very complicated and expensive to maintain. EBL systems require almost constant maintenance to keep them operating within specifications. The main advantage of EBL is in its ability to do rapid prototyping with a higher resolution than is currently available with optical lithography systems. This allows research to continue and gives the opportunity to foresee new problems, which might arise as devices approach the nanoscale. Once practical prototypes have been produced by EBL, they may be mass-produced by future high-resolution parallel processing techniques such as nanoscale optical lithography when they become commercially available.

Figure 2.2 shows a block diagram of a typical commercial EBL system [28]. The column is responsible for forming and controlling the electron beam. Underneath the column is a vacuum chamber containing a stage for positioning the sample to the area of interest and it allows for sample loading and unloading. A vacuum has to be maintained from the electron gun down through the column and within the sample chamber that holds the substrate to be patterned. Electrons are a form of radiation called beta particles, which are strongly attenuated by air. A vacuum system capable of maintaining a pressure of at least 10E-5 Torr is required. A set of control electronics supplies power to the beam forming lenses and the electron beam scanning and positioning deflectors. The computer system handles such diverse functions as setting up an exposure sequence, loading and unloading the sample, aligning and focusing the electron beam and sending pattern data to the pattern generator.

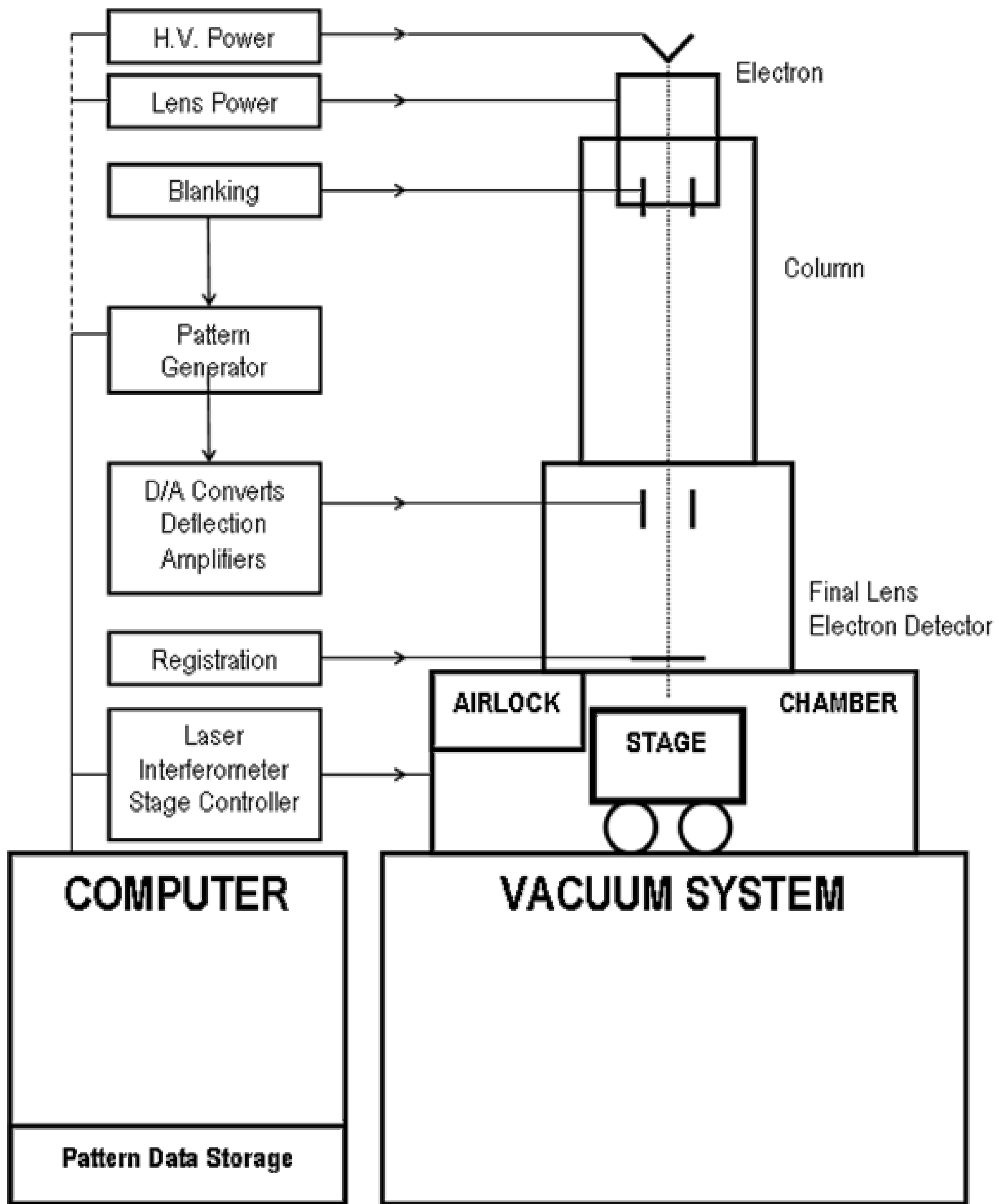

Figure 2.2 Block diagram of a typical commercial EBL system [28].

Figure 2.3 shows a picture of a typical commercial EBL system including the column, chamber and control electronics. It is designed for various applications in the research field, including GaAs FETs, optical elements, X-ray masks, Si devices and quantum effect devices that require ultra fine pattern exposure.

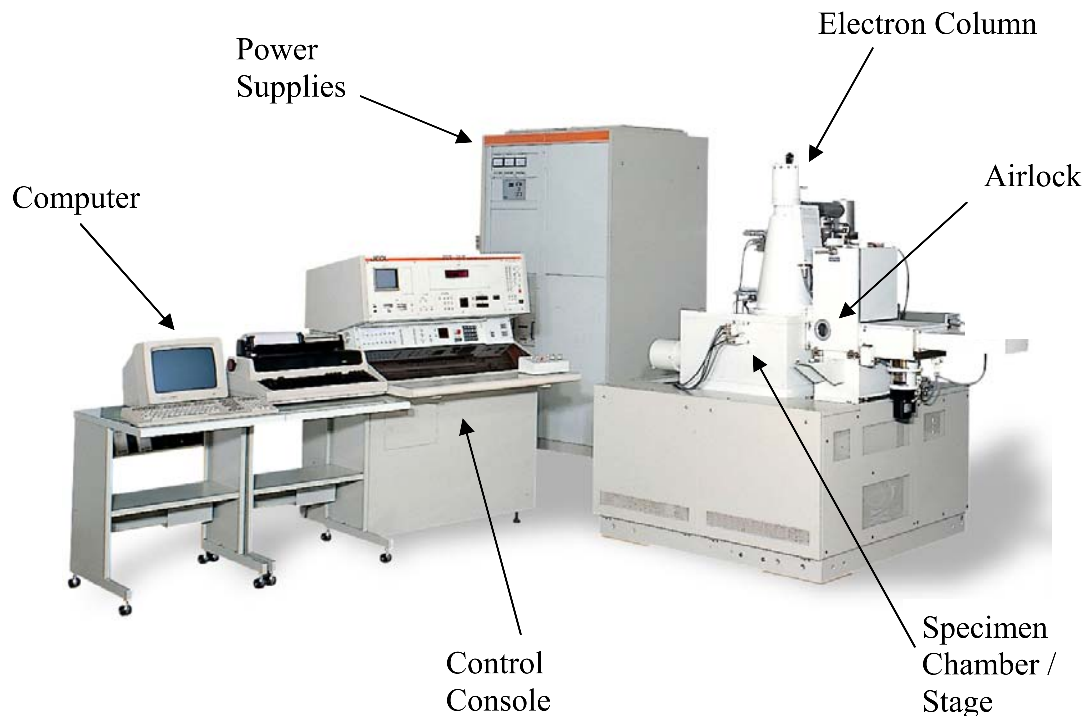

Figure 2.3 A commercial electron beam writer, the JOEL model JBX-5000LS/E (Photo courtesy of JEOL)

Figure 2.4 shows a striking example of the small resolution that can be achieved with EBL [32]. Long ~ 5nm wide openings were made in positive PMMA by EBL. Then a granular Au film was thermally evaporated such that only one Au island formed across the width of each line and liftoff produced the results seen in the image. This work was done on a 200 kV Transmission Electron Microscope (TEM)/SEM which is not commonly available in most laboratories.

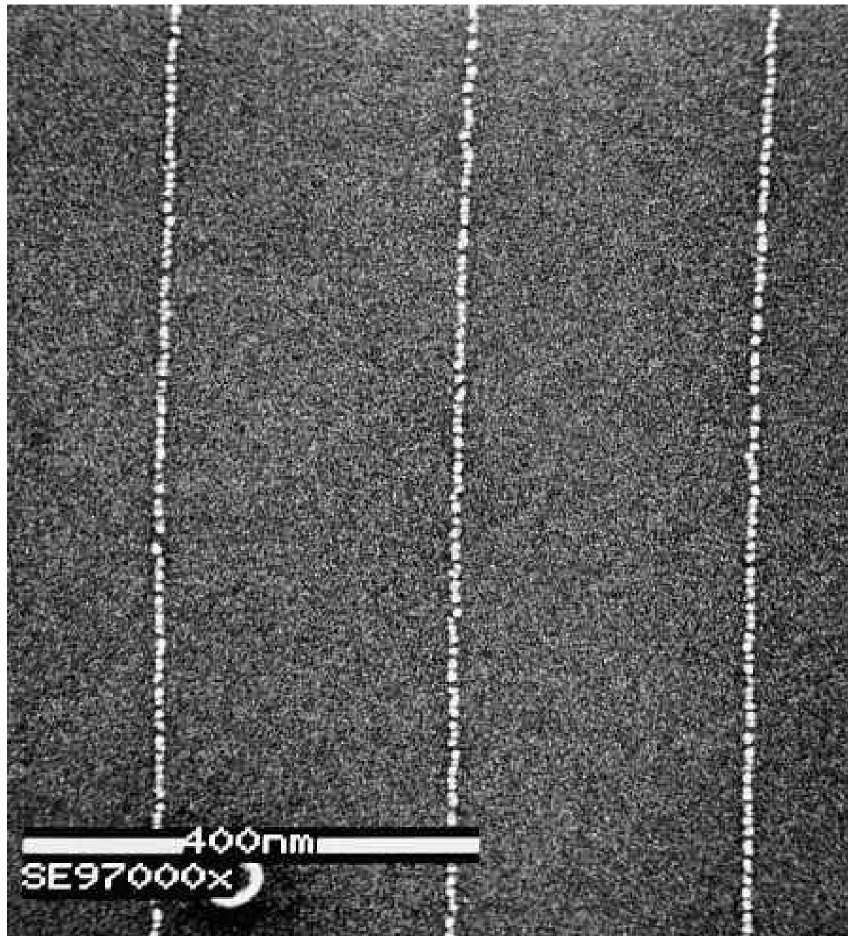

Figure 2.4 SEM micrograph of 5nm lines formed by EBL on PMMA [32].

An instrument such as this, operated at high accelerating voltage, is necessary to achieve this low resolution. Although this is a very specialized system, it does demonstrate the practical resolution EBL is capable of. On a more commonly available modern thermal field emission lithography system, such as the one shown in Fig. 2.3, the resolution is approximately 30nm.

2.3.1 Converting an SEM into an Electron Beam Lithography System

The EBL work in this research was performed on a Japan Electro Optical Ltd. model JSM 840 Scanning Electron Microscope that was converted into an EBL system. Figure 2.5 shows a photograph of the system. The conversion was done using a commercial package called the nanometer pattern generation system (NPGS). The NPGS system is available from JC Nabity Lithography systems in Bozeman Montana.

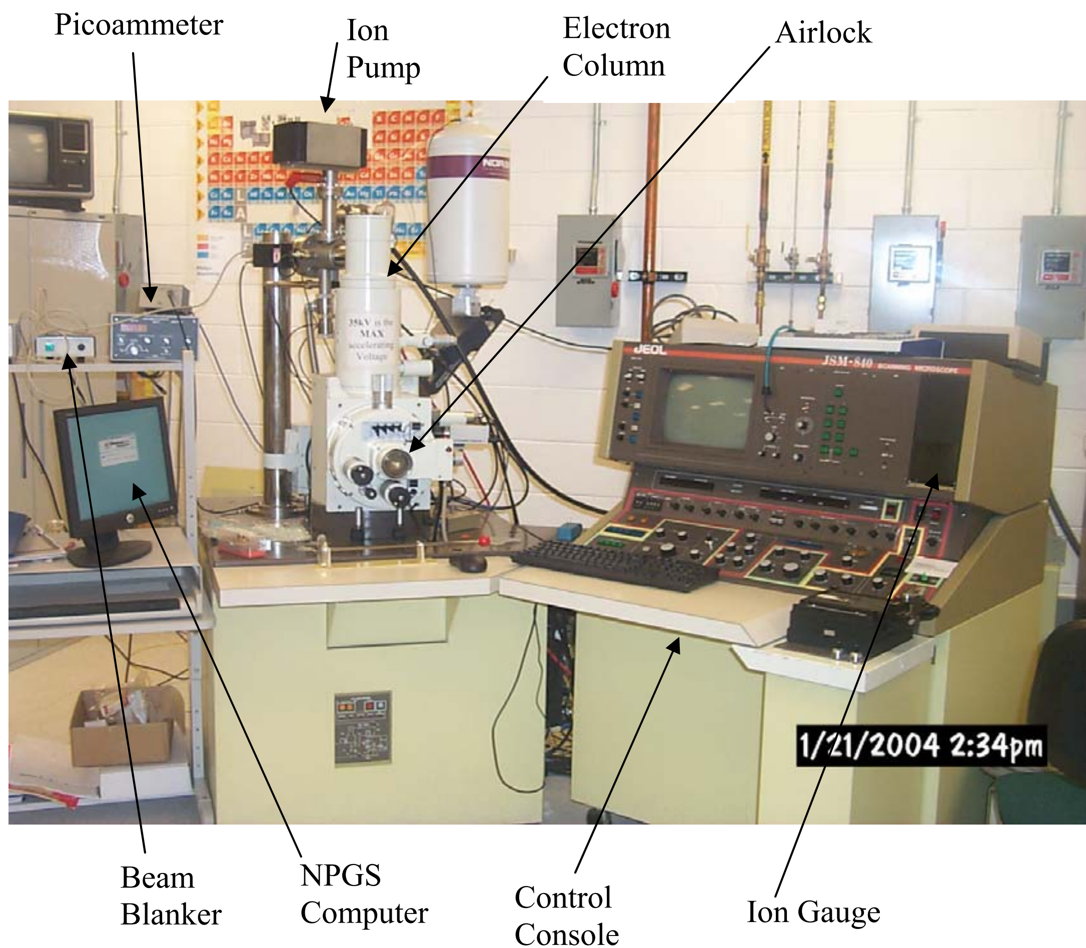

Figure 2.5 Photograph of the JSM-840 after EBL conversion. The beam blanker, ion gauge, ion pump and NPGS computer were added to the SEM for conversion to an EBL system.

The beam blanker, ion gauge, ion pump and NPGS computer system were added during the conversion of the SEM into an EBL system. The package consists of a desktop computer, with a scanning control board mounted in an available PCI expansion slot on the computer motherboard. The user interfaces to the SEM through the scan control board via a computer program called NPGS.

The original JSM 840 came with an electromagnetic beam blanker. This was replaced with an electrostatic beam blanker manufactured by Scan Service Corporation of Tustin California. This was done to reduce the noise inherent in a magnetic blanker and to increase the blanking speed. An ion pump was added to the electron gun chamber to improve the vacuum. This helps to increase the life of the electron gun filament and reduces contamination, which can lead to arcing when the acceleration voltage is applied. A cold cathode ion gauge was also added to the gun chamber to allow the vacuum to be monitored. A record of the vacuum level helps to ensure the vacuum system is functioning properly. This is important to get reproducible EBL results, since the electron beam characteristics can change with fluxuations in vacuum level.

To understand the complications one can encounter while attempting to write nanoscale patterns a good understanding of the SEM is required. Thus, the next sections will discuss the scanning electron microscope and electron optics.

2.4 The Scanning Electron Microscope

The SEM, as its name implies, uses a beam of electrons, typically focused to below 5nm diameter, to scan the topography of a surface and produce a magnified image. The electrons in the beam are accelerated by an electrostatic potential with an energy

range typically from ~ 0.5 to 200 kV. This gives the electrons the velocity they need to be directed to an area of interest where they cause emission of secondary electrons (SE) from the surface. Secondary electrons have energy in the range of 5 to 50 electron volts (eV) and can only escape from the first 10-20 atomic layers of the surface, depending on the material being studied. A secondary electron detector, or SED placed in the specimen chamber collects these electrons. The intensity of the electrons is measured by the SED and displayed on a Cathode Ray Tube (CRT). Topography is produced in an SEM image by raised areas such as small ridges or the edges of small pores that are present on the sample surface. These edges have a larger surface area and allow more secondary electrons to be emitted. Recessed areas, such as a hole, attenuate or absorb secondary electron emission, reducing the signal output from the SED. The topography thus modulates the SED output, which is then sent directly to the CRT.

As the electron beam in the CRT display is scanned over its surface, the SED modulates the intensity of the electron beam in the CRT, causing areas of attenuated SE output to appear dark. The SEM electron beam is then scanned over the surface to be imaged in synchronization with the CRT beam as it scans the surface of the display. Every line and pixel scanned in the CRT has a one to one mapping to a spot on the surface being imaged. Any areas of high SE emission appear as bright areas on the CRT. Magnification is simply a matter of reducing the scanning area so it maps the area to be imaged to a large CRT screen. Assuming a CRT dimension of 10x10 cm, a 100,000x magnification would require a scan area of 0.1 meter/10E5, or 1x1 μm. A typical CRT has 525 scan lines. To scan this many lines on the sample surface requires a beam small enough to accommodate 525 diameters within a 1x1 micron scan area.

2.4.1 Electron Sources

Generation of such a small beam size starts with choosing a suitable electron source. The size of the source is important since the length of the electron column determines the final spot size. Table 2.2 lists some of the most commonly available electron sources [28]. The standard thermionic electron source uses joule heating of a V shaped tungsten wire 5-100 um in radius heated to ~2500 to 3000 K. Lanthanum hexaboride (LaB6) has been used for many years and has now become an industry standard, due to its long life and high brightness. It is typically a rod of sintered powder about 1mm in diameter with a tip machined to a few microns in radius. It has a very low work function and high brightness is obtained by operating it at a temperature of ~ 1900K. However it requires a vacuum of 10^{-8} Torr, which is usually achieved by the addition of an ion pump to the SEM system.

Table 2.2 Commonly used electron sources [28].

Source type	Temp. (K)	Brightness (A/cm^2/sr)	Source size	Energy spread (eV)	Vacuum requirement (Torr)	Work function
Tungsten thermionic	2700	~10^5	25 um	2-3	10^{-6}	4.5
LaB_6	1900	~10^6	10 um	2-3	10^{-8}	2.4
Thermal (Schottky) ZrO field emitter	1800	~10^8	20 nm	0.9	10^{-9}	2.7
Tungsten field emitter	273	~10^9	5 nm	0.22	10^{-10}	4.5

The emission current density, J_c, delivered by thermionic sources depends on the temperature, T and is expressed by the Richardson law.

$$J_c = A_c T^2 \exp(-E_w/kT) \text{ A/cm}^2 \qquad (2.1)$$

Where A_c is a constant of the material (referred to as the Richardson constant) and E_w is the work function. Higher temperatures deliver greater beam current, but the tradeoff is an exponentially decreasing lifetime due to thermal evaporation of the cathode material.

Field emission sources typically consist of a tungsten rod sharpened to a point, typically 5-100 nm in radius. The sharp tip helps provide the very high electric fields needed to pull electrons out of the metal. Single crystal tungsten is used because it is a mechanically strong material. In order to get the desired brightness in electron current the electron extraction potential is held as high as possible. In fact, the fields are held so high that the tungsten tip is at the threshold of self destruction due to mechanical stress induced by the electric field [33].

The emission current density, Jc, delivered by Field emission, depends on the electric field, E and follows the Fowler-Nordheim equation [34].

$$J_c = BE^2 \exp\left(- 6.8 \times 10^7 \varphi^{3/2} / E\right) \qquad (2.2)$$

Where B is a field-independent constant of dimensions (A/V^2) and E is the applied field (V/cm).

Although cold field emission sources have become the sources of choice in electron microscopes, they have seen little use in EBL due to their instability in output, which is more of a problem for lithography than microscopy. The instability is caused by atoms that adsorb onto the surface of the tip [35]. This changes the work function, which results in large changes in the emission current. To minimize the current fluctuations, the electron source must be operated with ion pumps in an extreme ultra high vacuum (UHV) environment, 10^{-10} Torr, or better, which comes with a significant increase in cost.

The latest development in electron sources is the thermal field emission source. It is available in many commercial EBL systems and electron microscopes. This source combines the tungsten tip of the field emission source and the heating of the thermal source. The tip is operated at a temperature of ~ 1000 to 1800 K, which makes it less sensitive to gas adsorption. Although "thermal field emitter" is its common name, it is more properly called a "Schottky emitter" since the electrons escape over the work function barrier by both thermal excitation and field emission. Its brightness is almost as high as a cold field emission source, with a slightly larger tip size of 20 nm and an intermediate energy spread. The tungsten is usually coated with zirconium oxide to reduce the work function. It requires a vacuum in the range of 10^{-9} Torr, which means a more expensive pump than is required for a thermal emitter.

Figure 2.6 shows a cross section of a typical thermionic electron gun assembly which houses the source filament [36]. A negative bias voltage applied to the Wehnelt cylinder causes the electrons to come to a focus just beyond a circular aperture located at its center.

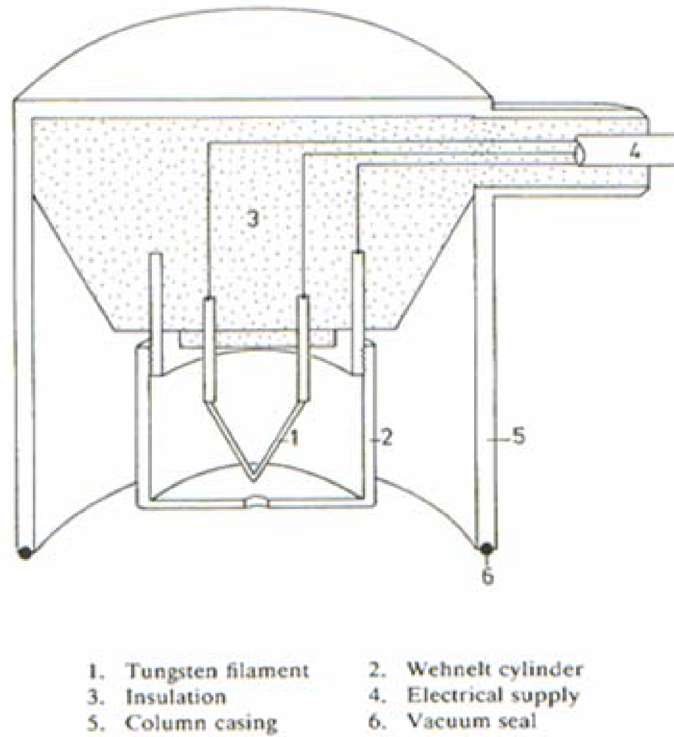

Figure 2.6 Cross section of JSM 840 thermionic electron gun [36].

Once the beam leaves the Wehnelt of the electron gun they are accelerated by voltage applied to the anode. After leaving the anode the beam then passes through alignment coils, which are used to reduce any astigmatism in the beam, as shown in Figure 2.7. A large amount of astigmatism causes the beam to be elliptical rather than cylindrical and the net result is a poorly focused beam. The astigmatism is reduced by adjusting the X and Y stigmators on the JSM 840 control console.

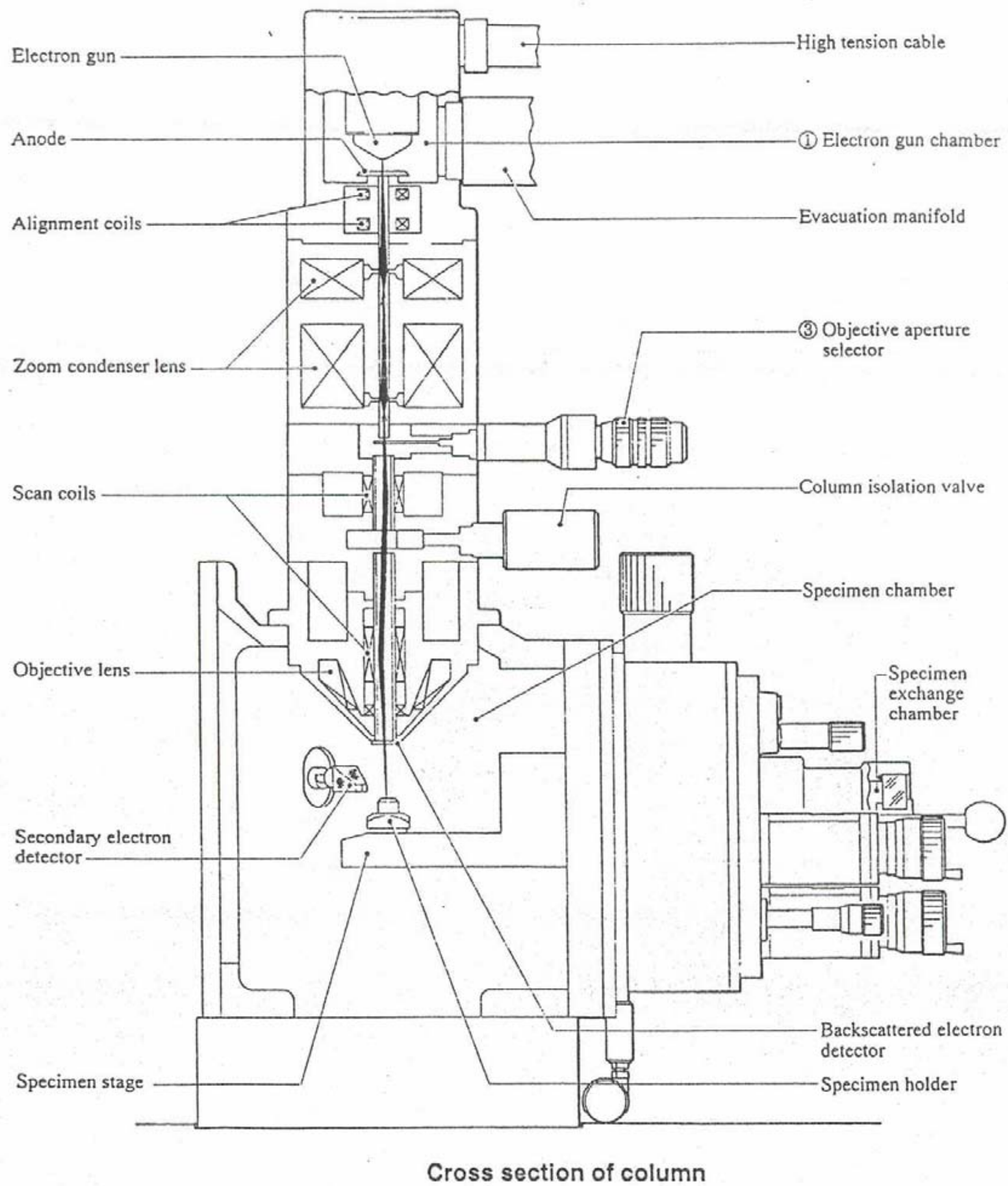

Figure 2.7 Cross section of JSM 840 electron optics and specimen chamber [36].

The beam then passes through a two stage magnetic condenser lens system which demagnifies the beam and determines the final beam current. The beam then impinges upon the objective aperture, which only allows the center of the demagnified beam to pass through. As the user turns up the current in the condenser lens the beam is defocused and expands. This in turn reduces the beam current to the target because a smaller fraction of the total beam current is allowed through the objective aperture. The beam then goes through the coils, which scan the beam and through the objective lens, which focuses the beam on the target.

The four user determined parameters, which are most important for high resolution Lithography and SEM imaging are as follows;

1) High acceleration voltages yield the smallest beam size,
2) High condenser lens setting decreases the beam current and thus decreases the beam size as discussed above,
3) Smaller objective lens aperture diameter also decreases beam size and,
4) Smallest possible target to objective lens working distance (WD).

High acceleration voltages make the beam more monochromatic in energy and this reduces chromatic aberration allowing for a more focused beam. Choosing a small working distance by adjusting the height or z-axis of the specimen stage, reduces the distance the electron beam must travel before reaching the target. This is important to reduce the interaction of the beam with any stray electric or magnetic fields, which may be present near the SEM.

2.5 Summary

The limitations and benefits of both optical lithography and EBL have been presented. Both systems are high cost and expensive to maintain. The main disadvantage for EBL is that it is a serial processing technique. However, the main advantage of EBL techniques is its ability to rapidly prototype devices at resolutions currently unattainable by optical lithography. Commercial systems have been used to fabricate metal line widths as small as 5nm, which is well into the nanoscale and far below that which can be expected to be developed by optical lithography, using currently available technology.

As part of this work, a JOEL model JSM-840 SEM was retrofitted with a nanometer pattern generation system (NPGS) procured from J.C. Nabity lithography systems [37]. An electrostatic beam blanker, ion pump and ion gauge were added to improve the performance of the system. A review of SEM operation and electron sources was also presented. The details of how this system can be used to make nanoscale patterns in semiconductor materials will be presented in Chapter 3.

Chapter 3

Synthesis of Nanoscale Structures by Electron Beam Lithography

3.1 Introduction

In this chapter a general overview of the techniques and methods used in Electron Beam Lithography (EBL) will be presented. Very subtle changes in the environment surrounding a lithography system can lead to problems, which may affect the quality of the patterns produced. Some of the general precautions that should be observed for successful lithography are detailed below. Following this, the general procedures used for the EBL work on silicon and silicon carbide will be presented.

The first step in producing nanoscale structures is to make sure all sources of electromagnetic interference and mechanical vibrations in the proximity of the lithography system are reduced to a minimum. A handheld digital gauss meter was purchased to ensure the fields surrounding the electron column were at or below 0.5 milligauss (mG) as specified in the JEOL JSM-840 manual. Noise from an old model CRT screen about 3-4 feet from the column measured about 3 mG prevented the first attempts at high-resolution work. After removing this, the field measured approximately 0.08 mG next to the column. Even if the user simply rotates around in a swivel chair used in the lithography laboratory produced significant shifts in the SEM image at magnifications greater than 100,000X. This was due to the magnetism in the iron frame

of the chair. These chairs were replaced with chairs constructed with plastic and aluminum and the problem was solved.

Since no method was available to measure mechanical vibration, pre-emptive measures were taken to reduce possible sources of vibration, including replacement of the rubber bushing connecting the turbo pump to the specimen chamber and placing the rubber feet under the column frame. The JSM-840 column has an integrated air shock system, which requires compressed air and was deemed to be in good working order. The operator must also check the instrument to be sure there is nothing touching the column, or bridging the small gap between the column and control console which will conduct vibration.

Transmitted sources of sound were also a concern. An electron microscope is a very sensitive microphone. It has been observed that casual talking near the EBL system can deflect the beam approximately +/- 10nm. In order to reduce the possibility of interference from talking or vibration when the room door is opened and closed, quiet signs were placed around the microscope and on the access door to the room to indicate lithography in progress. Most of the successful lithography patterns were produced after hours when the traffic around the lithography facility was at a minimum.

3.2 Sample Preparation

The samples used for initial trials of the lithography system were taken from polished 2-inch single crystal silicon wafers. These were chosen for initial studies because of the high cost of silicon carbide wafers. Approximately 10 runs were done on silicon before the process was optimized enough to produce successful patterns with a

feature size of ~20 nm in the PMMA resist. To produce substrates for lithography the wafers were first cleaned by ultrasonic bath in acetone and then in 2-propanol. The SiC substrates used in the final lithography work were received as 1cm squares and were also prepared in the same manner as the silicon samples.

3.2.1 Resist Spinning

The silicon wafers and SiC die were coated with PMMA resist, using a resist spinner. The resist manufacturer recommended the use of a standard 950,000 molecular weight resist because it has been shown to perform well in high resolution EBL work [38]. The resist used was a 950 MW resist with a 3% Anisole solvent obtained from MicroChem Inc.{39}. Generally the higher the molecular weight resists result in higher contrast, which result in sharper edges. Figure 3.1 shows a spin curve for 950MW resist.

For this work a spin speed of 4000 RPM was chosen which resulted in a resist thickness of approximately 195 nm. The highest spin speed was chosen from this chart to produce the thinnest resist possible. When the electron beam strikes the surface of the resist, the electrons immediately begin scattering laterally. The thin resist thickness reduces this effect and allows higher resolution lithography. The wafers were then baked in a convection oven at 170°C for 1 hour and cleaved into 1cm square die. The resist thickness was measured using a stylus profilometer, by scanning over an area where the resist was removed.

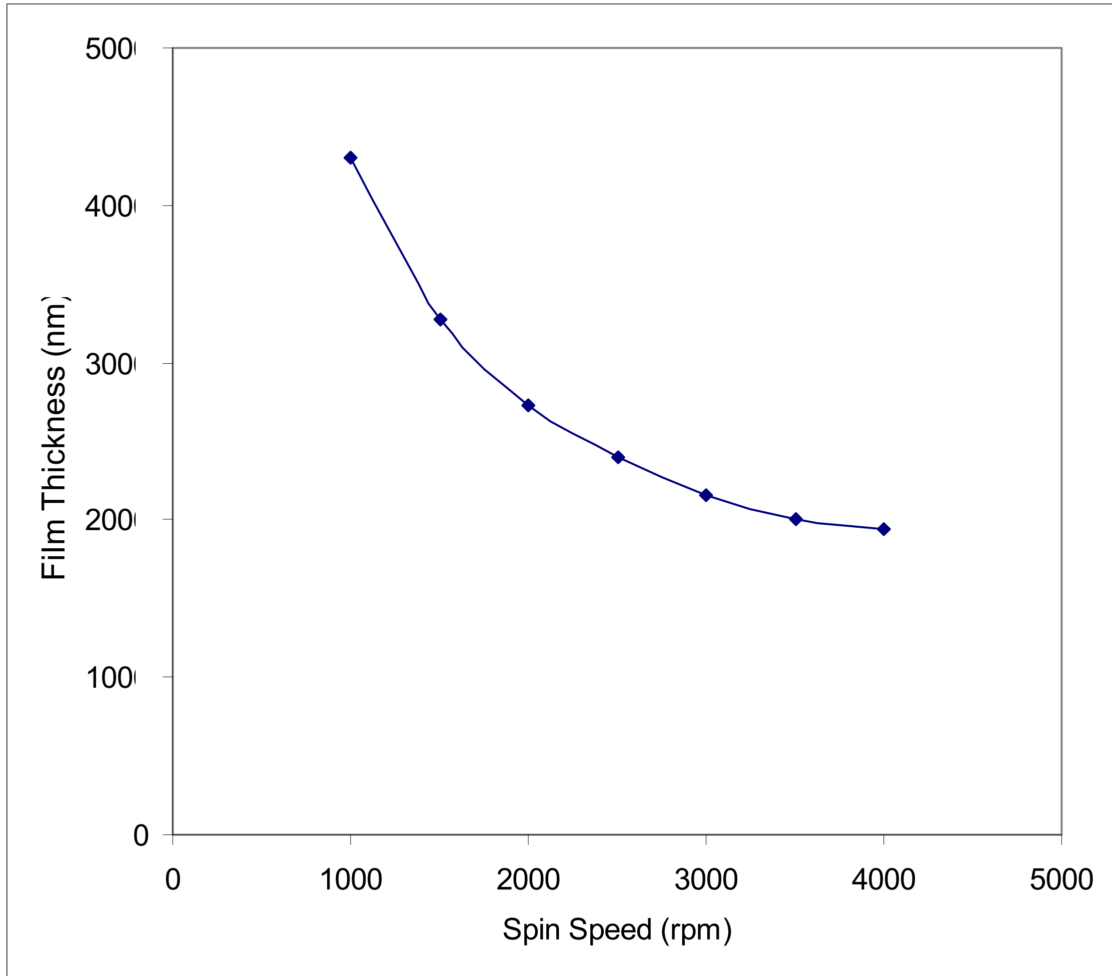

Figure 3.1 Plot of film thicknesses vs. spinning speed for 950 MW PMMA resist [38]

3.3 Sample Holder

After the resist has been cured, the coated dies are then scribed with a single stroke of a diamond scribe, with a scratch 2-3 mm long. The scratch is used as a marker to make it easier to locate patterns on the die after EBL processing. The scratch is oriented as shown in Figure 3.2. The die is then fastened with copper clips to an aluminum SEM sample holder that was made specifically for EBL work. A Faraday cup was made by drilling a small 2 mm hole into the aluminum. A 3 mm TEM grid with a

50-micron hole was then centered over the hole and glued in place with carbon paint. The Faraday cup is used to make accurate measurements of the electron beam current. A small piece of a carbon, stub sputter coated with gold, was fixed in place using silver paint. The small sputtered gold particles are useful for focusing and adjusting the beam without exposing the resist. This gold surface then serves as a gold standard during EBL processing.

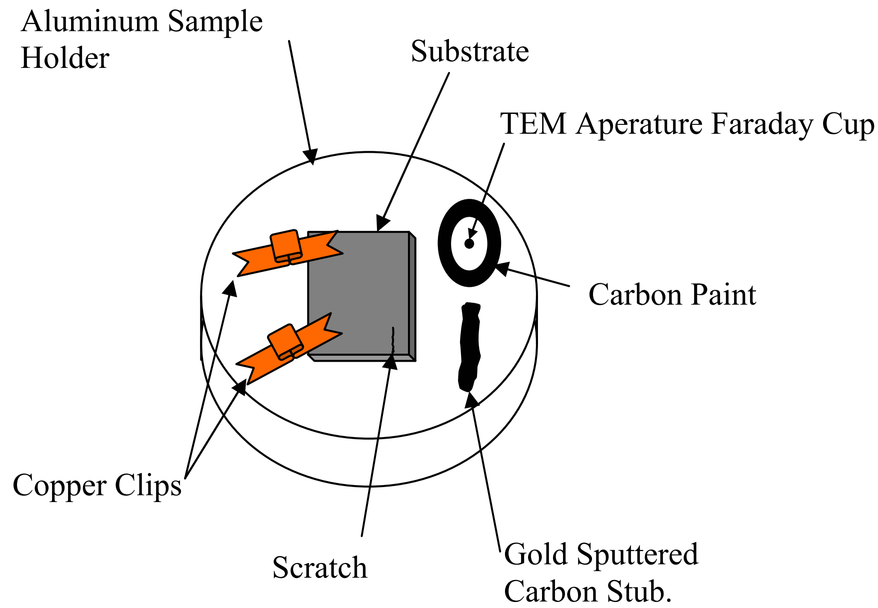

Figure 3.2 Aluminum sample holder developed for the EBL described in this work.

3.4 Electron Dose Array

After the die has been prepared and loaded into the SEM, it is ready for patterning. The beam is first carefully aligned and focused using the gold standard on the sample holder. A beam current measurement is then made using the Faraday cup. This reading is input into the nanometer pattern generation system (NPGS) scan control software which then adjusts the scanning speed to deliver a specified electron dose [37].

The NPGS software drives the pattern generator card. Patterns may be input into the NPGS software from any common CAD package, which supports DWG, DXF, GDSII, CIF and IGES file formats.

The patterns for this work were created using DesignCAD, which is a commercial computer-aided-design program that is integrated into the NPGS software [40]. Pattern designs can consist of lines of arbitrary slope, as well as circles, circular arcs and arbitrary filled polygons. Text, Bezier curves, cubic spline curves and elliptical arcs can also be generated and written as a series of short lines. Pattern elements that are to have different exposure parameters such as dose, exposure point spacing, microscope beam current, microscope magnification etc., are designed in different drawing layers or with different line colors. This gives an almost unlimited number of exposure conditions within a single pattern.

Good EBL practice requires running a test pattern with the same beam conditions on the die just before, or just after, a device pattern has been written. The test pattern typically consists of an array of circular patterns with radial spokes as shown Figure 3.3 In this work an array of nine wheels were drawn using DesignCad, with each wheel programmed to receive a specified dose. The doses were incremented on each wheel with lowest dose on the upper left wheel and the largest on the lower right. The dose is identified in the DesignCad drawing by using a different color for each wheel. The wheels in Figure 3.3 are all black and shown here just for illustration. The drawing is then imported into the NPGS software, which recognizes each color is to receive a different dose. The dose for each color is specified by the user in the NPGS software.

The black dots to the lower right of each wheel are a dump point to place the beam after writing each wheel. The Wheel array is a useful means of determining the dose that produces the best pattern. It is also useful for diagnosis of exposure problems such as beam stigmation, defocused beam, tilted stage, line frequency noise, etc. A series of wheel pictures which demonstrate most of the common problems is available on the J. C. Nabity website [41]. It is necessary to place the dump point several microns away from the patterns to prevent electrons from scattering up from the substrate and therefore over exposing the pattern. The wheel diameter designed for this pattern was 10 microns and the border outline was 95 x 95 micron. Thus, the entire width of this matrix is less than the diameter of a human hair and is too small to be seen with the naked eye.

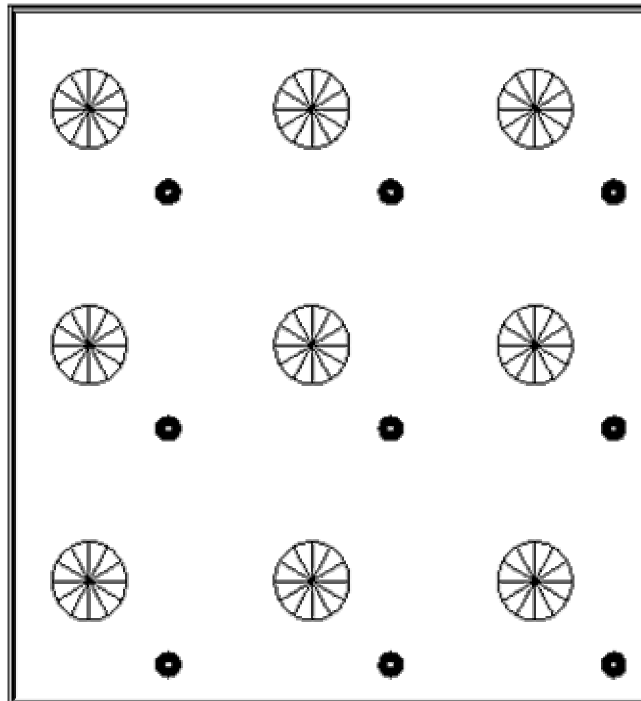

Figure 3.3 Wheel array test pattern for beam diagnostics, created using DesignCad [40].

3.5 Resist Processing

After exposing the resist with this wheel array the die is removed from the SEM and processed to develop the resist. The developer solution consists of 1 part methyl isobutyl ketone (MIBK), to 3 parts 2-propanol. The exposed die is rinsed for 70 seconds in the developer and then rinsed in 2-propanol for 20 seconds, followed by a 20 second rinse in de-ionized (DI) water. After development the exposed lines delineating the patterns are dissolved away. The next step is to inspect the patterns first with optical microscopy and then with the SEM. Even though the pattern lines are usually much too small to be resolved by optical lithography, one can still see if the patterns are there or not. This also gives an initial assessment of the quality of the patterns and can save many hours of SEM time searching for patterns that do not exist. After observation in the optical microscope, the dies are then viewed in the SEM for pattern characterization and metrology. It is necessary to sputter a thin gold film on the pattern to prevent charging before SEM observation.

3.6 Reactive Ion Etching

The next step in the process is to deposit a thin layer of metal through the resist pattern to form a metal mask, which is then used to transfer the pattern onto the substrate. The areas of metal covering the remaining resist are removed by dissolving the resist in acetone by the liftoff process.

In this work Reactive Ion Etching, or RIE, was used to etch the patterns into the silicon carbide substrates. Nickel was chosen as the mask material due to its resistance to etching in the RIE process [42]. The thickness of the nickel can vary depending on the

process used to transfer the pattern onto the substrate. For the best liftoff results, the nickel should be thinner than the resist. The fidelity of the pattern after liftoff degrades as the nickel becomes much thicker than the resist.

RIE experiments were carried out on 3C-SiC epitaxial films grown in house on silicon substrates [43] using a Plasma Therm PT700 RIE system. A mask designed for broad area laser diodes was patterned onto the 3C film using optical lithography [44]. An Electron beam evaporator was then used to deposit 1000 angstroms of nickel to form the mask which was used for RIE etch rate experiments. Figure 3.4 shows a low magnification FE-SEM image of the nickel pattern after liftoff processing.

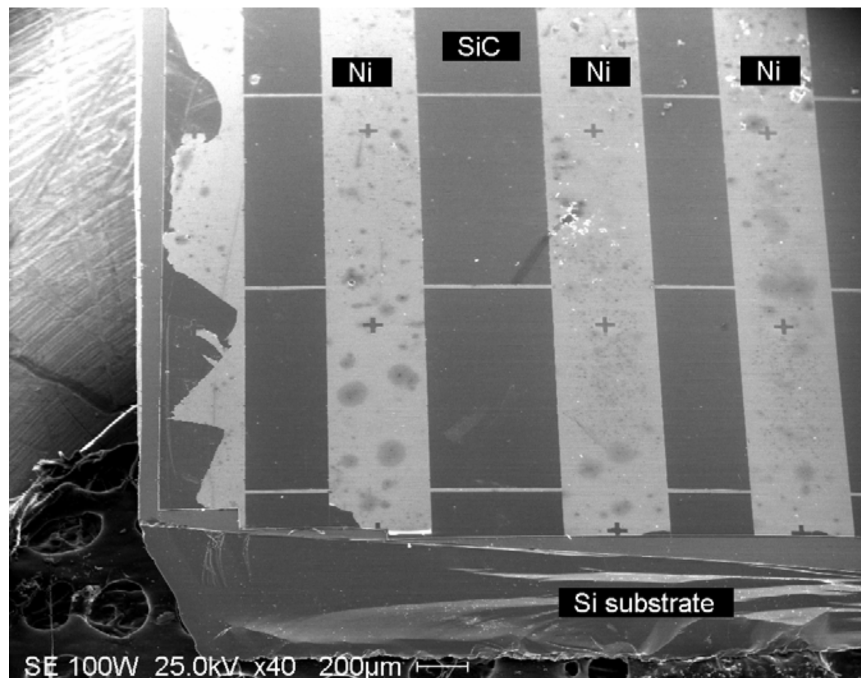

Figure 3.4 FE-SEM image of nickel RIE mask pattern formed on epitaxial 3C-SiC grown on a (001) Si substrate.

The etch rate experiments were conducted at a power of 100, 200, 300 and 400 watts for 5 minutes each. The etch runs were done at a pressure of 300 mTorr, with gas

flows of 40 sccm SF_6, 20 sccm O_2 and 10 sccm H_2. Figure 3.5 shows a plot of the etch depth vs. power. The curve shown in this plot was produced using a polynomial fit through the four data points. The etch depths were measured in cross section using FE-SEM.

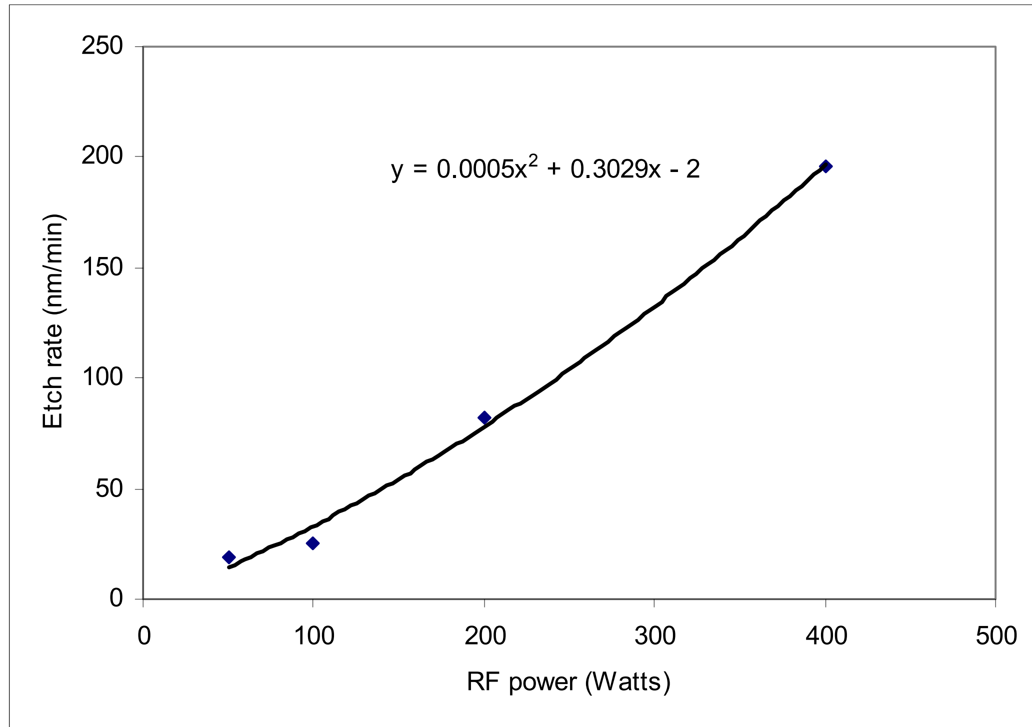

Figure 3.5 Plot of RF power vs. etch depth for 3C-SiC using RIE and a nickel mask.

Figures 3.6 and 3.7 show cross sectional views of the 100 and 400 watt etch profiles for reference. When SiC is etched on an aluminum platen using oxygen and a fluorinated gas, columnar residues form due to microscopic masking, also known as micromasking [45]. The micromasks are formed from small amounts of aluminum, which are removed from the bottom electrode and deposited on the SiC surface.

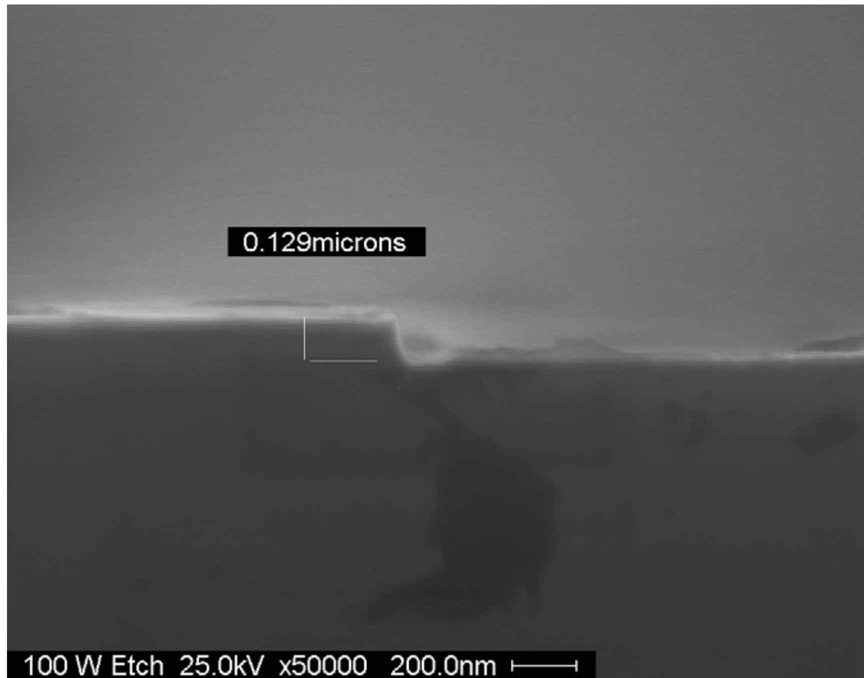

Figure 3.6 Cross-section FE-SEM image of the 100 watt etch profile. The etched mesa depth is ~ 130 nm.

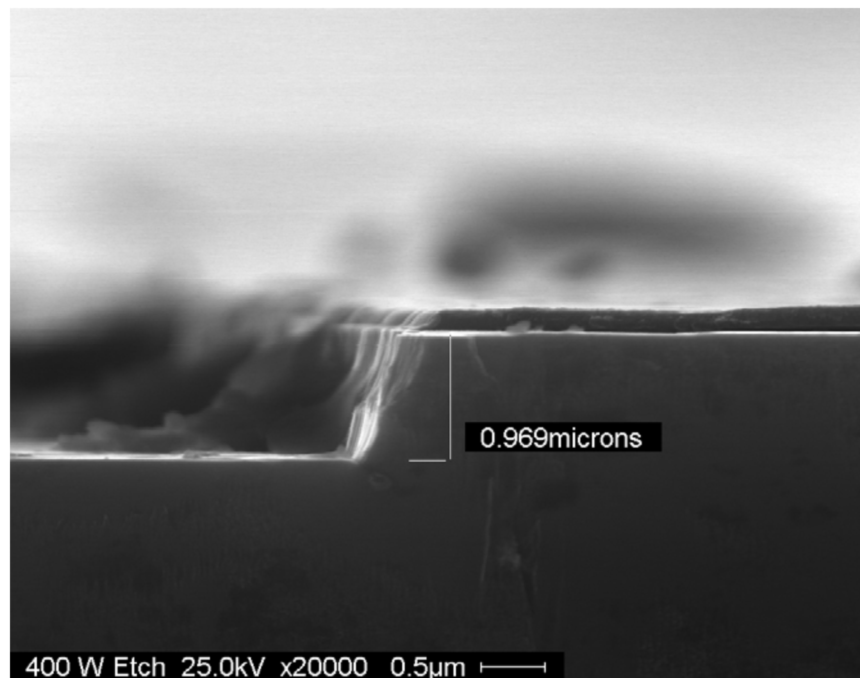

Figure 3.7 Cross-section FE-SEM image of 400 watt etch profile. The etched mesa depth is ~1000 nm, or 1 µm.

To reduce this effect, the bottom electrode on the RIE system was covered with a graphite ;plate and 10 sccm of hydrogen was added to the gas mixture. The hydrogen is added because it reacts with aluminum forming compounds, which are then pumped out of the system. Despite these precautions micromasking was still observed, although at a much reduced level. Figure 3.8 shows an SEM image in which a corner of the nickel mask has peeled away to reveal the 3C film underneath.

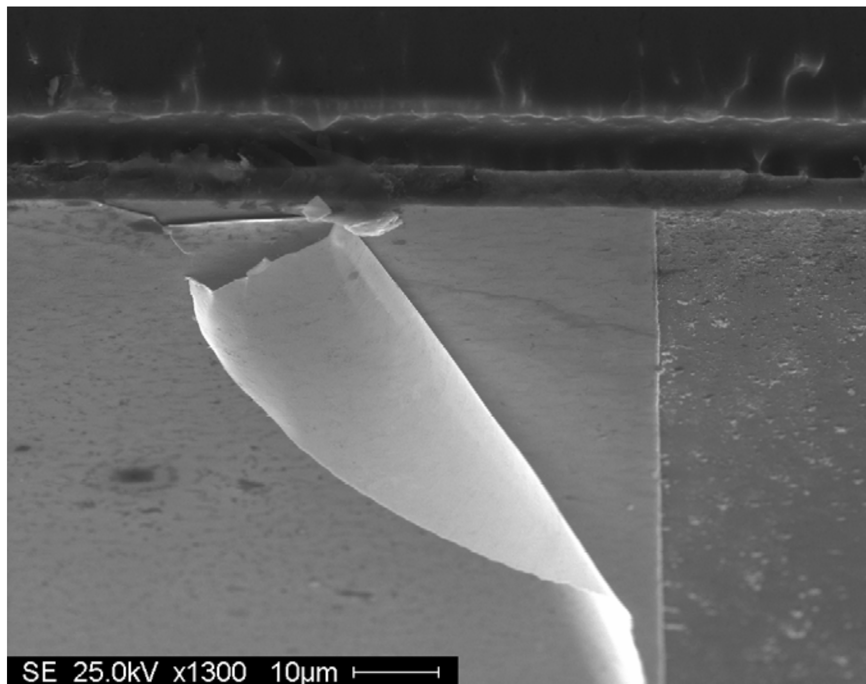

Figure 3.8 FE-SEM image after 200 watt etch. A corner of the nickel mask peeled up in this image to reveal the unetched 3C-SiC underneath.

Figure 3.9 shows a higher magnification image of this area showing the interface between the etched and non-etched regions. The micromasking can be seen here as small spikes near the edge of the die.

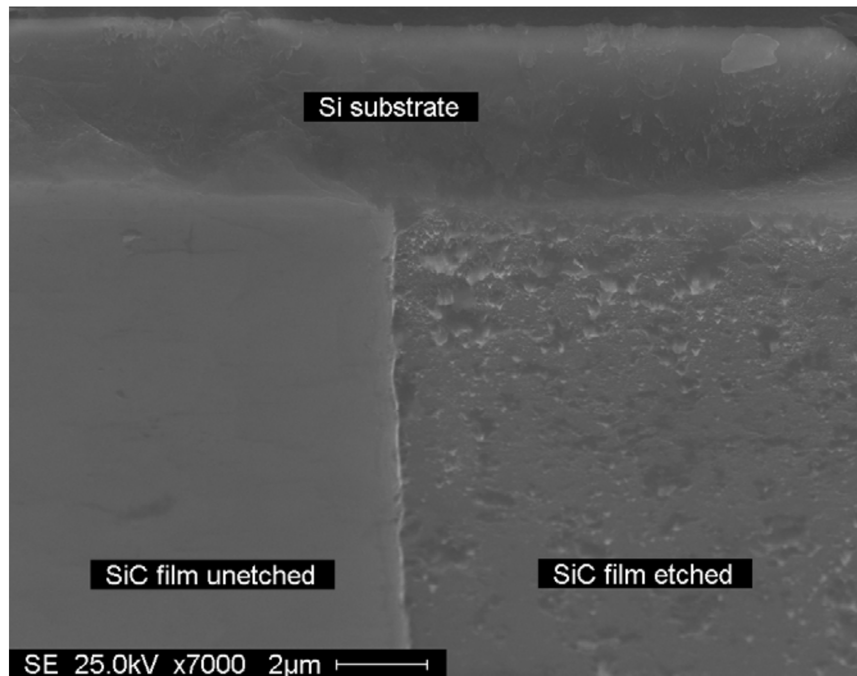

Figure 3.9 Higher magnification image of Figure 7, showing a closer view of the etched and unetched areas of the 3C-SiC. Enhanced micromasking is observed near the cleaved edge of the silicon substrate.

3.7 Summary

The first step in the synthesis of nanoscale structures by EBL is to take precautions to create an environment near the system which is free of electromagnetic interference and mechanical vibration. In a facility, which is not designed for EBL, it is recommended that the work be done during hours of low traffic to minimize coupling of noise into the electron beam.

Sample preparation for nanoscale EBL consists of cleaning and dicing of substrate material, which has been spin coated, with a thin layer of PMMA resist. The dies were first cut into 1 cm squares which can fit onto a SEM sample holder designed for EBL work. Before mounting to the sample holder, the dies were diamond scribed to allow registration of the EBL patterns after processing. Electron dose arrays using

spoked wheels were then patterned onto the resist, to determine the optimal electron dose. Following this, the resist was developed and inspected by optical and electron microscopy. The dies were coated with nickel and liftoff used to form a mask for subsequent RIE processing.

Using standard optical lithography and metal liftoff processing the etch rate for 3C-SiC was determined. This etch rate was then used to predict the etch rate on nano-patterned 4H-SiC structures, formed via EBL and discussed in Chapter 4. Once the die preparation and processing steps were in place, the next step was to optimize the EBL process to produce nanoscale patterns. This subject will be presented in more detail in the next chapter.

Chapter 4

Synthesis and Characterization of Nanoscale Structures in Silicon Carbide

4.1 Introduction

In this chapter, the synthesis of nanoscale structures in silicon carbide will be discussed. First, the procedures and lithography patterns used to optimize the electron beam profile will first be presented. This will be followed by characterization using scanning electron microscopy (SEM) of the electron beam lithography (EBL) runs performed in this work. The EBL runs were first performed on silicon to optimize the process. These processes were then performed on 4H- and 6H-SiC crystals and the pattern etched into the substrate using the reactive ion etching (RIE) process outlined in Section 3.7. For all SEM characterization a Hitachi model S-800 field emission SEM was used at a working distance of ~5mm and beam voltage of 25kV, unless otherwise specified. The EBL runs were done at a beam energy of 35keV, at a working distance of ~ 5mm and the lowest beam current setting available on the JOEL JSM-840, which measures ~ 6 pA in the faraday cup.

The initial EBL runs, which were conducted on silicon substrates, produced a dot resolution of approximately 50 nm diameter in poly(methyl-methcrylate) PMMA. In some cases PMMA nanodots less than 10 nm in diameter were produced as a result of under exposure of the resist. Figure 4.1 shows a DesignCad drawing of the dot array,

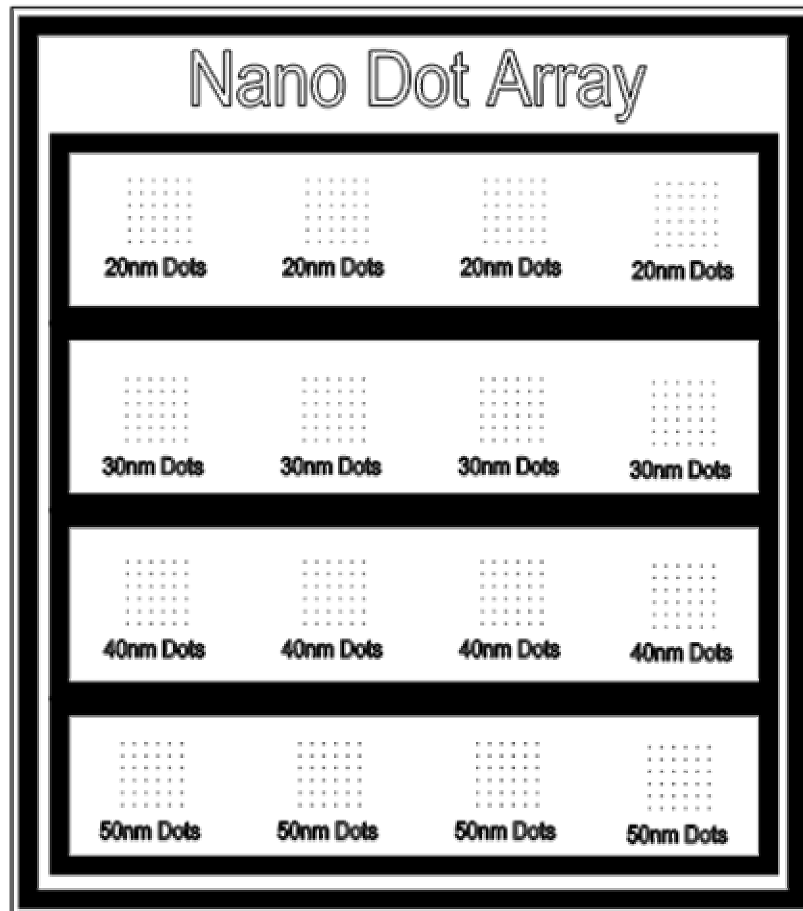

Figure 4.1 DesignCad TM drawing of nanodot test array used to measure EBL resolution in PMMA. Each of the four columns of dots receives a specified dose, which can be varied to determine the optimal dose for dot synthesis.

which was used to determine the smallest dot, or pixel, which could be produced in the PMMA resist. This drawing consists of 4 columns of dot patterns. The NPGS software was programmed to deliver a different dose to each column. The SEM was then used to characterize the dots to see which of the four columns produced the most accurate patterns, thus determining the most effective electron dose. Within each column, four 6x6 arrays were designed with dot sizes of 20, 30, 40 and 50 nm diameter. Rectangles were drawn around the entire array and labeling was added to aid identification of individual arrays during characterization.

During the course of the EBL process optimization, a technique was developed to optimize the beam. This involved turning the SEM electron beam scanning system off, thus putting the SEM in spot mode. In spot mode the beam is focused to the center of the scanning area which is ~100x100 microns at 1000X magnification. The scanning, or raster width, is found by dividing the SEM CRT dimension, in this case 0.1 meter, by the magnification. The beam is allowed to dwell in spot mode for 30 seconds, which "burns" a spot in the resist. The lowest beam current possible, ~ 5pA, was used to get the most well defined beam possible. The JSM-840 specifications indicate a resolution of 2nm for this SEM, which would indicate a beam diameter several times smaller than this. Assuming a 0.5 nm beam diameter, the area of the beam is 0.196 nm^2 which, for 5pA of beam current gives a beam current density of approximately 2500 A/cm^2. Although the total power is very low, due to the high local current density the resist undergoes a change in polymerization, which is visible under the SEM. This gives a direct means to observe the beam profile, which can then be adjusted to give a well-defined and symmetrical beam. Figure 4.2 shows a series of spots burned in the resist. After each 30-second burn the SEM beam alignment, focus and astigmatism are adjusted until there is no further improvement of the beam profile. As can be seen in the Figure 4.2, the beam starts out slightly out of focus and after adjusting the focus and astigmatism the spot on the far right was produced, which is smaller and more symmetrical.

Once the beam has been optimized an accurate measurement of the beam current is obtained using the Faraday cup located near the substrate on the sample holder. The SEM stage micrometers are then moved to the end of the scratch made in the substrate

during sample preparation and a final spot is burned at this location and photographed just prior to pattern writing. The beam is then blanked and the micrometers are moved to

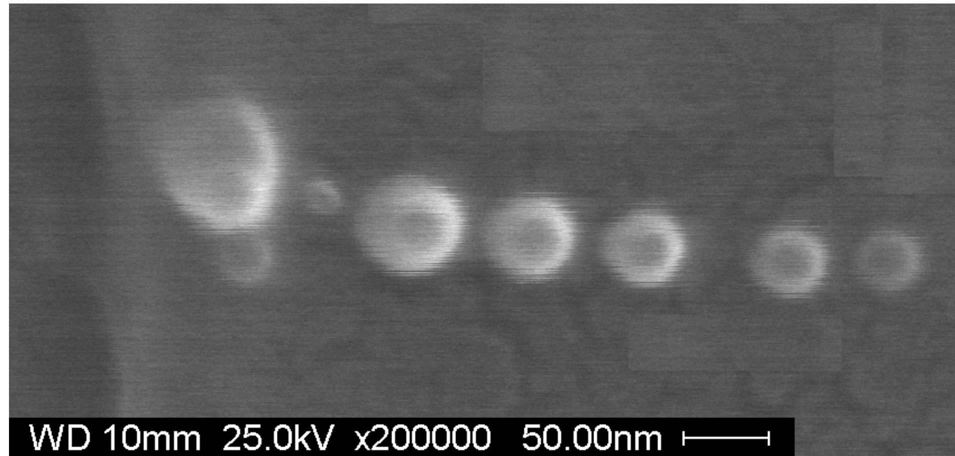

Figure 4.2 Spot burning technique in which the beam profile is improved, (from left to right), resulting in the well defined beam spot on the far right of the Figure.

an area 100 microns from the end of the scratch. The pattern design is then loaded into the NPGS software and the scanning system is switched to computer control. The proper magnification is selected and the pattern is run to expose the resist. The patterned substrate is finally removed and developed as discussed in section 3.6.

4.2 Electron Dose Array on Silicon

Figure 4.3 shows an SEM image of one of the first successful wheel patterns produced on a silicon substrate after liftoff. This pattern was used to determine the best electron dose to use for subsequent experiments. The resist thickness for this test pattern was 150 nm, which was then coated with 50 nm of nickel after patterning and resist development. As can be seen here, the most complete wheel was produced at a dose of 452 $\mu C/cm^2$.

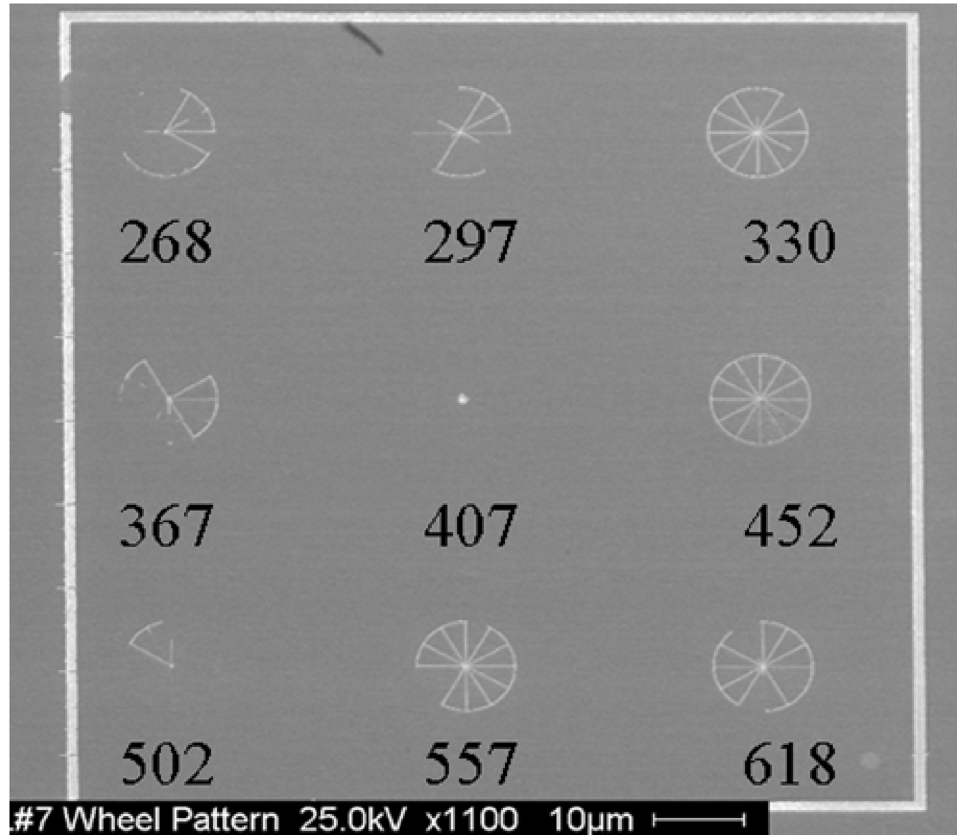

Figure 4.3 SEM micrograph of first successful liftoff of nickel wheels on a silicon substrate. As can be seen here the 452 μC/cm^2 produced the most complete wheel pattern and was therefore chosen as the most effective dose for resist exposure.

4.3 PMMA Nanodots on Silicon

Figure 4.4 shows an SEM image of the nanodot pattern of Figure 4.1 after writing the pattern in PMMA on a silicon substrate. This image was taken just after developingand after the resist was sputter coated with a 5 nm gold film to prevent charging during SEM characterization. The rectangle, which was drawn around the nanodots and the text labels for each dot array were all successfully developed. The area electron dosage from left to right was 300, 400, 500 and 600 μC/cm^2 for each column,

respectively. This span was chosen to center around the areal dose of 452 μC/cm^2 which was determined from the silicon wheel experiment above.

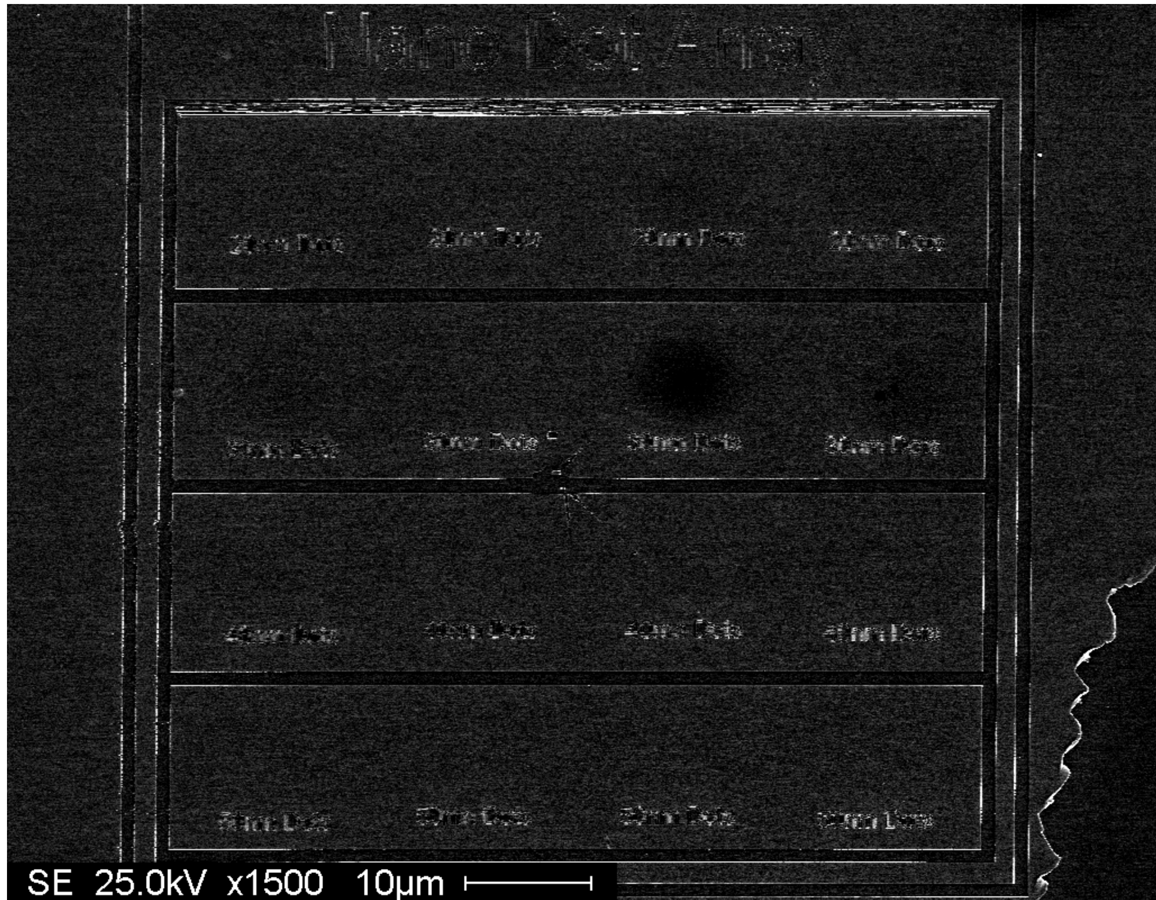

Figure 4.4 SEM micrograph of nanodot pattern created in PMMA on silicon. This image was taken just after resist development. The area electron dosage from left to right was 300, 400, 500 and 600 μC/cm^2 for each column of dots, respectively.

Figure 4.5 shows a collage of SEM images of one dot from each of the dot arrays of Figure 4.4, taken at a magnification of 200,000X. The collage is arranged in the same order as the larger dot arrays in Figure 4.1. In order for a dot array to be considered successful, all the dots from the entire 6x6 array for each size and column had to be visible. Since only a few of the 20 nm dots appeared sporadically they were not

considered reproducible and were not included for comparison in the collage. As can be observed in Figure 4.4, the 30, 40 and 50 nm dots were produced with some variability in accuracy. The best results appear to be in the third column from the left, i.e. the 500 $\mu C/cm^2$ dose.

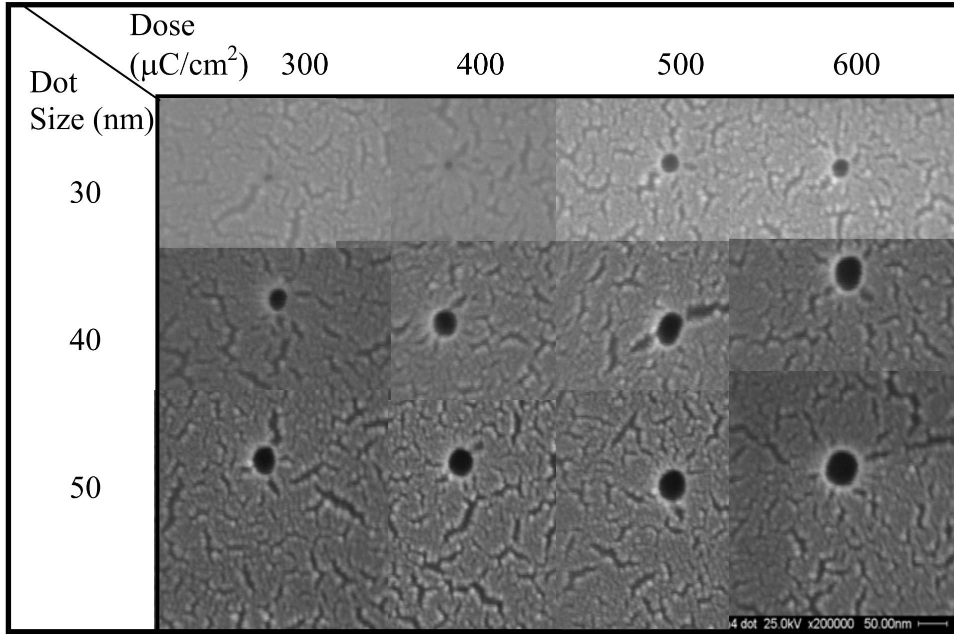

Figure 4.5 High resolution SEM collage of individual dots from the pattern in Figure 4.4, after sputter coating with 10 nm of gold. The gold sputter coat is visible at this resolution and may interfere with dot metrology.

Interestingly, the under exposed 300 and 400 $\mu C/cm^2$ dose arrays for the 30 nm dots actually produced dots which were below 10 nm in size. All these dots are difficult to measure in the SEM due to the necessity of the gold sputter coat to prevent charging. The grain size of the sputtered gold particles tends to interfere with the dot metrology. This is particularly evident with the 40 nm dot at 500 $\mu C/cm^2$, where the dot appears to have been deformed as a result of being straddled by a crack in the gold film. The sputtered gold film for this image was 15 nm thick.

4.4 Electron Dose Array on 6H-SiC

The first experiments on silicon carbide were performed on 6H-SiC and prepared as described in Section 3.2. Figures 4.6 and 4.7 show SEM micrographs of the wheel array after patterning and metal liftoff, respectively. The dosages used for each wheel were as labeled in the Figure in units of $\mu C/cm^2$. In this experiment an error was made during electron beam deposition resulting in a nickel film which was 3 times thicker than the resist. As a general rule, for successful liftoff, the nickel thickness should be the inverse of this or 1/3 the thickness of the resist. As can be seen in Figure 4.7, the nickel film did still liftoff in areas that had a proximity to the electron beam, i.e. around the edges and the wheels.

Although the electron dose in these areas was not sufficient to dissolve the resist during development, it was enough to allow it to make it more sensitive to dissolution in the acetone used for liftoff. This may suggest a method to assist liftoff in cases where a process calls for a nickel mask, which is thicker, then the resist. This would be a simple matter of including an additional step, i.e. using the SEM to image over the entire area of the pattern to deliver a dose just under that needed for resist development.

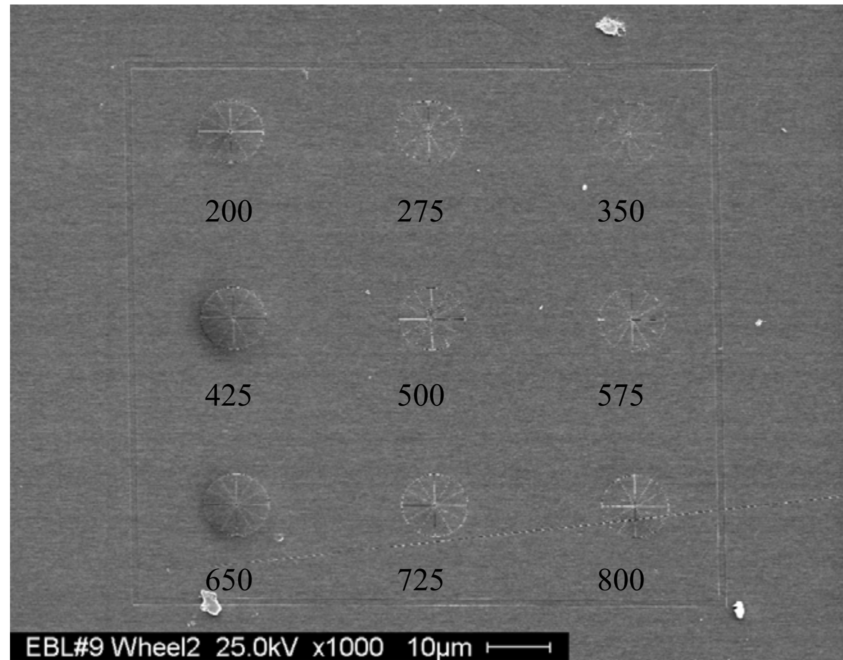

Figure 4.6 Electron dose array for determining the exposure dose on 6H-SiC. The dose for each wheel is shown in units of $\mu C/cm^2$. The SEM image was taken just after resist development.

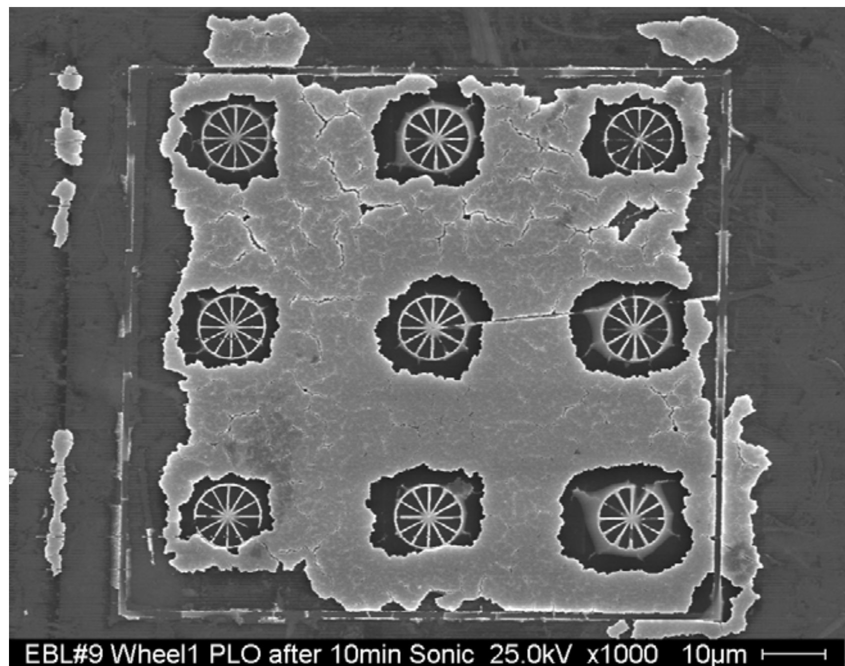

Figure 4.7 Wheel pattern from Figure 4.6, after deposition of 450 nm nickel and liftoff processing. This shows poor pattern fidelity and incomplete liftoff due to the thick nickel mask.

Figure 4.8 shows one of the wheels of Figure 4.6 at higher magnification. This demonstrates the utility of the wheel patterns in beam diagnostics. As can be seen in the Figure, the line width of 92 nm on the left side of the wheel is thinner than the119 nm line on the right edge, indicating the sample holder may have had a slight tilt during patterning which may have defocused the beam. The spokes in this wheel were also larger than expected at 66 nm, which also indicates an out of focus beam. Even at the very high exposure dose during the spot burning shown in Figure 4.2, the beam was less then 50 nm. It would be expected that the spot size in the resist during writing should have been less than this because of the decreased exposure time.

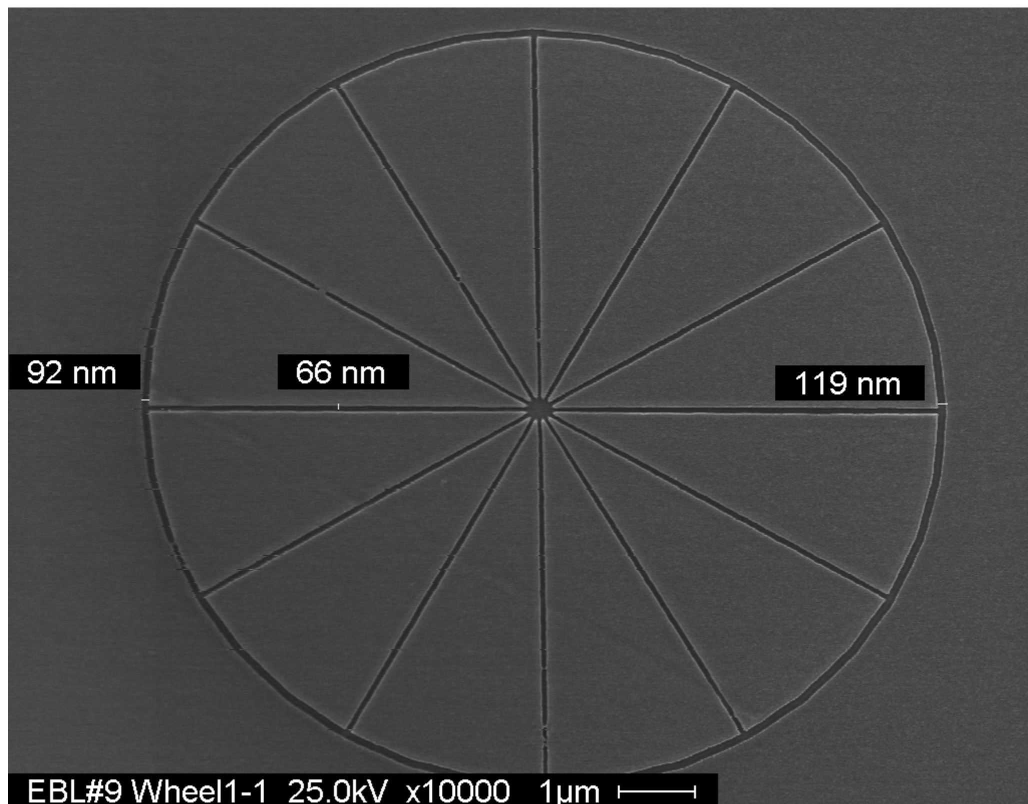

Figure 4.8 SEM micrograph of one of the wheels from the pattern in Figure 4.6, showing the effect of a slight tilt in the SEM sample stage and an out of focus beam.

4.5 Reactive Ion Etching of 6H-SiC Wheel Pattern

As a first test of the SiC RIE process the wheel pattern in Figure 4.7 was processed using RIE on 6H-SiC. This was done using the process parameters from section 3.7 at a power of 100 watts. Figure 4.9 shows a close-up of wheel #4 from this pattern exposed at a dose of 425 $\mu C/cm^2$. This image was taken at an angle of 45 degrees to show the thickness of the nickel mask in relation to the wheel.

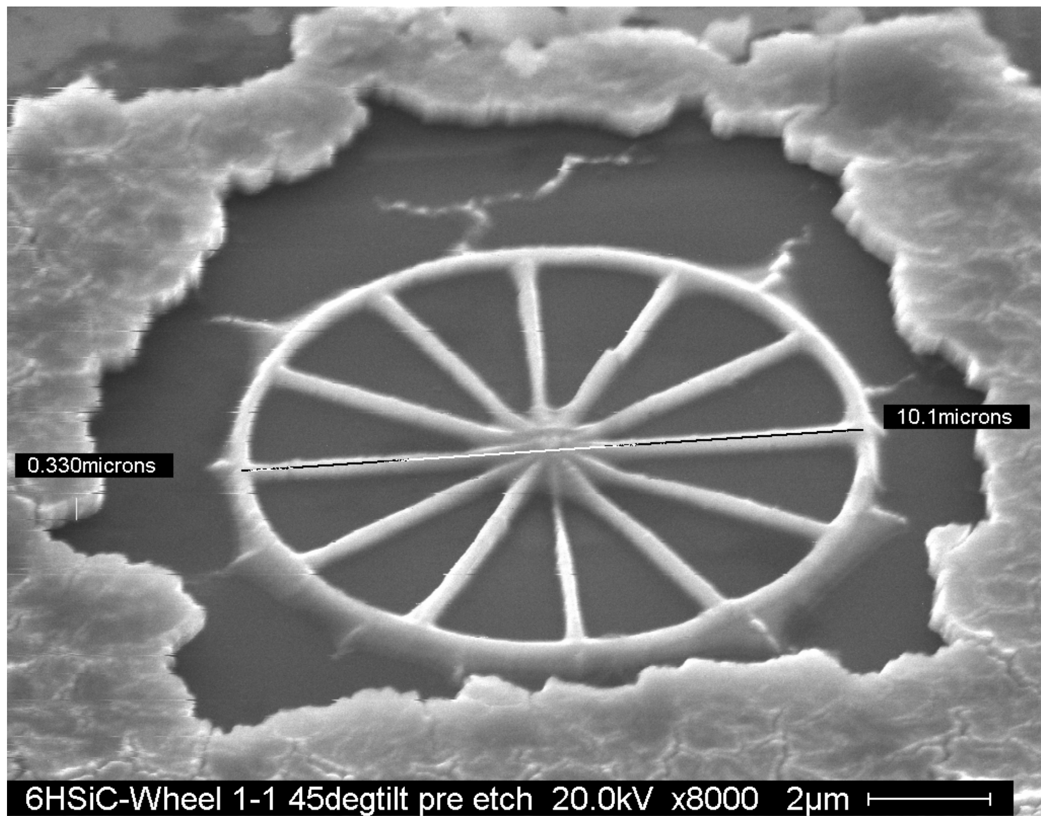

Figure 4.9 SEM image of the 425 $\mu C/cm^2$ dose wheel from Figure 4.6 after liftoff. This image was taken at a 45 degree angle to reveal the thickness of the nickel mask in relation to the wheel.

Figures 4.10 and 4.11 show a close-up of the wheel hub before and after etching, respectively. The 6H-SiC mesa between the wheel hubs shows extensive micromasking

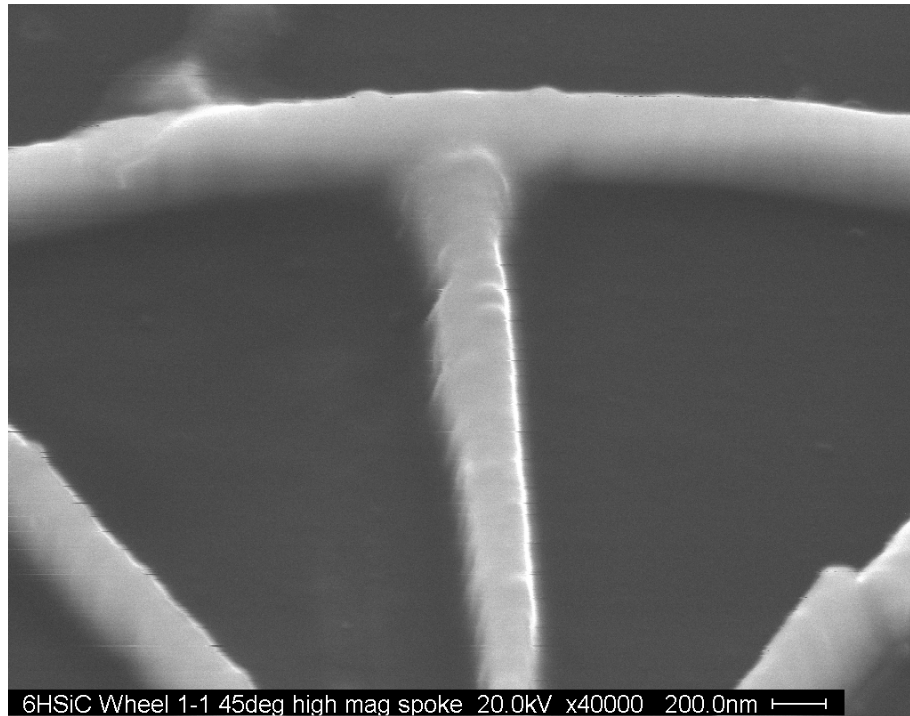

Figure 4.10 SEM micrograph of the wheel hub and 6H-SiC mesa from the wheel in Figure 4.9 before RIE.

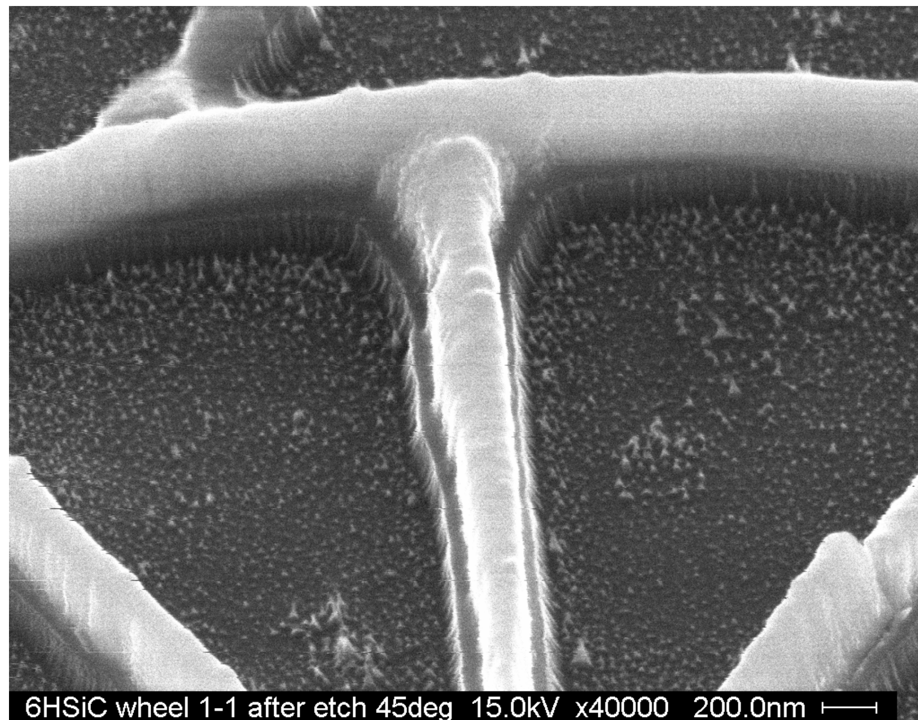

Figure 4.11 SEM micrograph of the wheel hub and 6H-SiC mesa from the wheel in Figure 4.9 after RIE, showing extensive micromasking.

due to the incomplete removal of the nickel after liftoff. This is likely due to the redeposition of the nickel from adjacent areas. Figure 4.12 shows a higher magnification image of the wheel hub where the etch depth was measured to be 213 nm. Because this image was tilted at 45 degrees, the etch depth was found by dividing the vertical measurement of 151 nm by sin (45°) or 0.707. This gives an etch rate of 42.6 nm/min which is considerably higher than the 100 watt etch on 3C-SiC. The micromasking can be seen in greater detail here and appear as small spikes on the order 20 nm in diameter.

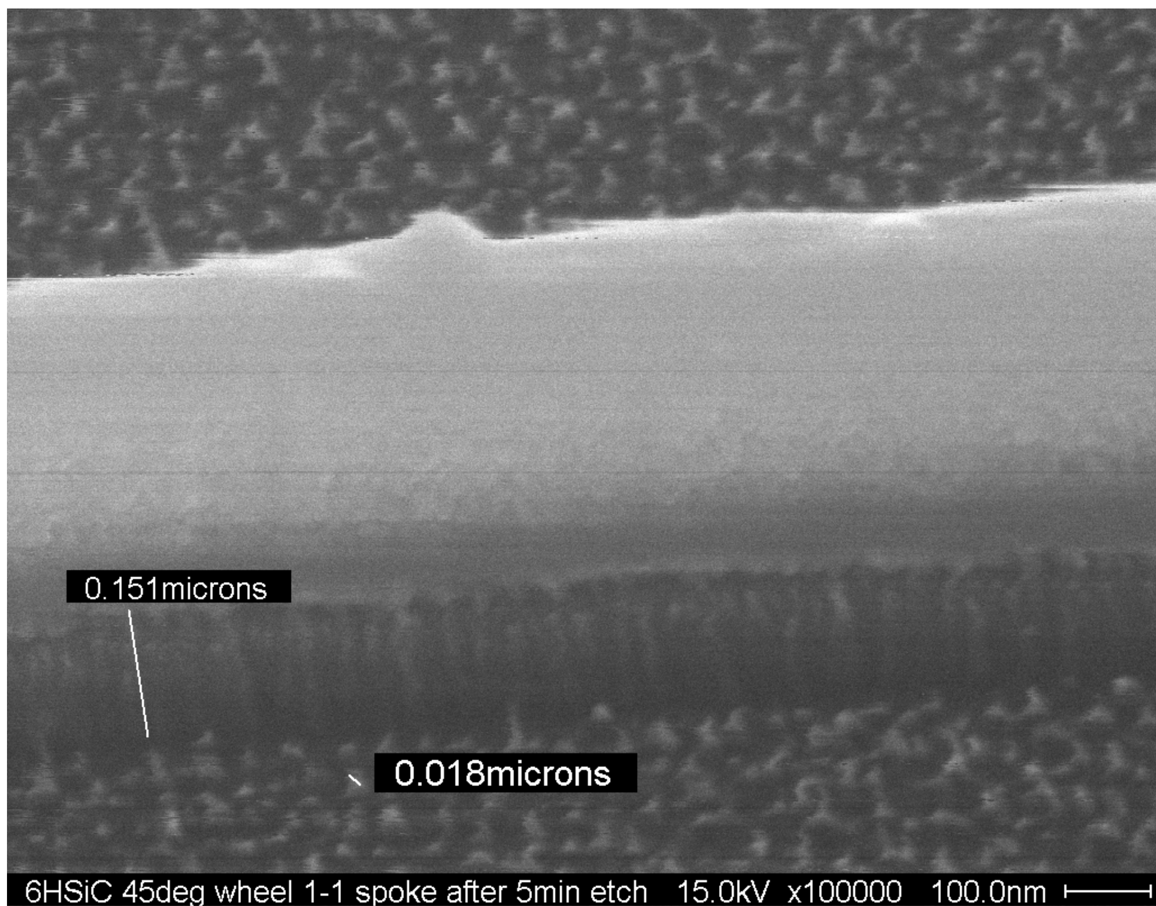

Figure 4.12 Close up SEM micrograph of the wheel hub and 6H-SiC mesa from Figure 4.9 after RIE, showing the etch depth of 151 nm, as measured at 45 degrees. This corresponds to an actual depth of 213 nm. From this the etch rate was calculated to be 42.6 nm/min for 6H-SiC.

4.6 Electron Beam Lithography of 4H-SiC

EBL was then performed on 4H-SiC die also prepared as presented in section 3.2. Figures 4.13 and 4.14, show SEM micrographs of the wheel dose array and nanodot arrays, respectively, after EBL and liftoff. The dosage used for each wheel and column were as labeled, in units of $\mu C/cm^2$. For this run the 600 $\mu C/cm^2$ wheel appeared to have performed the best, giving the most complete wheel after liftoff. Figures 4.15 and 4.16 show the wheel spokes magnified at 150,000X, before and after etching. These images were taken at a tilt of 85 degrees and show no signs of micromasking, which was present on the 6H-SiC sample. This is likely due to the fact that there is now only a very small amount of nickel in the vicinity of the patterns which could be redeposited. The etch power for this run was also 100 watts and was applied for 2 min. This resulted in an etch depth of approximately 42 nm as measured using SEM, giving an etch rate of ~21nm/min for the 4H-SiC. The nickel thickness also appears to have been reduced from 37 nm to 30 nm after the etch run. The error in measurement using the SEM can be on the order of a few nanometers, given the resolution is specified at 2 nm on a gold standard from the manufacturer [36]. The top edges of the nickel lines appear smoother and were also likely etched a few nanometers after the 2 minute etch run.

As was the case in the nanodot array in silicon, only the 30, 40 and 50 nm dots were developed in the resist on 4H-SiC. The 600 $\mu C/cm^2$ dose was included as one of the nanodot column doses as labeled in Figure 4.14 and also produced the most complete nickel dot patterns. Only the 40 and 50 nm dots were developed in this run on 4H-SiC. None of the 20 or 30 nm dots survived liftoff.

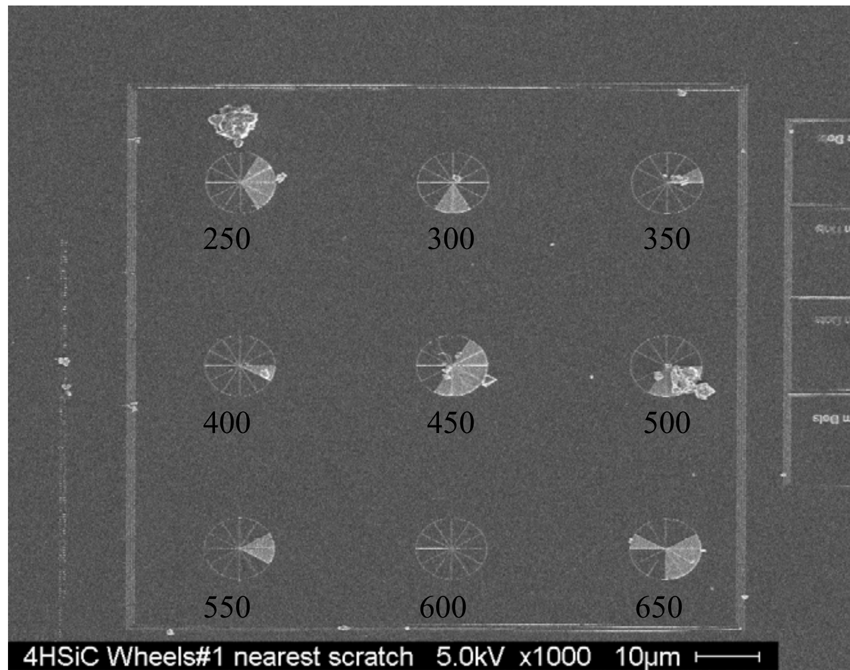

Figure 4.13 SEM micrograph of 4H-SiC wheel dose array after EBL and liftoff, showing the best wheel at a dose of 600 μC/cm^2.

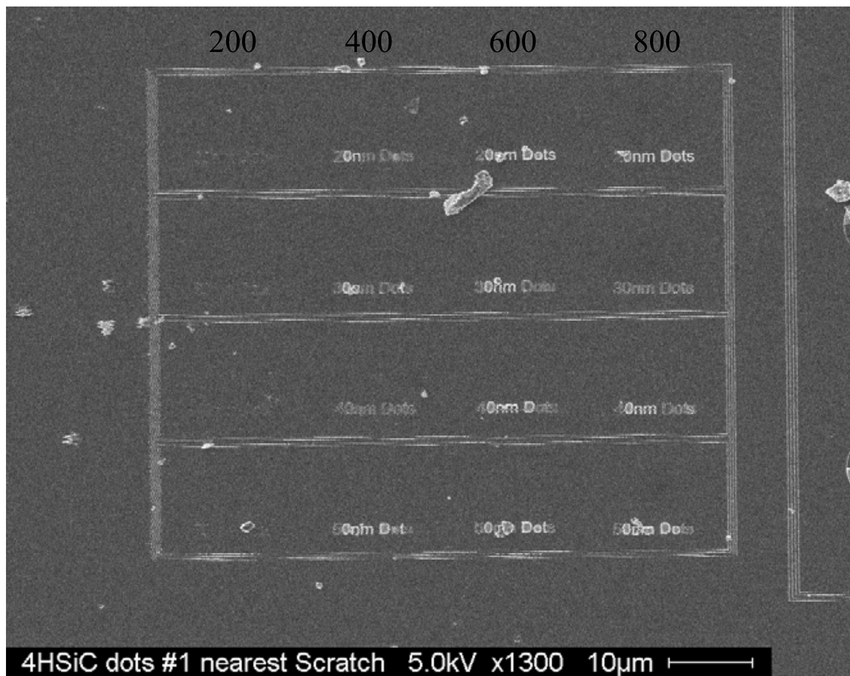

Figure 4.14 SEM micrograph of 4H-SiC nanodot array after EBL and liftoff. The 600 μC/cm^2 dose gave good dot formation for only the 40 and 50 nm dots.

Figure 4.15 SEM micrograph of 600 μC/cm^2 wheel spokes after EBL and liftoff, before RIE, showing a the thickness of the nickel mask.

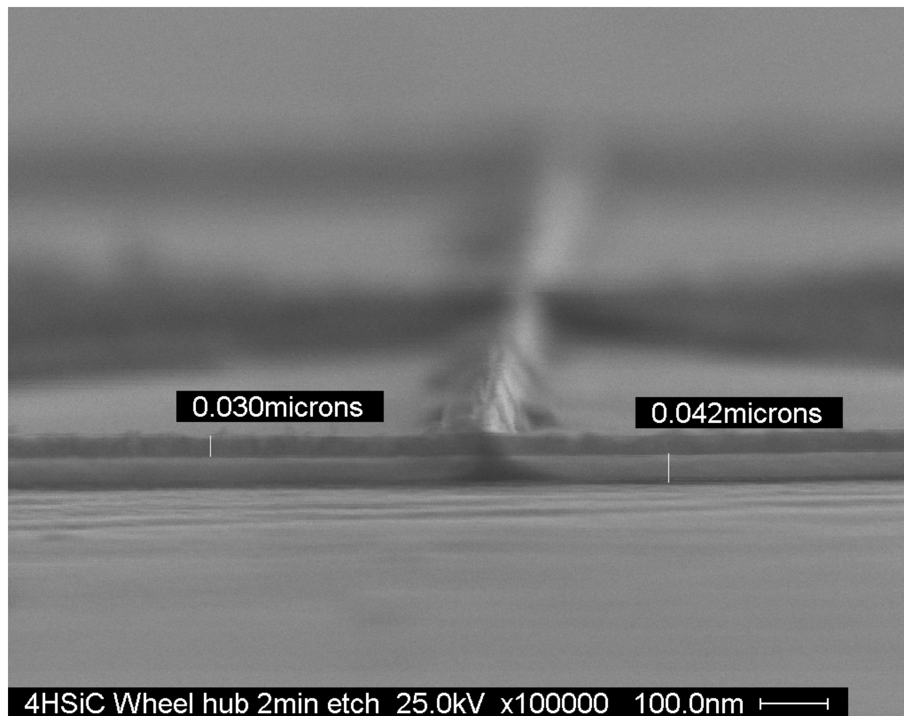

Figure 4.16 SEM micrograph of 600 μC/cm^2 wheel hub after a 2min RIE at 100 watts, showing the thickness of the nickel mask and the etch depth in the 4H-SiC.

Figure 4.17 shows an SEM image of the 40 nm nickel dots before etching and again show a height of 36 nm as measured on the image, which agrees well with the 37nm measurement made on the wheel spoke in Figure 4.15. Figure 4.18 shows these same nickel dots after the 2-minute etch run. The dot in the foreground shows a height of approximately 35 nm here, with a width of 55 nm at the base. Both the nickel dot and the SiC under it appear to have some taper. The taper in the nickel dot was also evident in the image before etching in Figure 4.17. The noise in these images and a few nanometers in measurement error are expected due to the fact that these pictures were taken at 300,000X, which is the highest magnification available on the Hitachi S-800 FE-SEM.

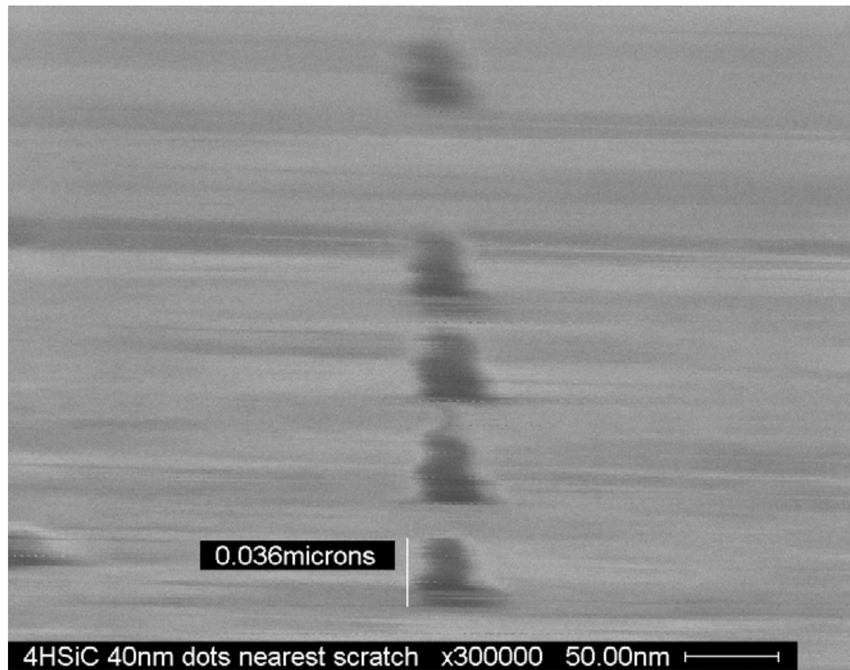

Figure 4.17 SEM micrograph of the 600 μC/cm^2 40 nm nickel dots before RIE. As measured from the Figure the dot height is 36 nm.

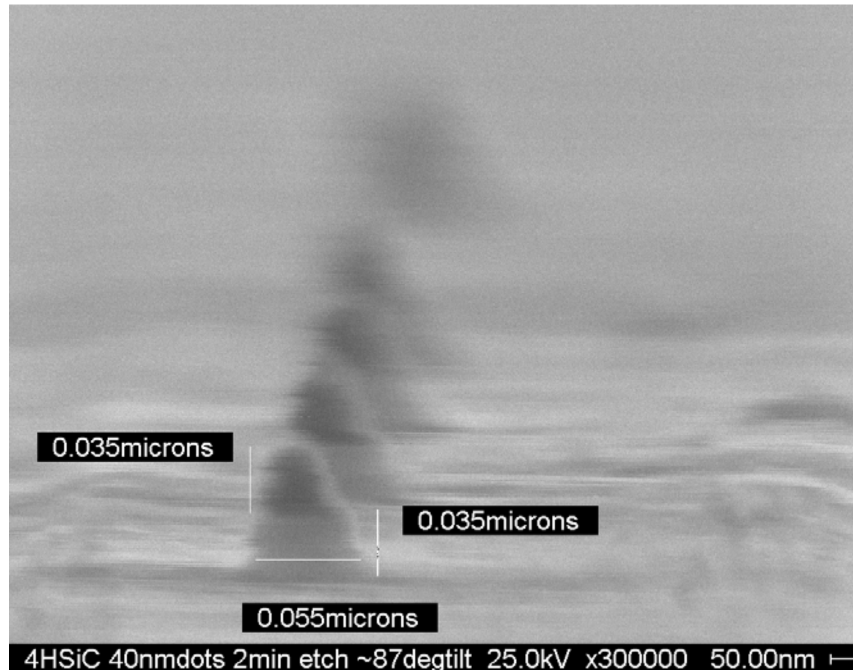

Figure 4.18 SEM micrograph of the same nickel dots after RIE, showing a dot height of 35nm and base width of 55nm.

At this magnification the slightest vibration or electromagnetic interference tends to cause noise, which makes accurate metrology very difficult. To measure features less than 50 nm, an SEM with higher magnification and resolution capability will be needed.

4.7 Summary

In the first section of this chapter, the procedures and lithography patterns used to optimize the electron beam profile were presented. Wheel and nanodot patterns were designed and used to determine the optimum electron dose needed to produce the smallest dots in PMMA resist on silicon. A spot burning technique was then developed to optimize the electron beam profile before pattern writing, 30 nm nanodots were successfully produced in the PMMA at a dose of 500 $\mu C/cm^2$.

These techniques were then applied to produce nanostructures on single crystal 6H- and 4H-SiC substrates. The final EBL runs yielded nanodots, which were measured to be 40 to 50 nm in diameter using a Hitachi FE-SEM.

Chapter 5

Conclusion

5.1 Conclusion

Electron Beam Lithography (EBL) has been used to pattern 40 nanometer diameter nanodots in single crystal silicon carbide. In Chapter 1, an introduction to nanotechnology and the general processes used to fabricate nanoscale structures was presented. Silicon carbide is an emerging electronic material and was chosen for this work because it is a wide bandgap material and has excellent material properties, which allow it to be used in high power and/or high temperature applications. SiC is also biocompatible, hence processing SiC material surfaces to contain nanoscale features may find applications in chemical and biological sensing and medical technology. While the applications of nano-textured SiC surfaces have yet to be fully identified, clearly the first step is to create such surfaces. Only then can technologists study the interaction of nano-scale SiC features with chemical and biological systems and matter.

Many of the process techniques and terminologies used in EBL have come from optical lithography. Since optical lithography is also the main technique used in large scale patterning of semiconductors, a general review of this technique was given in Chapter 2. A general introduction to EBL and scanning electron microscopy SEM, were also presented in Chapter 2.

In this work an EBL system was constructed by retrofitting a JEOL SEM with a commercially available nanometer pattern generation (NPGS) system. An electrostatic

beam blanker was also added to the system to to avoid exposing the resist between patterns. An ion pump was added to the SEM electron gun chamber to improve the vacuum, thus decreasing contamination of the electron optics and allowing longer filament life in the electron source. An ion gauge was also added to the system to monitor the vacuum level during EBL patterning. As discussed in Chapter 3, an EBL process was developed and optimized on silicon first and then on silicon carbide to produce nanoscale structures in poly-methyl-methacrylate, (PMMA) resist. An RIE process was then developed on 3C-SiC to etch these patterns into silicon carbide crystals, using an electron beam deposited nickel mask and liftoff processing.

Initial EBL test runs on silicon were able to produce 50 nm diameter features in PMMA resist on silicon. Pattern arrays using wheel and dot structures were designed to determine the optimum electron dose, as seen in Chapter 3. After process optimization, using a spot burning technique, this was reduced to approximately 20 nm diameter in PMMA resist on silicon. Dots as small as 10 nm in diameter were produced in resist that was under exposed. As presented in Chapter 4, these processes and patterns were then applied to silicon carbide material. After patterning and resist development, nickel was deposited to form a mask layer for RIE to etch the patterns into the silicon carbide surface. The resulting structures were then characterized using FE-SEM. The FE-SEM results show the successful synthesis of 4H-SiC nanodots from the 40 and 50 nm diameter dot arrays. The nanodots from the 40 nm array had a tapered profile and were measured to be 55nm at the base.

5.2 Future Work

To create reproducible structures smaller than 40 nm diameter, additional steps will have to be taken to reduce the interference and noise in the EBL facility. The Hitachi FE-SEM used to characterize the nanodots was used at its absolute maximum magnification. To accurately characterize structures much smaller than this will require an electron microscope that can produce images with higher resolution and less noise. Improvements can also be made in the JEOL JSM-840 SEM to increase the EBL resolution. This would involve replacement of the tungsten thermionic emitter with a lanthnanum hexaboride (LaB6) emitter. As shown in Table 2.2 of Section 2.4.1, the brightness of a LaB6 emitter can be an order of magnitude higher than a tungsten emitter. In addition, as can be seen in Table 2.2, LaB6 also has a smaller source size, which should improve the resolution for EBL

Since successful 20 nm diameter dots were produced in the PMMA resist, it should be possible to synthesize structures of this size and possibly smaller. The tapered profile seen in the silicon carbide nanodots SiCNDs in Chapter 4 may be due to the fact that the electrons immediately begin to diffuse laterally as they pass through the resist. For the EBL in this research a single 195 nm resist layer was used. As seen in the literature, it is possible a double layered resist structure can yield higher resolution and could help mitigate this effect [46]. This would entail using a two layered resist using a more sensitive resist in the top layer and performing experiments in which the thickness of these layers are varied to compensate for electron scattering.

One interesting outcome from the PMMA nanodot experiments in Section 4.3 were the 300 and 400 $\mu C/cm^2$ doses for the 30 nm dot array in Figure 4.5. These

appeared to produce holes in the resist, which were less than 10 nm. These arrays were considered under exposed because they did not produce dots 30 nm in diameter as specified by design. Experiments designed to determine if this effect can be controlled to reproduce dots less than 10 nm should be conducted. Atomic force microscopy (AFM) or a higher resolution SEM than the one that was used for the metrology in this work would have to be used in this case to accurately image and measure dots of this size. Extensive AFM studies could also be performed to determine the effect of surface roughness on the resultant EBL. These studies should be performed on the SiC surface as received, after coating with PMMA and after PMMA exposure. AFM may be able to verify if the 10 nm dots seen in Figure 4.5 have been completely developed through to the substrate.

Another area to be explored is a study of the aspect ratio possible in SiC using EBL. High aspect ratio dots or columns would be useful for their high surface area in variety of applications. Experiments should also be performed to determine if low dimension hollow cylinders with high aspect ratios can be produced using EBL to form SiC nanotubes. These would also be useful for high surface area structures if they can be practically made with high aspect ratios and with diameters in the 10 nanometer range. As discussed in Section 1.3.3, once functionalized these high area surface area structures will be useful for such devices as chemical and biological sensors and in hydrogen storage applications.

Experiments should also be performed to refine the RIE process used for etching the SiC. These would include experiments with a range of the RIE process parameters

including the gas composition, pressure and RF power. Different mask materials may also be tested to increase the etch selectivity and produce more defined edges.

Other experiments will include a study of the effects of SiC polytype on low dimensional structures. The a lattice constant of Cubic 3C-SiC is 0.436 nm, while the a and c lattice dimensions of hexagonal 6H-SiC are 0.308 and 1.512 and for 4H-SiC, 0.308 and 1.008 nm, respectively [5]. It can be expected that as the dimensions of SiC nanostructures approach the nanometer range, the lattice constant size may become a factor. In the case of 6H-SiC a 10 nm diameter dot may only be 6 or 7 units across, if the c lattice dimension is parallel to the surface.

References

1. *Nanoelectronics and Information Technology*, edited by Rainer Waser, (WILEY-VCH Verlag GmbH & Co. KgaA, Weinheim, c2003) p 625.

2. P.J. Breton, "From Microns to Nanometers: Early Landmarks in the science of Scanning Electron Microscope imaging", *Scanning Microscopy* Vol. 13, No.1, 1999 (pages 1-6).

3. http://www.jeol.com/sem/semprods/jsm7700f.html.

4. Boon K. Teo, "Doing chemistry on low-dimensional silicon surfaces: silicon nanowires as platforms and templates", *Coordination Chemistry Reviews*, Volume 246, Issues 1-2, November 2003, Pages 229-246.

5. *Process technology for silicon carbide devices,* edited by Carl-Mikael Zetterling, London : INSPEC, c2002.

6. Peter Råback, *Modeling of the Sublimation Growth of Silicon Carbide Crystals*, Ph.D. dissertation, Helsinki University of Technology, Helsinki Finland, June 1999.

7. Cree. Inc., 4600 Silicon Drive Durham, NC 27703.

8. Cree. Inc., 4600 Silicon Drive Durham, NC 27703. (http://www.Cree.com/Products/sic_silicarb.asp).

9. Mehran Mehregany and Christian A. Zorman, *SiC MEMS: opportunities and challenges for applications in harsh environments, Thin Solid Films*, Volumes 355-356, 1 November 1999, Pages 518-524.

10. Conrad R. Stoldt, Carlo Carraro, W. Robert Ashurst, Di Gao, Roger T. Howe and Roya Maboudian, *A low-temperature CVD process for silicon carbide MEMS, Sensors and Actuators A: Physical*, Volumes 97-98, 1 April 2002, Pages 410-415.

11. Jean-Mario Nhut, Ricardo Vieira, Laurie Pesant, Jean-Philippe Tessonnier, Nicolas Keller, Gaby Ehret, Cuong Pham-Huu and Marc J. Ledoux, "Synthesis and catalytic uses of carbon and silicon carbide nanostructures*", Catalysis Today*, Volume 76, Issue 1, 1 November 2002, Pages 11-32.

12. B. Q. Wei, J. W. Ward, R. Vajtai, P. M. Ajayan, R. Ma and G. Ramanath, "Simultaneous growth of silicon carbide nanorods and carbon nanotubes by chemical vapor deposition*", Chemical Physics Letters*, Volume 354, Issues 3-4, 12 March 2002, Pages 264-268.

13. A. Tibrewal, *Oxidation of single crystal SiC in flowing plasma after-glow*, MS Thesis, University of South Florida, Tampa Fl, Nov. 2002.

14. A. G. Revesz and H. L. Hughes, "The structural aspects of non-crystalline SiO_2 films on silicon: a review", *Journal of Non-Crystalline Solids, Volume 328, Issues 1-3, 15 October 2003, Pages 48-63.*

15. K.E. Bean, "Anisotropic etching of silicon", *IEEE Trans. Electron Devices,* ED-25 (1978), pp. 1185–1193.

16. V. Kandregula, *Reactive Ion Etching of SiC in Fluorinated Plasmas*, MS Thesis, University of South Florida, Tampa Fl, Nov. 2002.

17. Silva K. Thesis, M. J. Caturla, M. D. Johnson, J. Zhu, T. Lenosky, B. Sadigh and T. Diaz de la Rubia, "Atomic scale models of ion implantation and dopant diffusion in silicon", *Thin Solid Films*, Volume 365, Issue 2, 17 April 2000, Pages 219-230.

18. T. M. Anklam, L. V. Berzins, D. G. Braun, C. Haynam, T. Meier and M. A. McClelland, "Evaporation rate and composition monitoring of electron beam physical vapor deposition processes", *Surface and Coatings Technology*, Volumes 76-77, Part 2, December 1995, Pages 681-686.

19. K. L. Choy, "Chemical vapour deposition of coatings", *Progress in Materials Science*, Volume 48, Issue 2, 2003, Pages 57-170.

20. Alain Dollet, "Multiscale modeling of CVD film growth--a review of recent works", *Surface and Coatings Technology*, Volumes 177-178, 30 January 2004, Pages 245-251.

21. J. S. Williams, "Ion implantation of semiconductors", *Materials Science and Engineering A*, Volume 253, Issues 1-2, 30 September 1998.

22. S. E. Saddow, M. Mynbaeva, M. C. D. Smith, A. N. Smirnov and V. Dimitriev, "Growth of SiC epitaxial layers on porous surfaces of varying porosity", *Applied Surface Science*, Volume 184, Issues 1-4, 12 December 2001, Pages 72-78.

23. Bernard Fay, "Advanced optical lithography development, from UV to EUV", *Microelectronic Engineering*, Volumes 61-62, July 2002, Pages 11-24.

24. Kuide Qin, Brij Moudgil and Chang-Won Park, “A chemical mechanical polishing model incorporating both the chemical and mechanical effects”, *Thin Solid Films*, Volume 446, Issue 2, 15 January 2004, Pages 277-286.

25. N. P. Hung, Y. Q. Fu and M. Y. Ali, “Focused ion beam machining of silicon”, *Journal of Materials Processing Technology*, Volume 127, Issue 2, 30 September 2002, Pages 256-260.

26. Thomas P. Niesen and Mark R. De Guire, “Review: deposition of ceramic thin films at low temperatures from aqueous solutions”, *Solid State Ionics*, Volume 151, Issues 1-4, November 2002, Pages 61-68.

27. Liang, J., et. al., “Two-dimensional lateral superlattices of nanostructures: Nonlithographic formation by anodic membrane template“, *Journal of Applied Physics*, v. 91 no. 4 (February 15 2002) p. 2544-6.

28. M.A. McCord, M.J. Rooks, *Handbook of Microlithography, Micromachining and Microfabrication*, Chapter 2, Electron Beam Lithography, Vol. 1, SPIE, The International Society for Optical Engineering, Bellingham WA, 1997 pages 128-252.

.

29. Frank Gottschalch, Thomas Hoffmann, Clivia M. Sotomayor Torres, Hubert Schulz and Hella-Christin Scheer, “Polymer issues in nanoimprinting technique”, *Solid-State Electronics*, Volume 43, Issue 6, June 1999, Pages 1079-1083.

30. Shipley Company, 500 Nickerson Road Marlborough, MA 01752, USA.

31. ASML US Inc., 8555 South River Parkway Tempe, AZ 85284, USA.

32. Christopher Vieu, Franck Carcenac and Huguette Launois, "From Nano- to Macroscale Science and Technology”, *Condensed Matter* News - Vol 6, Issue 3-4, p22-30, (1998).

33. Goldstein, et. al*, Scanning Electron Microscopy and X-ray Microanalysis*, Plenum Press, New York, 1981, p 30.

34. R.H. Fowler and L.W. Nordheim, *Proc. R. Soc.*, *London A* 119 (1928), p. 173.

35. Todd and Rhodin, *Surface Science*, vol. 42, 1974 p 109.

36. *JEOL JSM-840 operating manual*.

37. J. C. Nabity Lithography systems PO Box 5354 Bozeman, MT 59717. (http://www.jcnabity.com).

38. MicroChem Corp.1254 Chestnut Street Newton, MA 02464. (http://www.microchem.com/products/pmma.htm).

39. MicroChem Corp.1254 Chestnut Street Newton, MA 02464.

40. Upperspace (makers of DesignCAD, formerly ViaGrafix), Software Division, One American Way, Pryor, OK 74361, USA.

41. J. C. Nabity Lithography systems PO Box 5354 Bozeman, MT 59717. (http://www.jcnabity.com/pictures.htm#Exposure%20Guide).

42. A. L. Syrkin, J. M. Bluet, J. Camassel and R. Bonnot, “Reactive ion etching of 6H-SiC in an ECR plasma of CF4-O2 mixtures using both Ni and Al masks”, *Materials Science and Engineering B*, Volume 46, Issues 1-3, April 1997, Pages 374-378.

43. Rachael Myers, *CVD Growth of SiC on Novel Si Substrates*, Master's Thesis, University of South Florida, Tampa, FL, Oct, 2003.

44. Stephen E. Saddow, *Optical Control of Microwave Integrated Circuits Using High-Speed Photoconductive Switches,* Ph.D. Dissertation, University of Maryland, College Park MD, Dec., 1993.

45. W. Reichert, D. Stefan, et.al., “Fabrication of Smooth, SiC Surfaces by Reactive Ion Etching using a Graphite Electrode”, *Materials Science and Engineering B46*, (1997) 190-194.

46. T. Köster, B. Hadam, J. Gondermann, B. Spangenberg, H. G. Roskos, H. Kurz, J. Brunner and G. Abstreiter, “Investigation of Si/SiGe heterostructures patterned by reactive ion etching”, *Microelectronic Engineering*, Volume 30, Issues 1-4, January 1996, Pages 341-344.