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# Design and Fabrication of a Re-Configurable Micromirror Array for an Optical Microspectrometer

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Design and Fabrication of a Re-Configurable Micromirror Array

for an Optical Microspectrometer

by

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DEDICATION


To my dear parents,

Shree L.D. Upadhyay and Shrimati Rekha Upadhyay

and my loving fiancé

Nikhil

ACKNOWLEDGEMENTS

TABLE OF CONTENTS

# LIST OF TABLES

iii

## LIST OF FIGURES

DESIGN AND FABRICATION OF A RE-CONFIGURABLE MICROMIRROR

ARRAY FOR AN OPTICAL MICROSPECTROMETER

Vandana Upadhyay

ABSTRACT

This thesis presents the design and fabrication of a re-configurable micromirror array which can be used as a component of an optical microspectrometer. In an optical microspectrometer, an array of mechanically positionable micromirrors can be implemented as a reconfigurable exit slit to selectively focus particular wavelengths of a diffracted spectrum onto the detector stage. The signal to noise ratio and response time of an optical microspectrometer can be vastly improved by this technique.

In the approach presented here, a hybrid bulk- and surface- micromachining process is demonstrated for fabrication of a 1XN array of micromirrors. The reconfigurable micromirrors presented here comprise of two elements, a surface-micromachined positioning mechanism, and a bulk-micromachined mirror. These elements are finally integrated using a flip-chip bonding technique. The integrated micromirror assembly can be positioned by means of a driving mechanism consisting of arrayed electrothermal actuators. Various techniques for fabricating the micromirror array

components are discussed in detail in this thesis along with a review of techniques applicable for integrating the individual components.

In order to enhance the efficiency of the positioning system, the classic electrothermal actuators were redesigned in this research. The modified design of thermal actuators is introduced in this thesis. An analysis of the modified thermal actuators is also presented to demonstrate the validity of the suggested modifications.

CHAPTER 1

INTRODUCTION

1.1.    Optical-MEMS

MEMS (Micro Electro Mechanical Systems) is a technology implemented for the
fabrication of integrated mechanical and electronic devices having dimensions in the
ranging from micrometers to millimeters [1]. MEMS is regarded as an "enabling
technology" owing to the tremendous augmentation it offers to conventional technology.
Some of the advantages of the microfabrication approach are inexpensive batch
fabrication, small size, and compatibility with VLSI processing. Pressure sensors,
accelerometers, print-heads, and micromirror displays are few examples of MEMS
enabled devices that are widely utilized and are commercially successful at present.

Bulk and surface micromachining are two classes of microfabrication. Bulk
micromachining involves the fabrication of a MEMS element by selectively etching away
the bulk material. Silicon is the most widely used material for bulk micromachining
because of its excellent material properties [2]. Surface micromachining refers to the
microfabrication technique wherein layers of materials are deposited on a substrate and
subsequently selectively etched to fabricate a microstructure. The thicknesses of the

various deposited layers typically range from a few hundred Angstroms to a few microns. Polycrystalline silicon is the most widely used material in surface micromachining [3]. The two classes of micromachining have their own advantages and drawbacks. Surface micromachining is generally not employed for fabrication of high aspect ratio structures while bulk micromachining process steps can be easily designed for very high aspect ratio features. Another drawback associated with surface micromachined devices is the presence of residual stresses commonly associated with thin film deposition steps. Residual stress is hardly an issue in micromachined structures. The release of the sacrificial material used in surface micromachining often introduces problems of stiction in features with large surface areas. On the positive side, surface micromachining facilitates better dimensional control of features and allows easier integration of electronics. Structures with arbitrary features can be easily fabricated using this method. Surface micromachining is especially attractive for manufacturing high feature density microstructures. A favorable combination of the above fabrication techniques can be selected in order to best suit the requirements of a particular device. Hybrid surface-bulk micromachined systems that utilize the advantages of both these techniques have been demonstrated elsewhere [4], [5].

The application of MEMS to produce integrated optical systems and micro-optical components is known as Optical-MEMS or MOEMS (Micro-Optical-Electrical-Mechanical Systems). A multitude of both passive and actuated micromachined optical devices have been demonstrated so far including micromirror display systems [6], diffraction gratings [7], variable optical attenuators (VOA), etalons, beam splitters, scanners [8], and switches.

1.2.    Microspectrometer


Spectroscopy is the science of experimental observation, measurement and analysis of optical spectra. Table 1 lists the various regions of the optical spectrum. Spectral analysis of emission and absorption spectra is a fundamental tool for detection of chemical and biological specimens. Optical spectrometers are grating based devices used to separate light into its constituent wavelengths and analyze the resulting spectrum.

Table 1.    Various regions of the optical spectrum [9].

| No. | Component | Wavelength Range |
|-----|-----------|------------------|
| 1 | Vacuum Ultraviolet | 5 Å – 2000 Å |
| 2 | Ultraviolet | 2000 Å – 4000 Å |
| 3 | Visible | 4000 Å – 7000 Å |
| 4 | Photographic infrared | 7000 Å – 1.2 μm |
| 5 | Infrared | 1.2 μm – 40 μm |
| 6 | Far infrared | 40 μm – 1000 μm |

The chief parameters that characterize an optical spectrometer are [10]:

i)     Etendue or Luminosity - also known as light gathering power, denotes the amount of light that passes from through the instrument on to the detector.

ii)    Spectral Resolution - spectral resolution is inversely proportional to the linear dispersion of a spectrometer. The term linear dispersion signifies the extent of spatial separation of two wavelengths in the focal plane.

iii)   Resolution – Luminosity Product: it is the efficiency of a spectrometer and is often used to compare the performance of two spectrometers.

iv)    Free Spectral Range - the range of wavelengths that a spectrometer can

detect.

The various components of a typical optical spectrometer are: light source, sampling interface, entrance and exit slits, collimating lens/ mirror, focusing lens / mirror, dispersion element and detectors. Based on the arrangement of these components, various configurations of optical spectrometers have been designed e.g. Fabry-Perot, Czerny-Turner [10]. Figure 1 below shows the set-up of a Czerny-Turner mounting spectrometer [11].
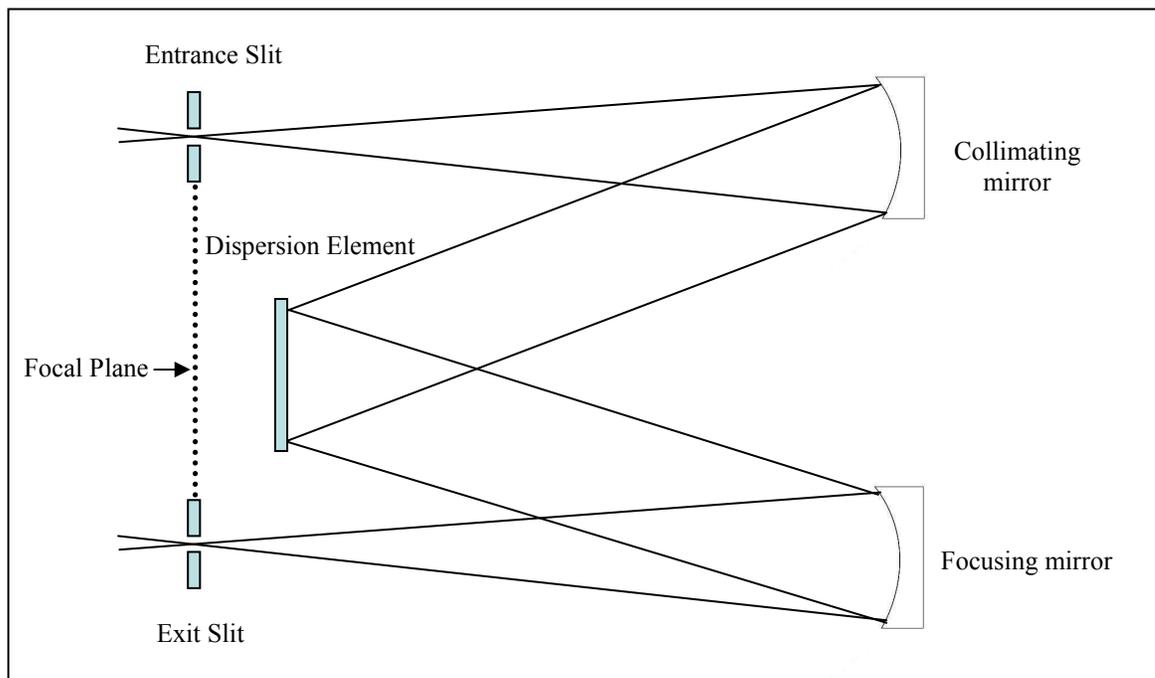


Figure 1.    Configuration of a Czerny-Turner spectrometer. Adapted from [11].

The collimating lens/mirror is used to collimate the light incident on it from the entrance aperture. Diffraction gratings serve to spatially separate incident light into its constituents. Light diffracted by the grating is directed to the focusing mirror which then

focuses the diffracted light onto the detectors. The detector is typically an array of CCDs (Charge Coupled Detectors) or photodiodes that is situated at the output of the exit slit.

The optical resolution of a spectrometer is determined by the design of the diffraction grating and dimensions of the entrance and exit optics. The important parameters of any diffraction grating are: groove density, spectral range, blaze wavelength and efficiency. Groove density, specified in units of mm$^{-1}$, is directly proportional to the optical resolution of a diffraction grating [9].

Some of the advantages of MEMS based spectrometers are: small size, low cost, fast response, high signal to noise ratio, reduced complexity and low power consumption. MEMS based spectrometers pertaining to several configurations and implementing both reflective and diffractive optical elements have been designed and fabricated in earlier efforts [12], [13], [14].

1.3.    Micromirror array in microspectrometer

Micromachined mirror arrays have been a focus of active research in the field of MOEMS and find application in optical systems such as beam deflectors, choppers, spatial light modulator (SLM) displays [6] , optical cross-connects (OXC), switches, and scanners [8]. The key features of an ideal micromirror array are: a 100% fill-factor, minimum surface roughness and high reflectivity (ideally 100%) in the wavelength range of interest, zero insertion loss, zero noise, simple control, and identical deflection versus input energy response [15].

A unique application of micromachined mirrors can be performance enhancement of a spectrometer by selectively focusing a particular spectral component on a detector thereby reducing the number of detectors required. Scanning of the entire wavelength range of interest can be carried out by sequentially activating a series of such mirrors. The ability to focus or block the desired wavelength components of a spectrum incident on the detector improves the signal to noise ratio of the spectrometer device. Application of this technique effectively overcomes the limits of generic spectral sensing systems that have a high response time due to the large volume of data acquisition and processing tasks carried out at the detector stage. The method of utilization of micromirrors to enhance a spectrometer performance has been reported earlier [16].

In this research, the basic idea was to fabricate a 1-dimensional array of mirrors wherein each mirror can be individually controlled. In this arrangement (see Figure 2), the micromirror array effectively acts as the exit slit of a spectrometer.
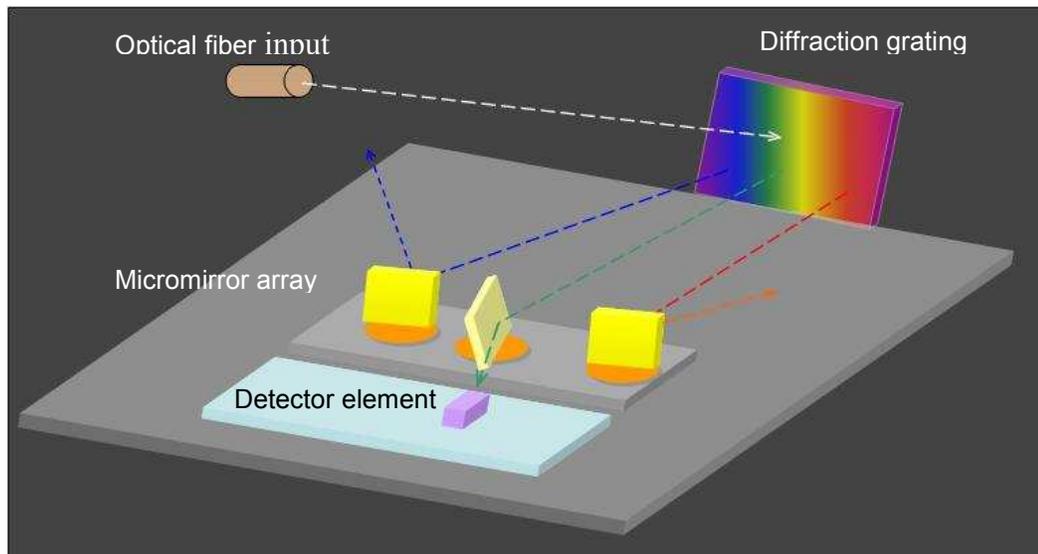


Figure 2.    Schematic diagram of a microspectrometer set-up utilizing a micromirror array.

The width of the exit slit (mirror) is directly proportional to the Bandpass or Spectral Bandwidth of a spectrometer. The bandpass of a spectrometer is defined as the wavelength interval of light that is incident upon the detector [17]. An instrument with a smaller bandpass can resolve closely located wavelengths. Reduction of the slit width (micromirror size) is one method of reducing the bandpass. However, this method also results in a decrease of the light intensity. The trade-off between the spectral bandwidth and light intensity should be kept in mind while designing a spectrometer for a particular application. This research builds upon earlier work reported by P.R. Baddam [18]. The various issues discussed in [18] are highlighted below followed by a review of requirements for a new design.

1.3.1.  Micromirror array - previous design

Figure 3 shows the SEM image of a micromirror fabricated, in an earlier work [18], entirely by PolyMUMPs (Polysilicon Multi-User-MEMS-Process) that is a commercial surface micromachining process [19].
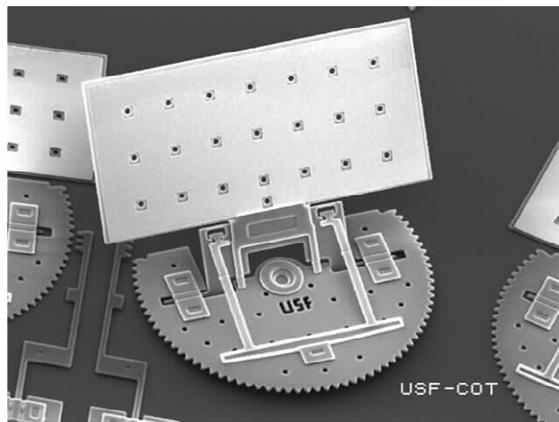


Figure 3.      SEM image of surface-micromachined micromirror fabricated in [18].

Here, a rotary stage system was designed to mount the micromirrors and a micro-machined actuator assembly was designed to position the rotary stages. The dimensions of the various components of this device are shown in Table 2.

Table 2.    Key architectural features of micromirror array designed in [18].

| No. | Dimension and Unit | Value |
|---|---|---|
| 1 | Mirror width $M_w$, μm | 214 |
| 2 | Mirror height $M_h$, μm | 105 |
| 3 | Mirror thickness $M_t$, μm | 2 |
| 4 | Mirror % reflective area | 95.2 |
| 5 | Rotary stage diameter D, μm | 180 |
| 6 | Mirror array pitch $M_p$, μm | 230 |
| 7 | Linear fill factor, % | 93 |
| 8 | Device foot print, mm | 1.95 |

There are several disadvantages in this approach; first, the mirror surface has holes in it that are required by the design rules for the proper release of the PolyMUMPs chip. These holes act as slits in the mirror surface thereby causing the diffraction of incident light eventually resulting in noise. It has been demonstrated in an earlier study [20] that such holes cause optical losses by causing diffraction of incident light and reduction of surface reflectivity.

Another drawback of the mirror shown in Figure 3 is that an additional mechanism is required to hoist the mirror up from the horizontal plane. This mechanism needs to be later disconnected from the mirrors using FIB (Focused Ion Beam) micromachining in order to allow free and independent rotation of the mirrors in the array. The hoisting mechanism described here consumes significant chip space. The FIB micromachining required here is not cost-effective for mass production of micromirror devices. The additional steps required for the hoisting and disconnecting process require

8

precision and are time consuming. In addition, these processes can result in damage to the released devices hence reducing yield.

A third issue is that a locking mechanism is required to hold the hoisted mirror in place. Figure 4 shows a SEM image of the locking mechanism implemented here. This mechanism is prone to failure due to fatigue. Moreover, fabricating the out-of-plane mirror according to the PolyMUMPs process requires that the rotary stage be designed as a half-gear in order to allow space for the mirror structure. Complete control of the gear movement is not possible in the case of a half-gear since the rotary stage might get positioned in a state where it is out of reach for the pushing arm.
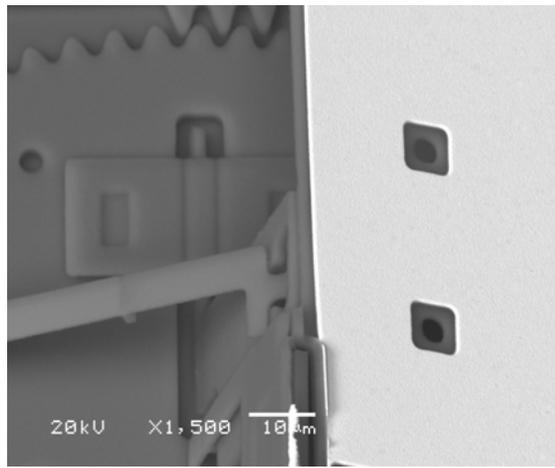


Figure 4.    SEM image of locking mechanism employed to hold the micromirror in a vertical position [18].

Finally, since the polysilicon (poly-Si) and gold micromirror is fabricated by a surface -micromachining process it has some residual stress present. This stress causes curvature of the mirror surface which results in high insertion loss and crosstalk. In a study, Zou et al. [20] have compared the reflectivity of gold-coated mirrors fabricated using monocrystalline silicon, LPCVD poly-Si and PolyMUMPs poly1 layer. This study

indicates that monocrystalline silicon mirror gives the best results and closely resembles an ideal reflector surface.

## 1.3.2.  Motivation for design modification

In order to address the issues discussed above, a different design approach needs to be considered. Hence the motivation for this research was to combine the favorable features of both surface and bulk micromachining methods for fabrication of a re-configurable micromirror array, henceforth referred to as RMA. Enhancement of the rotary stage, the actuating mechanism and the micromirrors was also desired in order to produce a simple, low optical loss system with zero stress reflective surface, high mechanical stability, and flexible design [21].

## 1.4.  Thesis outline

The design of a gear and ratchet assembly is presented in Chapter 2. The design of the modified thermal actuators and simulation results for the various designs employed in the rotary stage driving mechanism are also discussed in Chapter 2.

The design of the bulk-micromachined micromirror array is discussed in Chapter 3 along with an overview of the fabrication process steps involved. This chapter also includes a discussion on the investigation of bonding techniques suitable for a hybrid surface and bulk micromachined micromirror fabrication process.

Chapter 4 consists of a detailed description of the various processes used for fabricating the micromirror array. Wet and dry etching techniques and the various thin film deposition steps are also discussed in this chapter.

Chapter 5 finally outlines the conclusion of this thesis and recommendations for future work

CHAPTER 2


DESIGN OF MICROMIRROR POSITIONING SYSTEM


2.1.    Overview


The micromirror positioning system is a surface micromachined rotary stage that can be moved to the desired position by means of a thermal actuator based driving mechanism. Figure 5 presents the solid model of the rotary stage assembly. This model was designed and generated using a MEMS design and analysis software program- CoventorWare[TM] version 2003.1[1]. As shown in Figure 5, the rotary stage wheel is maneuvered by a "pushing-arm" which is in turn driven by a mechanism consisting of an array of thermal actuators. Electrical input is supplied to the system through the bond pads illustrated below.

A similar micromirror positioning mechanism was fabricated earlier [18]. The design discussed here introduces the following changes in the system described previously [18]:

i)      Addition of a ratcheting arrangement to the rotary stage to allow

        unidirectional motion.

[1] Coventor, Inc., 4000 CentreGreen Way, Suite 190, Cary, NC 27513.

ii) Enhancement of gear plate and tooth designs for smooth engagement, low stiction, and successful integration with the micromirror array.

iii) Modification of thermal actuator geometry to reduce probability of device failure.

iv) Reduction of device foot-print for more efficient utilization of chip space.

The details of the various design modifications are discussed in the following sections.
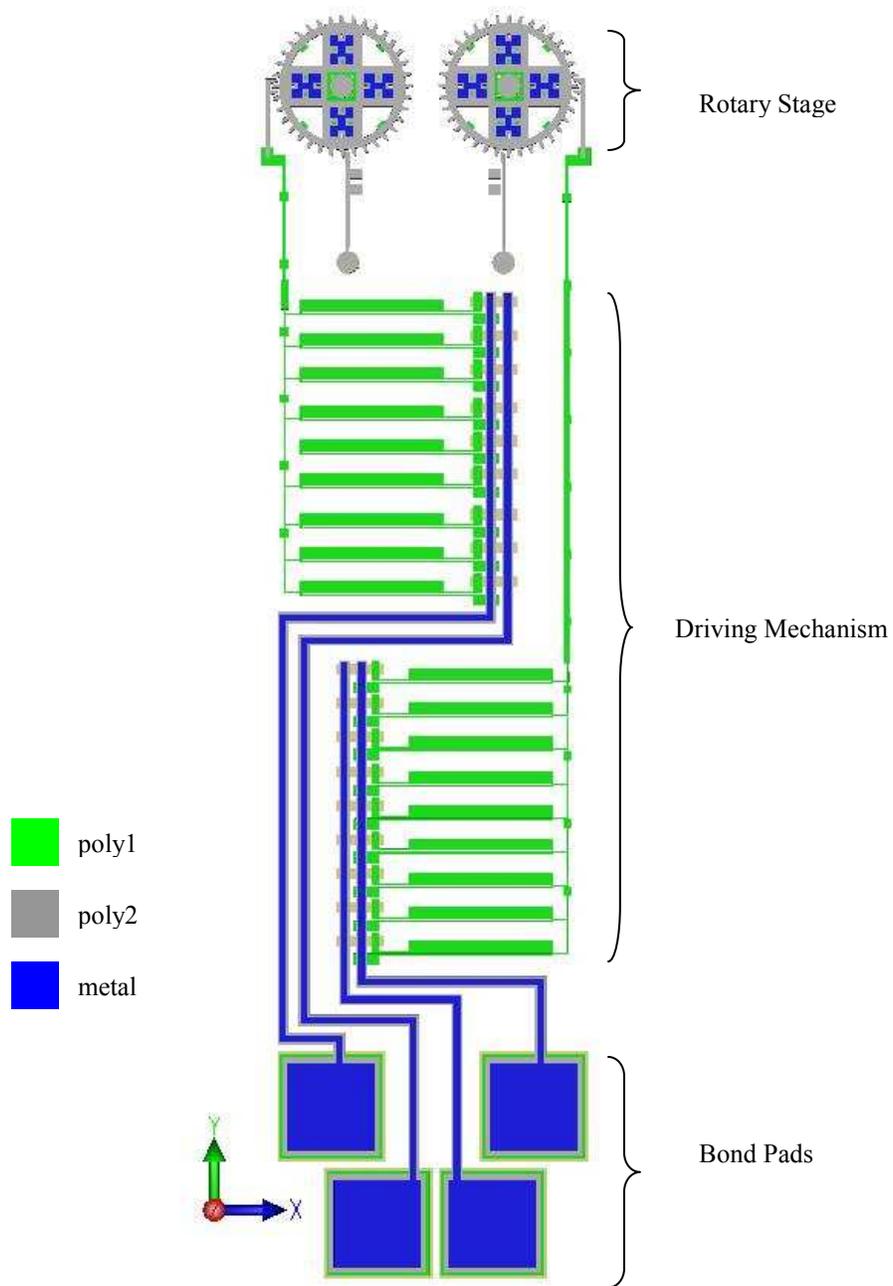
Figure 5.    Solid model of rotary stage assembly generated using CoventorWare.

## 2.2.    Rotary stage design

The rotary stage designed here is capable of complete 360° movement and includes a ratcheting arrangement to allow unidirectional rotation. Since the positioning system design was based on PolyMUMPs, an introduction to the PolyMUMPs process precedes the gear design description in the following sections.

### 2.2.1.  PolyMUMPs

MUMPs® (Multi-User MEMS Processes) is a commercial microfabrication foundry service offered by MEMSCAP Inc.[2], and PolyMUMPs (Polysilicon MUMPs) is a part of this service. PolyMUMPs is essentially a three-layer polysilicon surface micromachining process wherein layers of poly-Si serve as the structural material and phosphosilicate glass (PSG) is used as the sacrificial material. Electrical isolation from the silicon substrate is provided by a silicon nitride layer while metallization consists of 5000 Å thick Au layer with 200 Å thick chromium (Cr) adhesion layer. The various material layers and their corresponding thicknesses for PolyMUMPs are highlighted in Table 14 [19].

Besides the restrictions on allowed material layers, PolyMUMPs also requires designers to follow certain mandatory and directive design rules corresponding to the various design layers or masking levels (see Table 15). The various rules are summarized in Table 16 and Table 17. A more detailed description of the design guidelines can be

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[2] MEMSCAP Inc., 4021 Stirrup Creek Drive, Suite 120, Durham, NC 27703, USA.

found in the official PolyMUMPs design handbook [19]. Figure 6 is a snap-shot of the Process Editor file that was used to program CoventorWare 2003 for generation of the various positioning mechanism solid models. The process sequence shown in Figure 6 is merely representative of the PolyMUMPs fabrication steps and does not correspond to the actual processing conditions or methods employed in PolyMUMPs.

ProcessEditor: E:\vandana\Design_Files\PolyMUMPs\Devices\polymumps.proc

File   Edit   View   Help

| Step | Action | Type | Layer Name | Material | Thickness | | Color | Mask Name/ Polarity | | Depth | Offset | Sidewall Angle | Comment |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | Base | | Substrate | SILICON | 1.0 | | blue | GND | | | | | |
| 1 | Deposit | Conformal | SiN | SI3N4 | 0.6 | SCF | oran... | | | | | | |
| 2 | Deposit | Conformal | Poly0 | POLYSILICON | 0.5 | SCF | yellow | | | | | | |
| 3 | Etch | Front, Last Layer | | | | | cyan | poly0 | + | 0.5 | 0.0 | 0.0 | |
| 4 | Etch | Front, Last Layer | | | | | cyan | hole0 | - | 0.5 | 0.0 | 0.0 | |
| 5 | Deposit | Conformal | ox1 | PSG | 2.0 | SCF | white | | | | | | |
| 6 | Etch | Front, Last Layer | | | | | white | anchor1 | - | 2.0 | 0.0 | 0.0 | |
| 7 | Etch | Front, Partial | | | | | white | dimple | - | 0.75 | 0.0 | 0.0 | |
| 8 | Etch | Front, Last Layer | | | | | white | anchor2 | - | 2.0 | 0.0 | 0.0 | |
| 9 | Deposit | Planar | Poly1 | POLYSILICON | 2.0 | | green | | | | | | |
| 10 | Etch | Front, Last Layer | | | | | green | poly1 | + | 2.0 | 0.0 | 0.0 | |
| 11 | Etch | Front, Last Layer | | | | | green | hole1 | - | 2.0 | 0.0 | 0.0 | |
| 12 | Etch | Front, Last Layer | | | | | green | anchor2 | - | 2.0 | 0.0 | 0.0 | |
| 13 | Deposit | Conformal | Ox2 | PSG | 0.75 | SCF | blue | | | | | | |
| 14 | Etch | Front, Last Layer | | | | | blue | p12via | - | 0.75 | 0.0 | 0.0 | |
| 15 | Etch | Front, Last Layer | | | | | blue | anchor2 | - | 0.75 | 0.0 | 0.0 | |
| 16 | Deposit | Planar | Poly2 | POLYSILICON | 1.5 | | light... | | | | | | |
| 17 | Etch | Front, Last Layer | | | | | light... | poly2 | + | 1.5 | 0.0 | 0.0 | |
| 18 | Etch | Front, Last Layer | | | | | light... | hole2 | - | 1.5 | 0.0 | 0.0 | |
| 19 | Deposit | Stacked | Metal | GOLD | 0.5 | | gold | | | | | | |
| 20 | Etch | Front, Last Layer | | | | | gold | metal | + | 0.5 | 0.0 | 0.0 | |
| 21 | Etch | Front, Last Layer | | | | | gold | holem | - | 0.5 | 0.0 | 0.0 | |
| 22 | Sacrif... | | | PSG | | | | | | | | | |

Figure 6.        CoventorWare process editor file for PolyMUMPs process.

## 2.2.2.  Gear design

A gear is a toothed machine element that is used to transmit motion. The principal types of gears, based on the relative position of their axes of revolution are: spur, helical, double-helical, crossed helical, bevel, hypoid, and worm [22]. Spur gears have teeth that are parallel to the axes. The rotary stage for the RMA was designed as a spur gear and was based on the classic "rack and pinion" arrangement shown in Figure 7. The round gear is called a "pinion" and the flat gear, which is effectively a gear of infinite diameter, is called a "rack". This system is commonly used in the steering mechanism of vehicles. This arrangement was selected for the rotary stage because the actuation mechanism employed by the RMA delivers linear motion and "rack and pinion" can convert between linear and rotational motion.
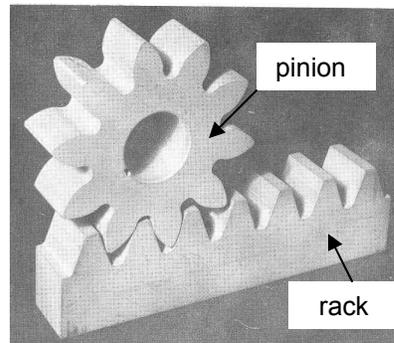


Figure 7.        Schematic of a classic "rack and pinion" gear arrangement. Adapted from [22].

## 2.2.2.1. Calculations

An important term to consider in gear design is the pitch circle (see Figure 8a) which, by definition, is the imaginary circle that rolls without slipping with a pitch circle

17

of a mating gear. In case of a rack gear, the corresponding term is known as the pitch line. The circular pitch (p) is defined as the distance along the pitch circle or pitch line between similar equally spaced tooth surfaces [23]. The circular pitch for the pinion (see Figure 8 (a)) can be calculated as follows:

$$p = (3.1416 * D) \div N \qquad (2.1)$$

where, D = diameter of pitch circle, and N = number of gear teeth.

The circular pitch of the rack (see Figure 8 (b)) and the pinion gears should be equal in order to properly mesh the gear teeth. Additionally, to facilitate smooth tooth engagement, the sum of the tooth thicknesses must be less than the circular pitch. However, it is not necessary for the tooth thicknesses of the mating gears to be equal [22].



(a)                                                    (b)
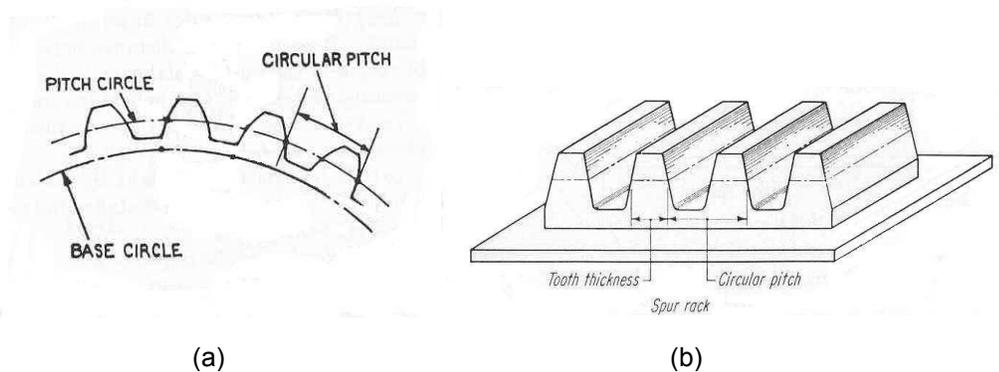
Figure 8.      Schematic diagram showing circular pitch for (a) pinion gear, and (b) rack gear. Adapted from [23].

The gear teeth for the rotary stage were designed in accordance with the above rules. Since the rotary stage fabricated earlier [18] was demonstrated to function satisfactorily, the gear diameter was not changed here. Figure 9 shows a perspective view of the 3-D solid model of the new gear.
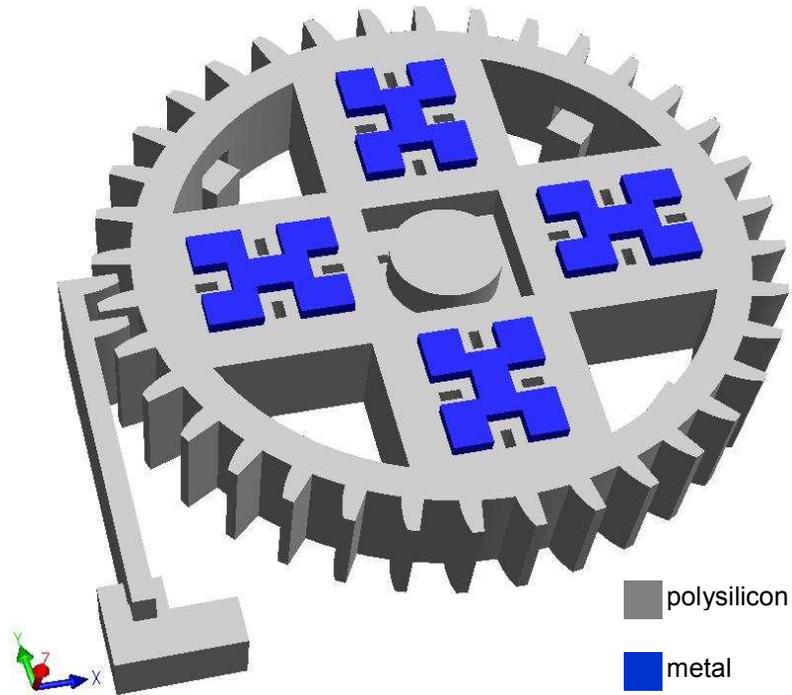
Figure 9.        Solid model of rotary stage gear.

The design specifications for the gear assembly are summarized in Table 3.

Table 3.        Design specifications for gear assembly.

| No. | Property | Value |
|---|---|---|
| 1 | Pinion gear diameter | 164 μm |
| 2 | Pitch circle diameter, D | 180 μm |
| 3 | Number of pinion teeth, $N_p$ | 36 |
| 4 | Circular pitch of pinion, p | 15.7 μm |
| 4 | Number of rack teeth, $N_r$ | 2 |
| 5 | Circular pitch of rack, p | 15.7 μm |
| 6 | Pinion tooth thickness, $T_p$ | 6 μm |
| 7 | Rack tooth thickness, $T_r$ | 6 μm |

2.2.2.2. Rotary stage mask layout


        The mask layout for the rotary stage is presented in Figure 10. This layout design

was done using the Layout Editor of CoventorWare. The various masking layers

19

corresponding to PolyMUMPs that form the structure of the gear are: poly1, hole1,

anchor1, dimple, poly1_poly2_via, poly2, metal, holem, and anchor2. Both rack and

pinion gears are designed using a special poly1 - poly2 stacked layer arrangement

suggested by PolyMUMPs for producing polysilicon structures made of poly1 and poly2.

This arrangement provides a thicker material stack (2.0 µm + 1.5 µm) for the gear body

which improves gear meshing and stiffens the rotary stage structure. However this is not

a guaranteed process. A description of the poly1-poly2 stacking process is given in

Appendix B.

A metallization area was designed on the spokes of the gear wheel for attaching

the bulk-micromachined mirrors. Dimples were placed on the inside periphery of the gear

wheel in order to eliminate stiction of the gear to the substrate after release.
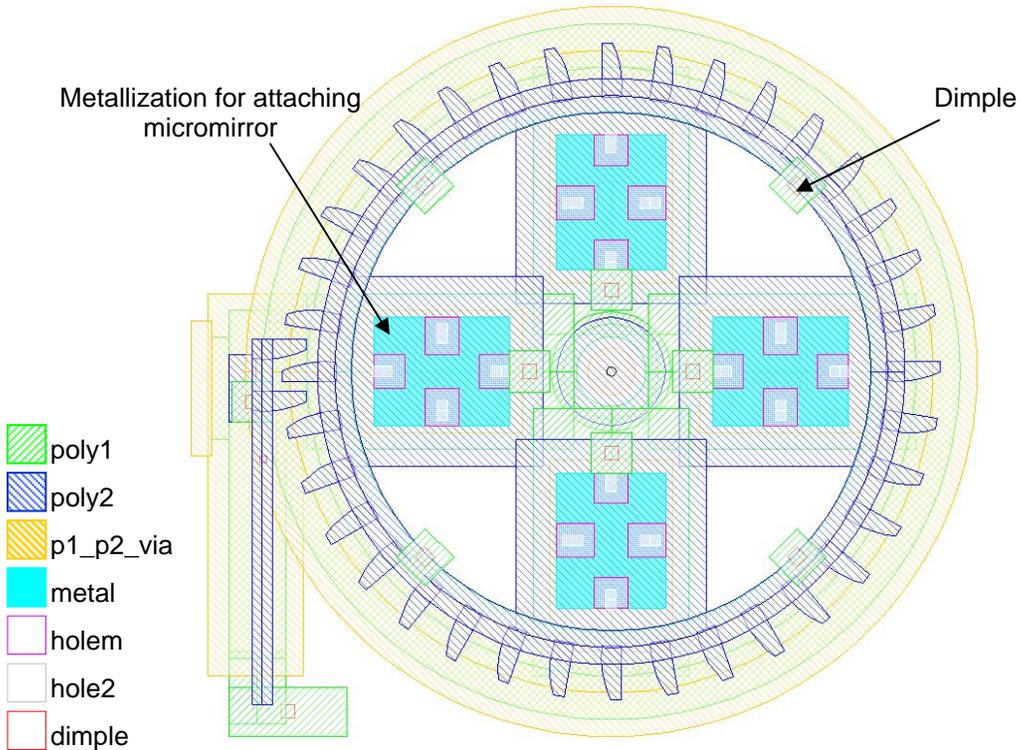


Figure 1.        Mask layout for rotary stage.

Design Rule Checking (DRC) of all the mask layouts was done using the Tanner
L-Edit software after completion of the initial drawing. This process was followed in
order to ensure adherence to the PolyMUMPs design rules. The L-Edit software was
preferred over CoventorWare for DRC because it allows checking of all design rules in a
single run and also facilitates zooming in to the exact error location. CoventorWare DRC,
on the other hand, permits the user to run only a single design rule at a time and does not
assist in precisely locating the error. DRC using CoventorWare can hence prove to be a
very tedious and inefficient process especially while checking layouts having high
density features.

### 2.2.3. Ratcheting arrangement

The rack and pinion system described above is intended to rotate the stage in a
clockwise direction; however, due to inertial effects it is possible that the stage will have
some motion in the counter-clockwise direction too, resulting in erroneous system states.
Therefore, to control accurate positioning of the gear stage, some mechanism for
enforcing unidirectional movement of the gears is essential.

The two designs commonly used in mechanical engineering to ensure
unidirectional movement of gears are: ratchet and pawl arrangement (positive drive) and
jamming ball arrangement (friction drive). Figure 11 presents a schematic illustration of a
typical ratcheting arrangement [24].
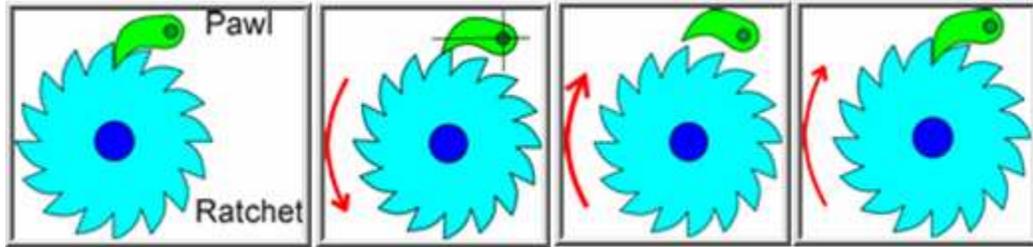
Figure 11.    Schematic of a typical ratcheting mechanism. Adapted from [24].

As shown in Figure 11, a pawl allows the ratchet wheel to rotate only in one (counter-clockwise in Figure) direction and jams rotation in the other (clockwise in Figure) direction hence prohibiting bi-directional rotation of the ratchet wheel. Figure 12 below is an example of a ratcheting mechanism as demonstrated by Danelle et al in a surface micromachined torsional ratcheting actuator device [25]. The ratchet here has been designed as a cantilever beam with restricted movement in one direction.
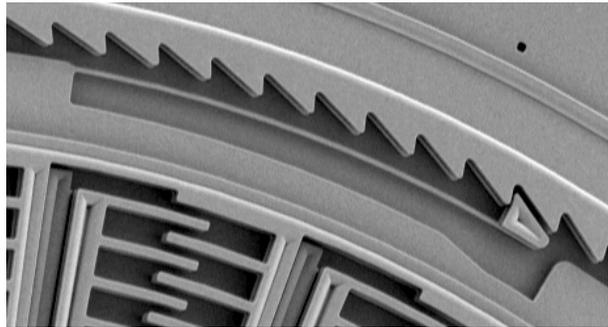


Figure 12.    SEM image of a ratcheting arrangement [25].

A similar ratcheting arrangement (refer to Figure 13), was utilized in the current rotary stage design. As shown in Figure 13, the pawl is basically a cantilever beam ending in a gear tooth shape with mechanical stoppers on one side of the beam. During clockwise rotation, the gear teeth push against the straight edge of the cantilever and bend the beam to allow for easy movement of the gear. Upon anti-clockwise rotation of the

22

gear, the toothed end of cantilever is pushed by the gear teeth. The anchored stoppers act against the cantilever movement and restrict the movement of the gears.
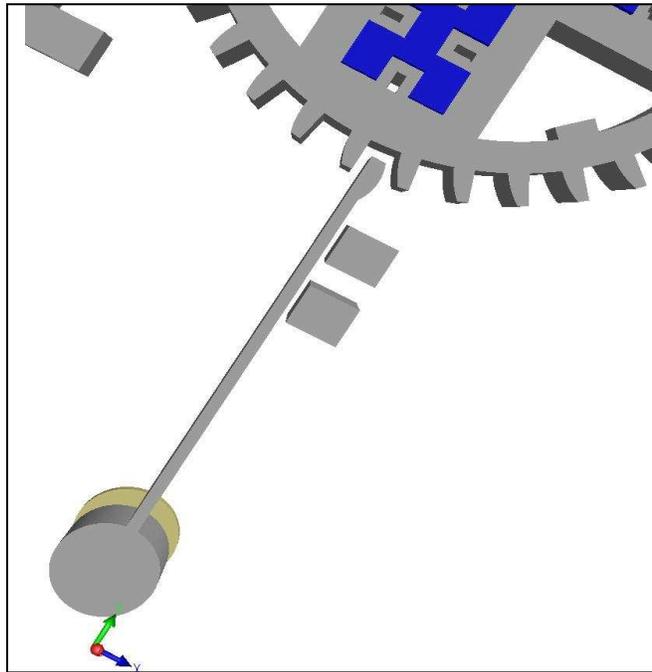


Figure 13.        Solid model of ratcheting arrangement used in the rotary stage design.

The ratcheting arrangement needs to be designed carefully to ensure its mechanical integrity. The design calculations carried out in this context are discussed herewith. The tip deflection $y$ of a simply supported cantilever beam, upon application of a point load P at the free end, is given by:

$$y = \frac{P \times L^3}{3EI} \qquad (2.2)$$

Where, P = point load at cantilever tip, L= length of cantilever beam, E= elastic modulus of beam and I = moment of inertia [26]. The point load P in the case of the ratcheting arrangement will be the force by which the rotary stage pushes the pawl.

The moment of inertia for a rectangular cantilever beam is given by,

$$I = \frac{wh^3}{12} \qquad (2.3)$$

where, w= width of cantilever, h= height of cantilever.

Substituting (2.3) into (2.2) we obtain the equation for L as:

$$L^3 = \frac{y.E.w.h^3}{4 \times P} \qquad (2.4)$$

The dimensions of the pawl cantilever were determined from equation 2.4. A similar approach to pawl cantilever design has been reported by Danelle et al [25]. For the calculations here, the cantilever height ($h$) was kept fixed at 3.5 μm (poly1 + poly2 thickness) and the elastic modulus of poly-Si ($E$) was taken as 160 GPa [27]. The overlap distance between the ratchet pawl and the next gear tooth was designed as 2 μm hence the value for deflection ($y$) was considered as 2 μm. The width ($w$) was arbitrarily chosen as 3.5 μm.

The applied point load at cantilever tip ($P$) was taken as 4 μN which was earlier determined as the force delivered by a single thermal actuator [18]. Arraying of thermal actuators increases the output force delivered, however the presence of friction and mirror loading effects are expected to reduce the force (4 μN) transferred from the rack gear to the pinion gear and finally to the pawl cantilever. In the absence of actual experimental values of force applied on the cantilever tip, the calculations for pawl design were carried out using a load of 4 μN. This value of load is expected to correspond to the minimum amount of force that will be seen by the pawl. By putting the above values in equation 2.4, the length of the cantilever beam *(L)* was found to be 144 μm.

## 2.3. Driving mechanism

All active MEMS devices employ some kind of actuating mechanism to function. The requisite features of the RMA actuation mechanism were identified as: low driving voltage, fast response, ease of design and fabrication, and high output force. Various actuating mechanisms like magnetic, electrostatic, thermal, magnetostatic and piezoelectric have been widely investigated and incorporated for actuating microstructures. The thermal actuation method was considered for the driving mechanism here as it has proved to be an attractive mechanism for micromechanical devices requiring high actuation forces, large deflections, good linearity and low actuation voltage [28].

### 2.3.1. Thermal actuators

Thermal actuators, also known as "electrothermal actuators", "heatuators" or "U-shaped thermal actuators", have been largely used in MEMS based devices to provide both in-plane and out-of-plane actuation [28]. Thermal actuators are also easily compatible with standard CMOS circuitry due to their low driving voltage. However, high power consumption remains a major drawback of the thermal actuation mechanism. Figure 14 schematically represents a basic thermal actuator design.
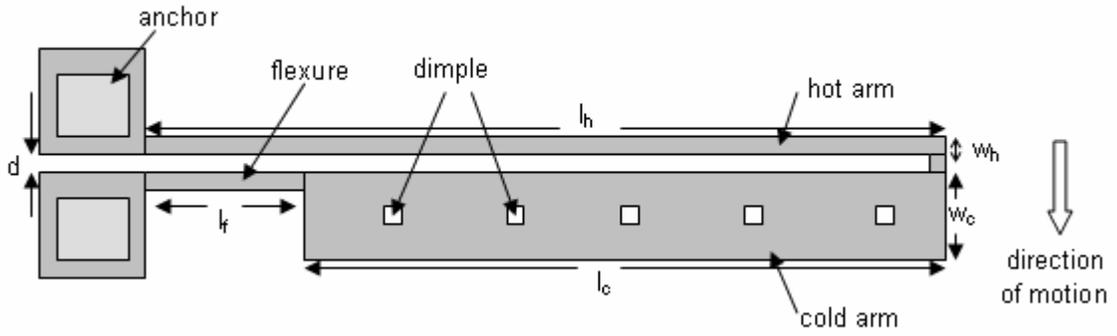
Figure 14. Basic thermal actuator design [29]. The dimensions are: d= 2.0 μm, $w_h$= 2.0 μm, $l_h$=240 μm, $l_f$= 40 μm, $l_c$= 200 μm, $w_c$=16 μm, width of flexure = 2 μm, and thickness of the device = 2 μm.

An electrothermal actuator works on the principle of thermoelastic expansion of materials induced by Joule heating. Any material with finite resistance (R) dissipates energy in the form of heat (Q) when electric current (I) is passed through that material. This phenomenon is referred to as Joule heating or resistive heating. The power loss (P) that causes this heat formation is expressed as:

$$P = I^2 \times R \qquad (2.5)$$

The resistance of a material depends on its length (L), area of cross-section (A), and resistivity (ρ) and is expressed as:

$$R = \frac{\rho \times L}{A} \qquad (2.6)$$

When current is passed through the arms of the thermal actuator, it causes differential heating of the two arms. The narrow arm, on account of its higher current density, undergoes a higher resistive heating and expands more than the wide arm. The asymmetrical expansion of the two arms which are mechanically coupled at one end and anchored to the substrate at the other end, results in an overall lateral deflection of the actuator tip in the direction of the cold arm. The deflection thus obtained is a function of

26

the temperature difference between the two arms, actuator geometry and actuator material properties [30]. It has been demonstrated by Bright et al [29] that forces delivered by individual thermal actuators can be combined by arraying of the actuators. The increase in generated force is linearly proportional to the number of actuators in the array. In view of above, an arrayed arrangement of thermal actuators was used to drive the rotary stage.

2.3.2. Modified thermal actuator

In order to utilize the thermal actuator for applications like micropositioning, it is of utmost importance that the actuator be reliable for its lifetime of operation. Hence, it is necessary to understand the failure modes of the device. In earlier reported reliability testing experiments on the classic thermal actuator design, it has been observed that the hot-arm of the actuator develops a high temperature region ("hot-spot") at its approximate center [31]. On application of high voltages , the temperature of the "hot-spot" can reach the melting point of poly-Si (~1600 K) resulting in device failure due to plastic deformation of poly-Si as shown in Figure 15. It has also been observed that development of high temperature, rather than high stress, is primarily responsible for the failure of thermal actuators in a given number of cycles of operation [31]. Thus the phenomenon of hot-spot formation can limit the usage of the actuator at higher voltages and adversely affect its lifetime, reliability and efficiency.

A possible solution to this problem would be increasing the width of the hot-arm but this will increase the surface area of the hot arm causing a reduction of the resistance of the hot-arm and ultimately a reduction in the amount of deflection obtained. However,

a selective increase of the arm width to cause sufficient heating without creating

concentration zones of high temperature could be another possible solution [33]. The

design presented here is based on the latter idea.
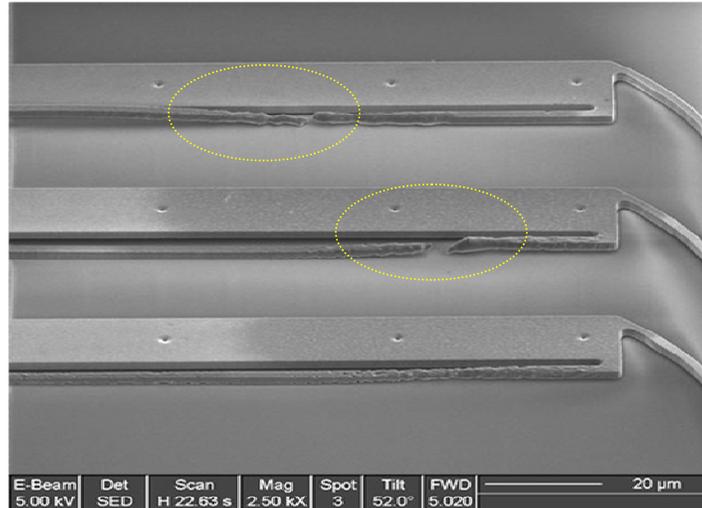


Figure 15.      SEM image showing thermal actuator burn-out upon application of high
voltage. Photo courtesy [32].

The modified design of the thermal actuator is shown in Figure 16 [34]. It can be

observed in the new design that the geometry of the hot arm has been modified to cause

an increase in the width of the hot arm at the approximate location of hot spot formation

while keeping the width of the adjacent areas smaller. This results in lesser heat

development and better conduction at what would otherwise be a "hot-spot". Hence in the

modified design, a more uniform temperature profile is obtained along the length of the

narrow arm as compared with the conventional design. As a result of the lowering of the

maximum temperature reached, more input energy can be applied to achieve a higher

deflection.
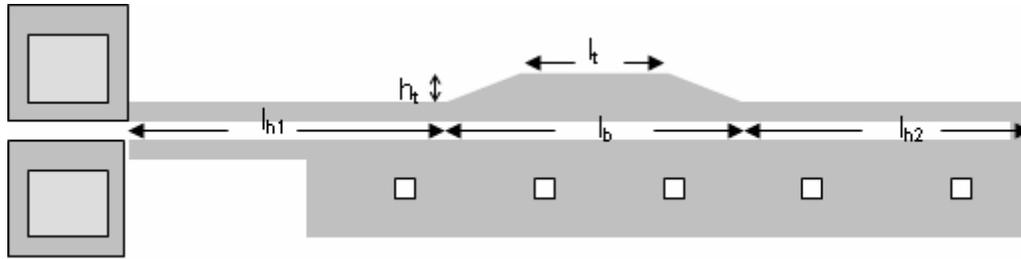
Figure 16.     Modified design of thermal actuator. The dimensions are: $l_t$= 28 μm, $h_t$= variable, $l_{h1}$= 88 μm, $l_{h2}$ = 102 μm, $l_b$= 50 μm, width of flexure = 2 μm. Rest of the dimensions remain unchanged vs. Figure 14.

The minimum dimensions of the actuator structures were chosen to conform to the design rules of PolyMUMPs. Dimples were placed all along the length of the wide arm and in the trapezoidal area of the hot arm in order to avoid stiction to the substrate during release of the fabricated device. The characteristics of the modified two-arm thermal actuator were next compared with the conventional thermal actuator. The effect of the geometry and location of the trapezoid on temperature and deflection of the modified thermal actuator were also investigated.

2.3.3.  Simulation results

The finite element analysis and coupled-physics simulation of the original and modified designs were carried out using the MemETherm module of CoventorWare[TM] 2003.1. The solid models of the actuator structure for the purpose of the simulations were generated using 2μm thick polycrystalline silicon (poly1) as the structural component. The material properties of poly-Si used in the analysis are presented in Table 4. These values agree with the material properties of poly-Si mentioned in standard reference [27].

29

Table 4.        Material properties of polysilicon.

| Property | Value | Units |
|----------|-------|-------|
| Density | 2.23 e-15 | kg/$\mu$m$^3$ |
| Thermal Conductivity | 1.0 e08 | pW/$\mu$m.K |
| Electrical Conductivity | 4.34 e10 | pS/ $\mu$m |
| TCE | 2.9 e-06 | 1/K |
| Poisson's Ratio ($\upsilon$) | 2.2 e-01 | - |
| Young's Modulus (E) | 1.69 e05 | MPa |

The solid models were meshed using the extruded bricks mesh and the partition quadrilateral meshing algorithm with an edge refinement index of 3. In the extruded bricks meshing technique, the area of interest is meshed in the X-Y direction using a suitable meshing algorithm and the mesh hence generated is extruded in the z-direction to form a complete three-dimensional meshed structure.

Past work on heat transfer mechanisms indicates that the thermal actuator loses heat to its surroundings primarily by conductive heat transfer [35]. Hence, heat loss via convection and radiation was not considered in this analysis. A fixed reference temperature of 300 K was applied to the anchors and the dimples as a thermal boundary condition to account for the conduction of heat. The application of this boundary condition assumes that the dimples on the thick arm assist in conductive heat transfer from the thick arm by contact with the underlying substrate. A dc input voltage ranging from 2V to 5V was applied at the anchors as the electrical boundary condition. The parametric study feature of CoventorWare$^{\text{TM}}$ 2003.1 was used to simulate the designs for this range of applied dc voltages. The simulations were carried out for incremental values of the variable $h_t$ (height of the trapezium structure above the hot arm). Simulations were

also done for the modified designs with various locations of the trapezium structure on

the hot arm of the modified thermal actuator.
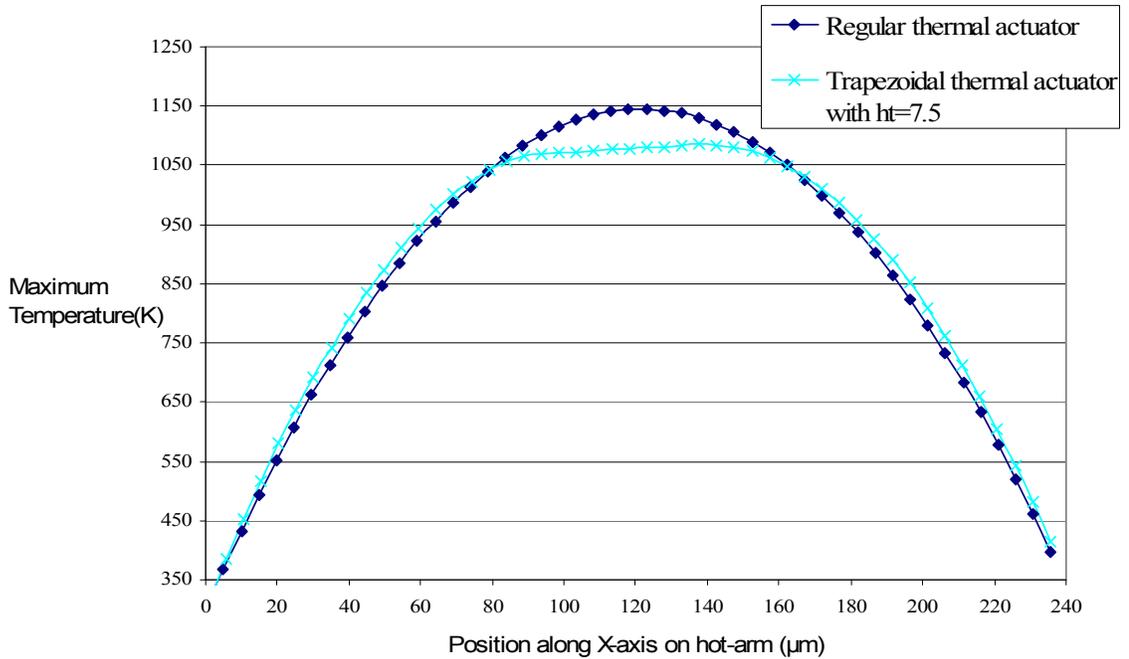


Figure 17.     Temperature distribution along hot-arm for regular and trapezoidal
thermal actuator at 5 V.

Figure 17 displays the temperature distribution along the hot arm, as a function of

position along the x-axis for the conventional design at an applied voltage of 5 V. It can

be seen that the location of hot spot formation (~1200 K) on the thin arm in the

conventional design of the thermal actuator is approximately at 120 μm from the

anchored end of the hot arm. Hence the trapezoid structure in the modified design was

placed around the location of this hot-spot. Figure 17 also shows the temperature profile

of the modified arm. It is clear from this figure that the temperature profile of the hot-arm

has significantly flattened in case of the modified design. Figure 18 and Figure 19

describe the variation of maximum temperature and maximum deflection as a function of the applied voltage for the regular and modified designs.
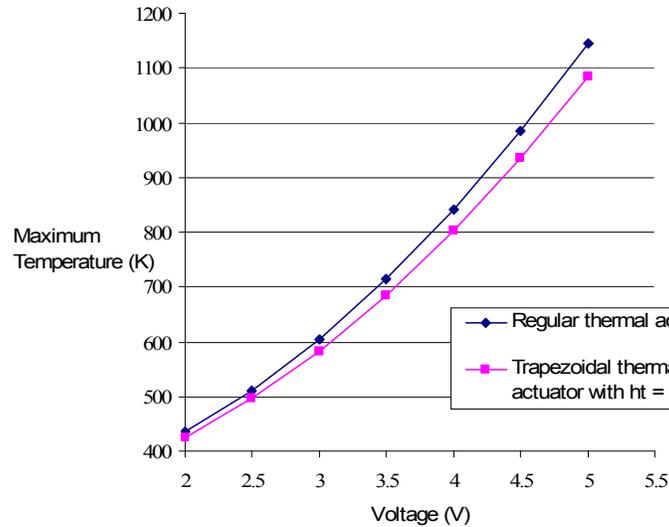


Figure 18. Plot of maximum temperature vs. applied voltage for regular and trapezoidal thermal actuator.

Figure 18 shows that the modified design reduces the maximum temperature at all voltages. Figure 19 shows that for the same applied voltage, the deflection obtained with the modified design is higher than that obtained with the regular design. Additionally, if the behavior of the two designs is compared by driving them to the same maximum temperature, then it is observed that the modified design increases the deflection by about 10-15%.
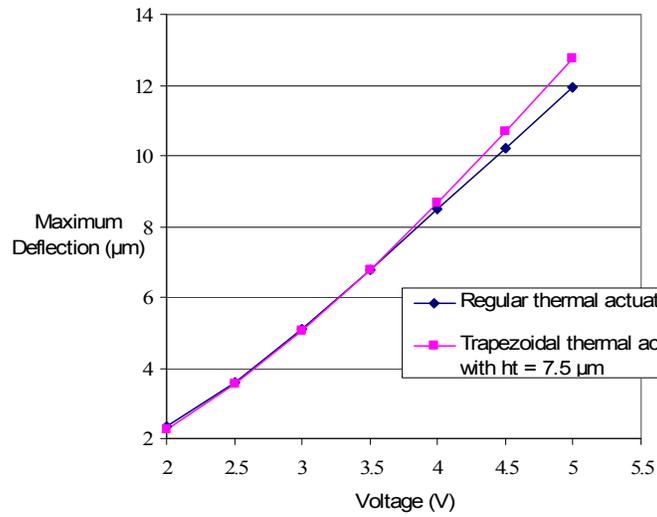
Figure 19.     Plot of maximum deflection obtained at various applied voltages for regular and trapezoidal thermal actuator.

Figure 20 presents the maximum temperature reached at various values of $h_t$ corresponding to the trapezoidal design for an applied voltage of 5V. Figure 21 shows the variation in deflection obtained by increasing the height $h_t$ of the trapezium at a fixed applied dc voltage of 5V.
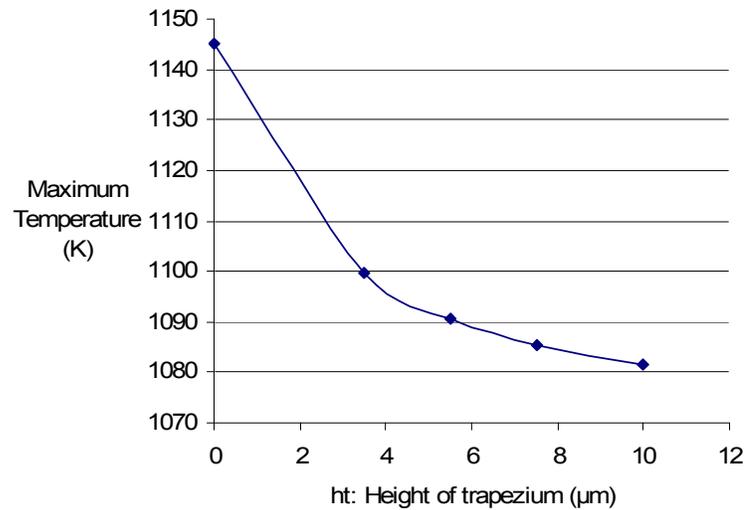


Figure 20.     Plot of maximum temperature vs. $h_t$, at 5Vfor trapezoidal thermal actuator.

33
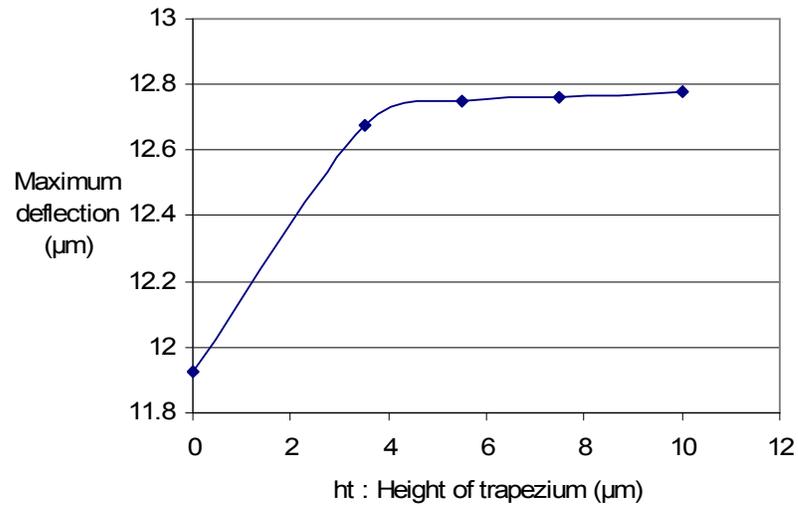
Figure 21.    Plot of maximum deflection vs. $h_t$ at 5 V for trapezoidal thermal actuator.

It can be observed from Figure 20 and Figure 21 that the slopes of the respective graphs are high at the outset and tend to reduce with an increase in $h_t$. It is also noted that as the total width of the hot-arm increases, overall power consumption of the device increases. This implies that an infinite increase in the height of the trapezoidal arm does not offer any significant advantage.

A study was done to find the most optimum location of the trapezium structure on the hot arm. For the purpose of this analysis, the dimensions of the trapezium on the hot arm were kept the same as described in Figure 16 ($h_t = 7.5\mu m$, $l_b = 50\mu m$, $l_t = 28\mu m$). However, the values of $l_{h1}$ and $l_{h2}$ were varied which effectively resulted in the shifting of the trapezium structure from one end of the hot arm to the other.

Figure 22 presents the variation in the maximum temperature as a function of the length $l_{h1}$. It can be seen in this figure that there is a negligible ($\sim 0.1$ K) variation in the maximum temperature as the location of the trapezium is shifted.

34
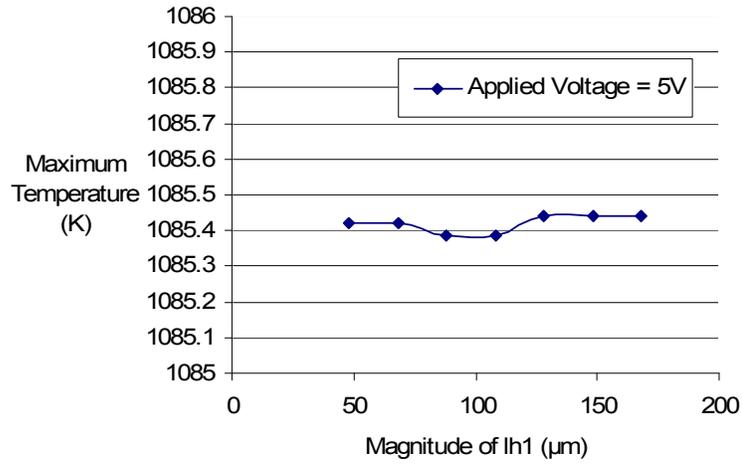
Figure 22.    Plot of maximum temperature vs. $l_{h1}$ at 5 V for trapezoidal thermal actuator.
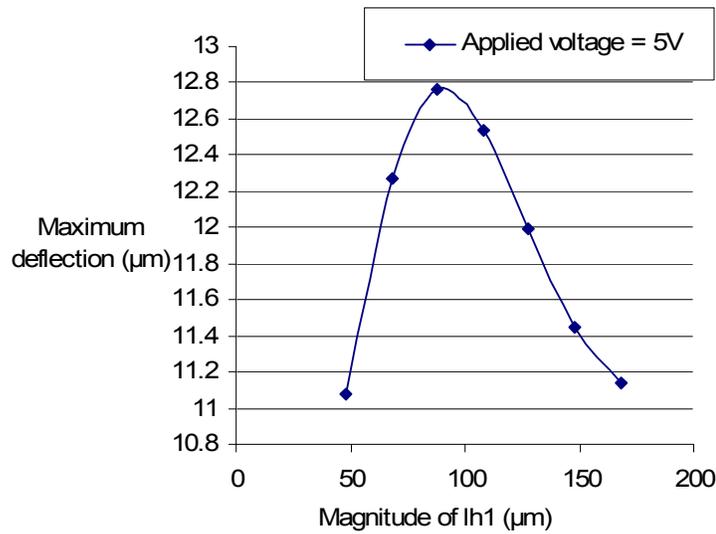


Figure 23.    Plot of maximum deflection vs. $l_{h1}$ at 5 V for trapezoidal thermal actuator.

Figure 23 above shows a plot of the maximum actuator tip deflection as a function of the length $l_{h1}$. It can be deduced from this figure that the deflection reduces by about 14% as the trapezium structure on the hot arm is shifted towards either the left or the

35

right of the location described in Figure 16. Hence it is important that the trapezoidal structure be placed approximately at the center of the hot arm in the modified electrothermal actuator.

The above results are obtained when it is ensured that the thick arm loses heat rapidly and is operated approximately at room temperature. Possible methods to achieve this are: including heat sink devices on or near the cold arm, ensuring the dimples on the cold arm contact the substrate, and mechanically coupling the thick arm to the device being actuated. However, further research is suggested to decide upon the most effective method for increasing the heat dissipation from the cold arm.

In previously reported work, an array of 9 thermal actuators was demonstrated to generate sufficient force to drive a rotary stage of dimensions similar to the one designed here [18]. Hence an array of nine thermal actuators was employed in the RMA driving mechanism after making the modifications suggested in the above discussion.

The design of the complete positioning mechanism was submitted for fabrication in PolyMUMPs foundry run #65. Figure 24 represents the layout of the micromirror positioning mechanism chip submitted to PolyMUMPs.
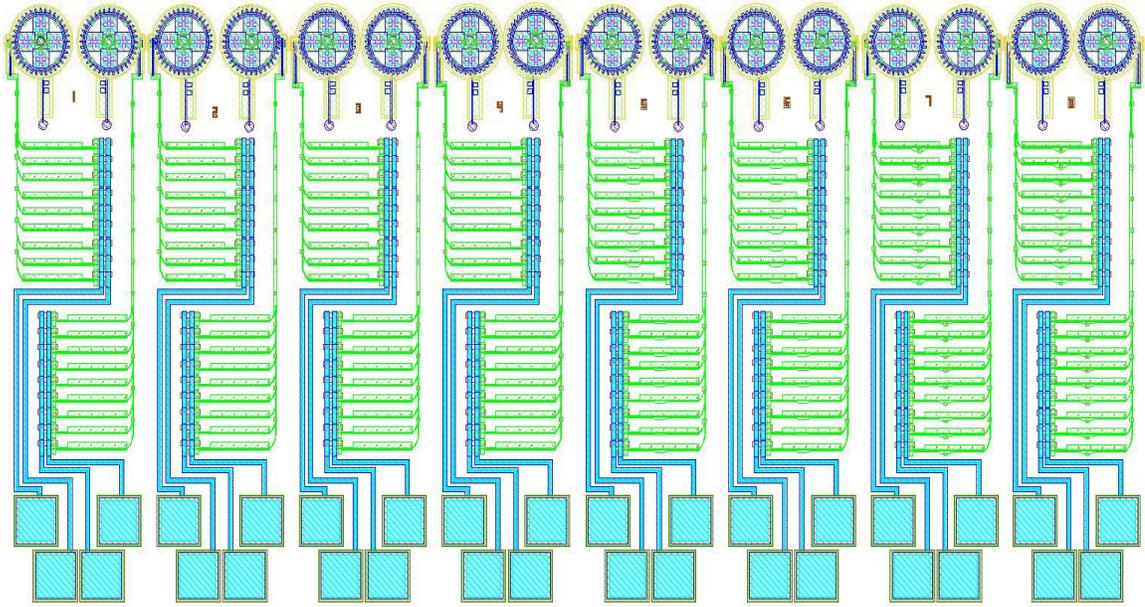
Figure 1.        Micromirror positioning mechanism chip layout.

poly0        poly1        poly2        p1_p2_via        metal

Figure 2 below shows the layout of a chip designed for testing the modified

thermal actuators. This chip was also included in the design submitted for PolyMUMPs

run.
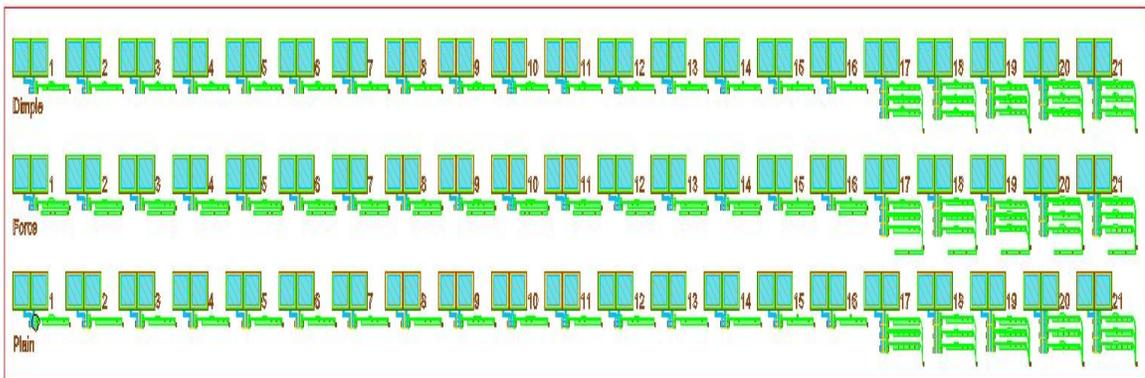


Figure 2.        Layout of thermal actuator chip sent for PolyMUMPs run 65.

poly0        poly1        poly2        p1_p2_via        metal

CHAPTER 3

DESIGN OF MICROMIRROR ARRAY

3.1.    Micromirror architecture

The micromirror positioning mechanism described in the previous chapter was designed for fabrication using a surface-micromachining process. The micromirror array, on the other hand, was designed for fabrication using bulk micromachining of silicon. Some of the advantages of considering this approach are:

i)      No release holes required on mirror surface, reducing optical losses.

ii)     No residual stress in the mirror mass, reducing insertion loss and cross-talk.

iii)    Batch fabrication of the entire assembly precluding usage of methods/parts required to raise the mirrors.

iv)     No stress prone hinge joints required for the structure, resulting in higher reliability of final device.

v)      Separate fabrication of micromirrors, allowing design of rotary stages capable of full 360 degree rotation leading to easier control of the positioning system.

The micromirror array design concept is presented in the following sections. The processing required for fabrication of the micromirror array is described in the next chapter.

### 3.1.1.  Initial design

The prime features desired in the micromirror design were:

i)      An out-of-plane tilted mirror surface with minimum surface roughness.

ii)      Parts for integrating micromirrors with the rotary stages.

Figure 26 shows different views of the 3-D model of the mirror that was conceptualized to satisfy the above requirements.
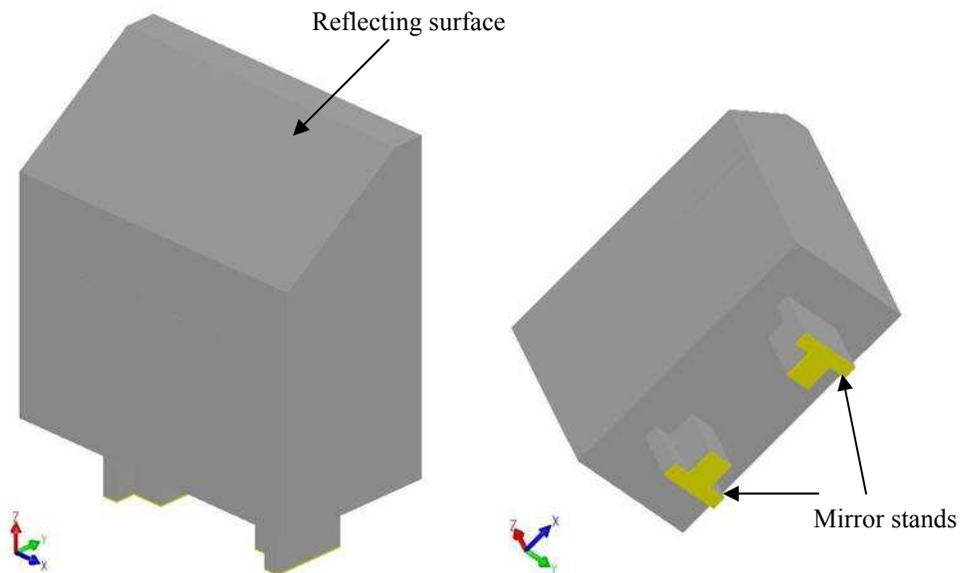


Figure 26.      Different views of the solid model of a single micromirror showing the mirror surface and the mirror stands.

The mirror reflecting surface was designed to be tilted because this arrangement ensures a wider scan angle and consequently less stringent location specifications of the auxiliary

components of the microspectrometer. The other criteria used for designing the micromirror were: maximum reflecting area, large surface area for bonding, minimum structural mass, and clearance space for the gear hub.

A tilted surface can be formed by the [111] plane exposed by wet anisotropic etching of (100) silicon. It has been reported earlier that the (111) surface can be used to form mirror surfaces [36]. Hence, anisotropic etching method was selected for defining the mirror surface. In anisotropic etching, certain planes of crystalline silicon are etched preferentially over the other planes. The etch rate of [111] planes of silicon is much less than the other planes, hence this plane gets exposed upon anisotropic etching. The angle formed by the [111] plane with the substrate plane depends upon the mask design and the crystallographic orientation of the substrate. As shown in Figure 27, an angle of 54.7° is formed when the etch mask opening is aligned parallel to the {110} direction of a (100) silicon wafer.
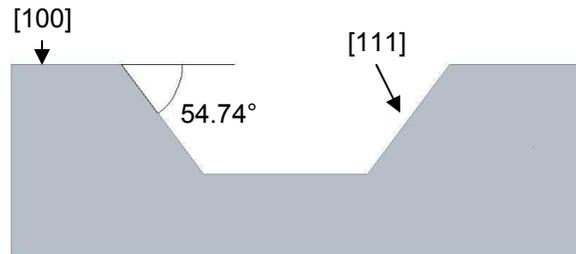


Figure 27.        V-groove sidewall angle in Si (100).

The micromirror stands shown in Figure 26 are required to provide bonding areas when integrating the micromirror with the rotary stage. This feature can be fabricated by a few cycles of the Deep Reactive Ion Etching (DRIE) process. The basic shape of each micromirror is also 'cut out' of the KOH patterned silicon using through-wafer DRIE etching. DRIE is a dry anisotropic etching technique that does not depend upon the

crystal orientation of the substrate being etched. This technique is generally used in

MEMS to fabricate very high aspect ratio silicon microstructures. In the DRIE Bosch

process, alternating cycles of polymer passivation (using $C_4F_8$) and etching (using $SF_6$)

are utilized along with a high density inductively coupled plasma source to allow etching

of structures with vertical or near-vertical sidewalls ($90 \pm 2°$) for features having aspect

ratios up to 30:1. Photoresist (selectivity 50:1), silicon dioxide (selectivity 150:1) and

aluminum (selectivity 300:1) work as very good masking materials for DRIE etching of

silicon [37].

After establishing the key etching techniques, the various edge lengths of the

mirror were determined based on the mirror design criteria, rotary stage geometry and

anisotropic etching characteristics of silicon. Figure 28 describes the various edge lengths

of the basic mirror structure.
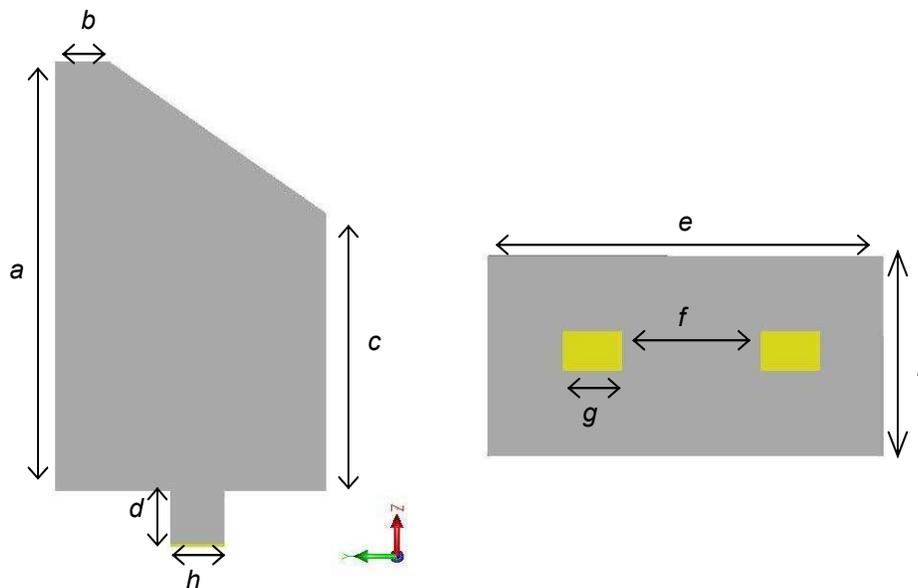


Figure 28.    Edge lengths of basic model of micromirror: $a$ = 346 μm, $b$ = 20 μm, $c$ = 166 μm, $d$ = 4 μm, $e$ = 200 μm, $f$ = 70 μm, $g$ = 30 μm, h = 20 μm, i = 100 μm.

The height of the micromirror stands ($d$) was decided as 4 μm in order to leave a gap of several microns over the "cap" located in the center of the rotary stage. This "cap" is required to keep the rotary stage wheel from flying off upon release. In theory, $d$ can be increased to a height of $d + c$ thereby resulting in reduction of the redundant mass of the micromirror. However, in practice, this is difficult to achieve since performing lithography operations on a surface having features that are tens of microns in height proves to be very challenging.

### 3.1.2. Modified design

It was observed that with the dimensions shown in Figure 28, upon rotation of the mirrors about their geometric center, at a particular point a clearance of only 4 μm existed between adjacent mirrors. The spacing between the rotary stage wheel and the anchor used to support the gear wheel is 3 μm (a specification set by PolyMUMPs design rules) and this clearance can reduce during rotation. Considering that when adjacent gears move 3 μm simultaneously, a high probability of collision of the adjacent mirrors exists. Figure 29 illustrates the described situation as simulated using the "Rotation" feature of the Layout Editor of CoventorWare$^{\text{TM}}$ 2003.
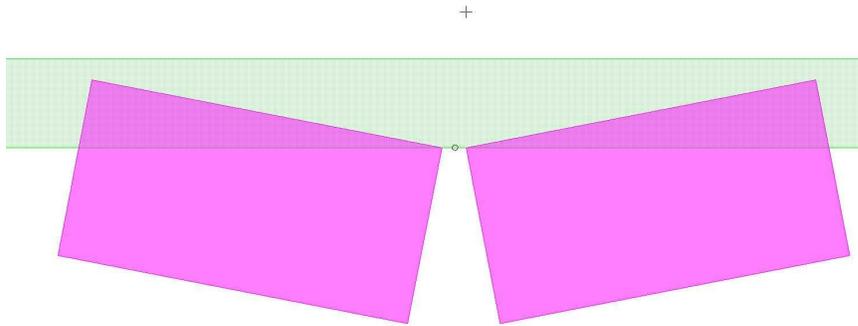
Figure 29.     Schematic of mirror collision situation.

In order to ensure that there is no collision of the mirrors in any rotational position, geometry of the micromirror was modified to a polygon as shown in Figure 30 (b). The design shown in Figure 30 (b) has a pitch ($M_p$) of 230 μm with 30 μm spacing between adjacent mirrors. This spacing reduces the fill-factor of the mirror array. The linear fill-factor for a micromirror array is expressed as [38]:

$$\text{Linear fill-factor} = \frac{M_w}{M_p} \qquad (3.1)$$

where, $M_w$ = width of a single micromirror, and

$M_p$ = micromirror array pitch.

The fill-factor is an important parameter to consider especially when designing micromirrors for a spectrometer. A lower fill-factor can influence the efficiency of a microspectrometer as wavelengths lying in the "dead region" will be undetected by the device. The fill factor for the mirror design shown in Figure 30 (b) is 86.9 %.

The basic design as shown in Figure 28 can be also positioned in a staggered fashion such that no wavelength escapes and fill-factor of the mirror array effectively

43

increases. However, such positioning will require very precise control of the individual gear drive mechanism.
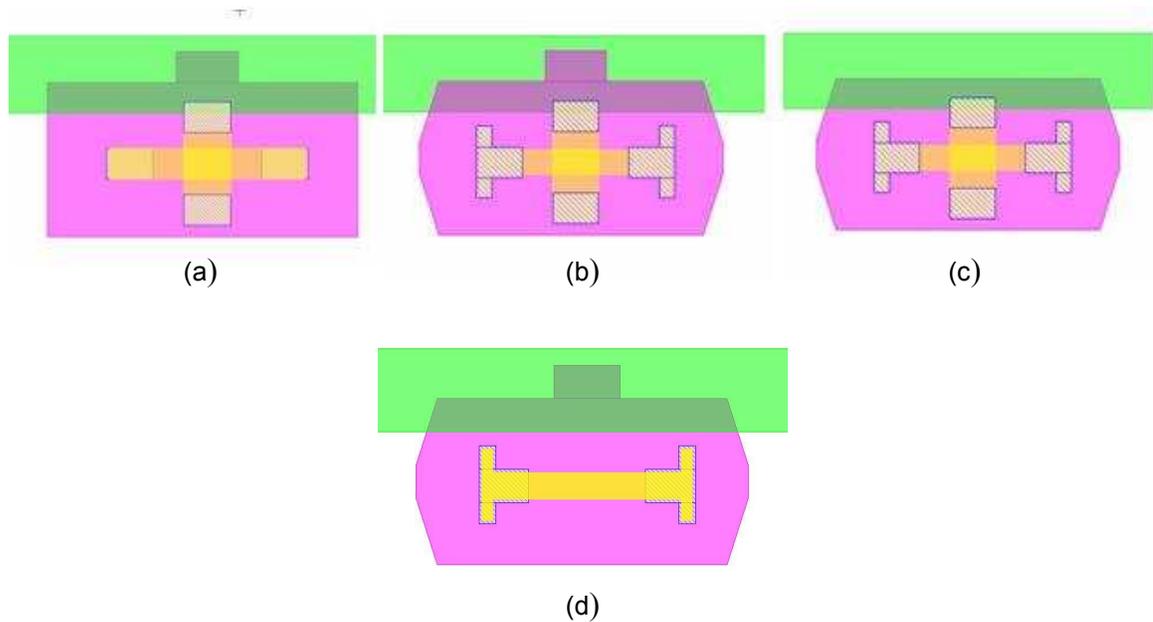


Figure 30. Various modifications of the basic mirror design.

As the micromirror stand shown in Figure 26 needs to bond to the metal layer on the gear stage, a greater surface area of the stand can be expected to produce better bonding quality and eventually better mechanical stability of the RMA. Hence another pair of stands perpendicular to the initial ones was added to the bottom of the mirror. The layout for the mirror designed with this modification is displayed in Figure 30 (b).

In order to integrate the micromirror array with the rotary stage on a wafer scale, it is important that the micromirror chip be temporarily bonded on the top side to a handle wafer (see Figure 31 a). Once the micromirror is permanently bonded to the rotary stage (see Figure 31 b), the handle wafer can be removed (see Figure 31 c).
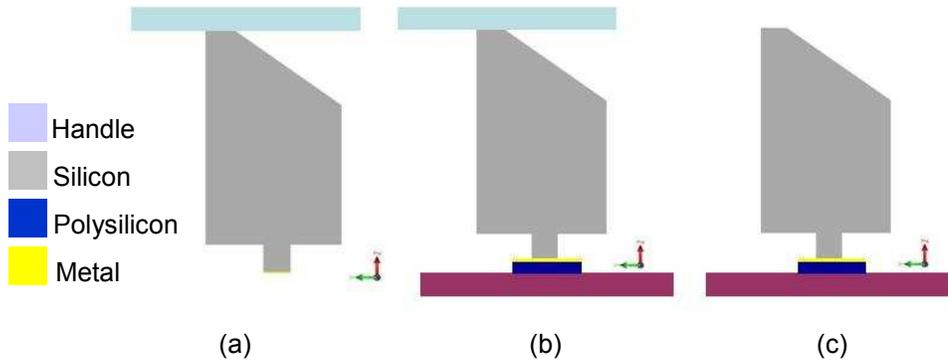
Figure 31.    Schematic representing transfer of micromirror to PolyMUMPs substrate. (a) a handle wafer is bonded to the micromirror, (b) the micromirror chip is bonded to the surface-micromachined rotary stage, and finally (c) the handle wafer is released.

An additional area was therefore included on the top of the micromirror structure to bond to the handle wafer. A design goal in this research was to maximize the mirror reflecting area and reduce the dimensions of any additional required areas to the minimum possible in order to reduce the total mass of the micromirrors. However it was suspected that a reduction in the top bonding area might result in peel-off of the mirror structure before or during the permanent bonding step. Hence the top bonding region was modified (see Figure 30 (c)) such that the overall width of the region was reduced and an extension structure measuring 40 μm X 30 μm was added to increase the total bonded surface area available. Figure 30 (a), (b), (c), and (d) represent the various modifications of the basic design.

3.2.    Process flow

The proposed process flow design for fabrication of the micromirror array is discussed below. A schematic illustration of the process flow is presented in Figure 32. A detailed description of each process step is given in Chapter 4.

i)    Deposit LPCVD silicon nitride on a 350 µm thick, double side polished (DSP), n-type, high resistivity (1-20 Ω-cm), Si (100) wafer (Figure 32 a).

ii)   Pattern photoresist on the front-side of the wafer with the "KOH" mask.

iii)  Etch openings in nitride with Reactive Ion Etching (RIE) (Figure 32 b).

iv)   Anisotropically etch the wafer to obtain 180 µm deep V-grooves (Figure 32.c).

v)    Pattern photoresist on the wafer backside using the "Indent" mask. Use backside alignment for aligning the V-grooves with the Indent features

vi)   Etch the backside nitride in RIE to open up windows for dry etching (Figure 32 d).

vii)  Etch exposed silicon on wafer backside by 4 µm using DRIE.

viii) Bond wafer front-side with a "handle" wafer.

ix)   Blanket etch nitride on wafer backside in RIE for 2 min (Figure 32.e)

x)    Sputter 200 Å Cr followed by 5000 Å Au on the backside of the wafer [3] (Figure 32 f).

xi)   Pattern photoresist on the wafer backside using the "Metal" masking layer.

xii)  Etch the Au and Cr on wafer backside (Figure 32 g).

xiii) Deposit oxide on the wafer backside. This oxide layer will act as a masking layer for the deep dry etching step discussed ahead (Figure 32 h).

xiv)  Pattern photoresist on the wafer backside using the "DRIE" mask.

xv)   Etch oxide on wafer backside to open windows for DRIE (Figure 32 i).

xvi)  DRIE etch through wafer to form the micromirror structures (Figure 32 j).

---

[3] The thicknesses of the Cr and Au layers mentioned here were arrived at by experimentation discussed later in this section.

xvii)    Blanket etch oxide used as masking layer for DRIE.

xviii)    Dice the individual mirror array chips (Figure 32 k).

xix)    Bond micromirror array chip with PolyMUMPs rotary gear stage chip (Figure 32 l).

xx)    Release "handle wafer" and PolyMUMPs gear stages by immersing in 49% HF solution for 2 minutes (Figure 32 m).

a)

b)

c)

d)

e)

f)

g)

h)

i)

j)

k)

l)

m)

| | Silicon | | Nitride | | PR | | Cr/Au | | Pyrex | | Oxide | | Polysilicon |
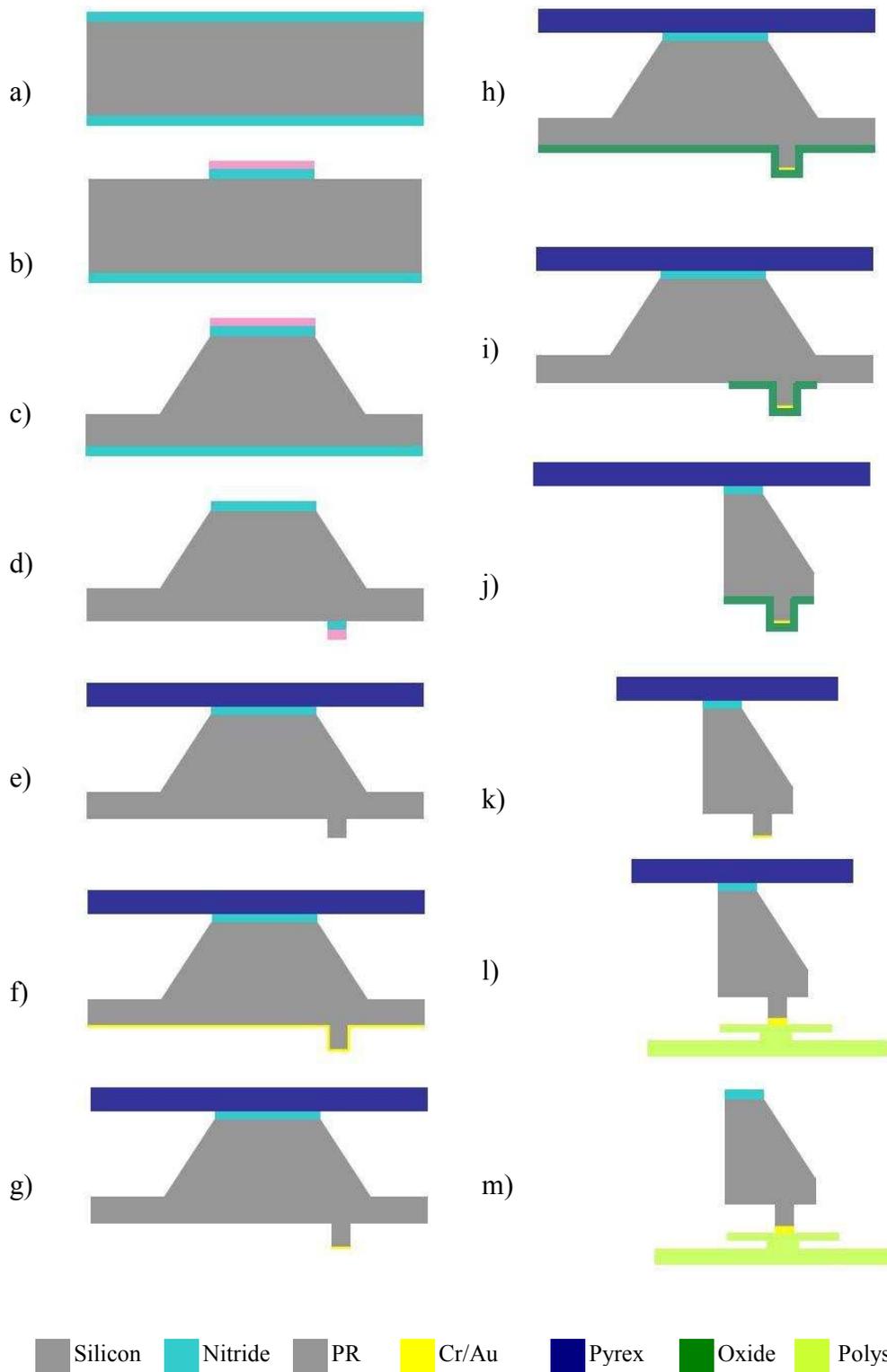
Figure 32.     Schematic illustration of the micromirror array fabrication process.

## 3.3. Micromirror array mask layout

The mask layout for the micromirror was done using CoventorWare Layout Editor. The initial layout was done in a quad fashion where all the masking layers were initially drawn on an area corresponding to a quarter of a 100 mm wafer surface. These layers were then separated digitally using Boolean operations to cover the entire wafer surface. By this method, a single mask plate could be used for all the masking layers thereby reducing the prototyping cost. Figure 33 shows the final master mask design.
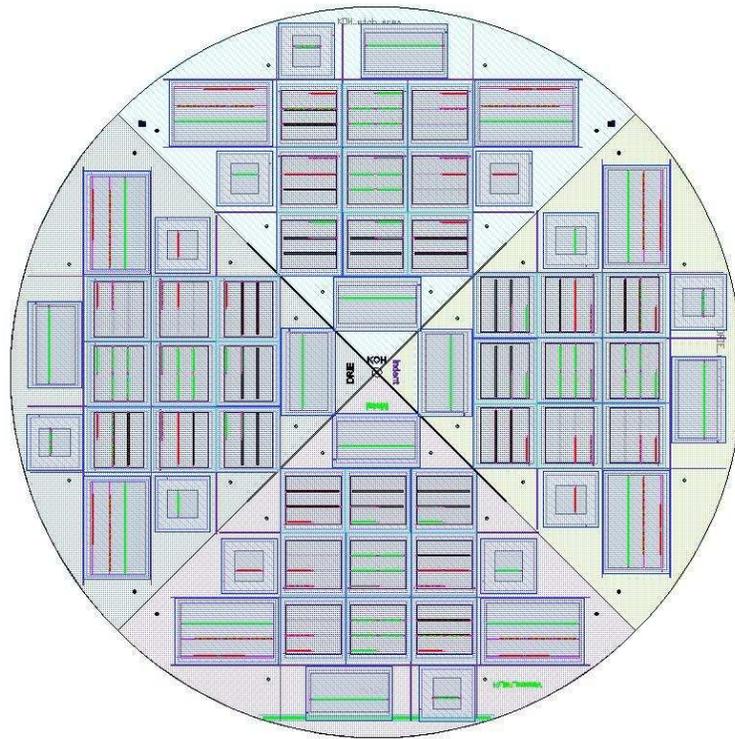


Figure 33.     Mask design for micromirror array fabrication.

Figure 34 (a) shows the mask layout for the "KOH" etch pattern followed by the backside etch mask for the "Indentation" in Figure 34 (b), the "Metal" layer in Figure

34(c), and finally the "DRIE" etch through mask in Figure 34 (d). Figure 34 (e) is a

schematic representation of all the masking layers superimposed together.



(a)

(b)

(c)

(d)

(e)
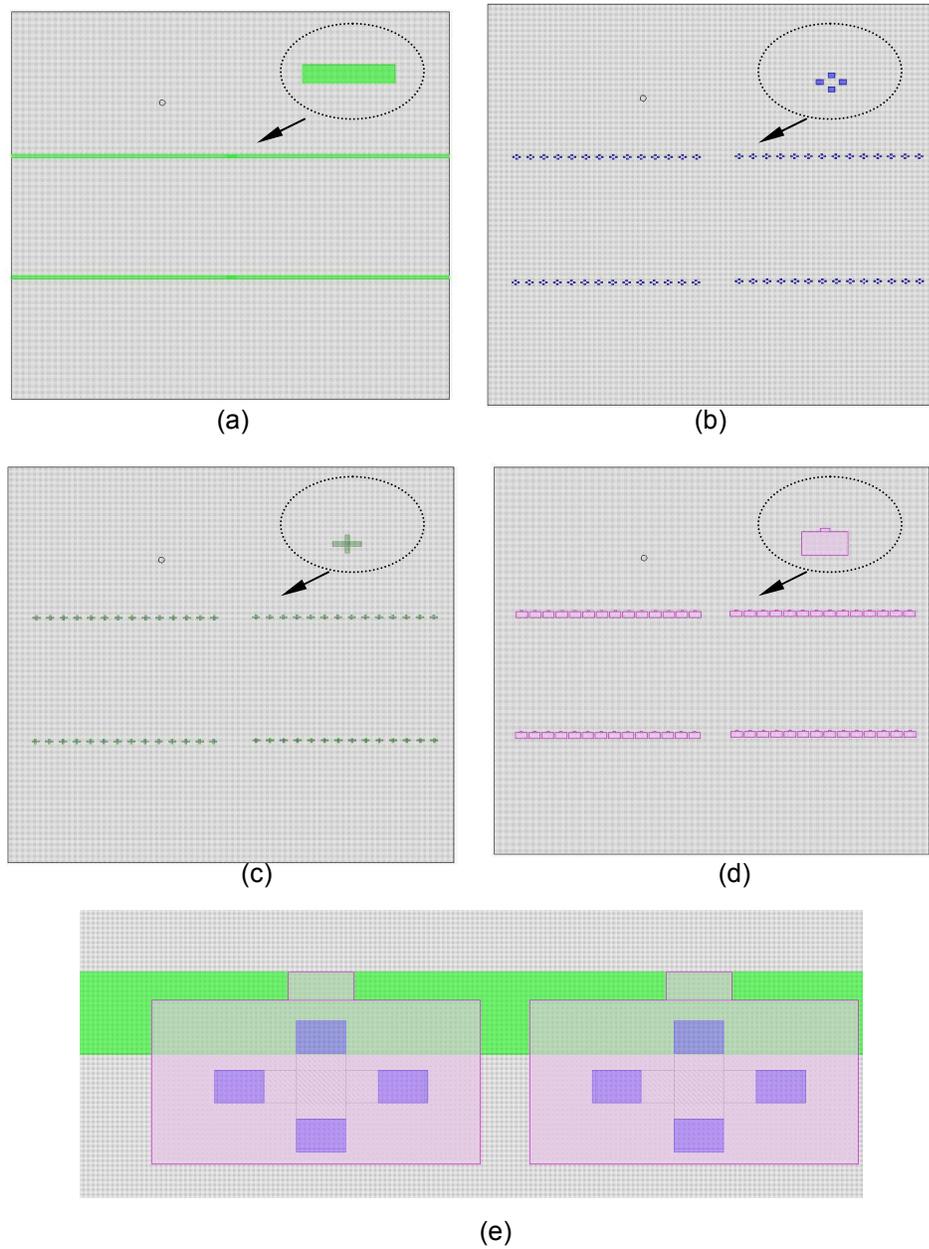
Figure 34.  Various layouts for micromirror array showing (a) "KOH" mask design, (b) "Indent" mask design, (c) "Metal" mask design, (d) "DRIE" mask design, and (e) layout of all masks superimposed together.

Figure 35 below shows the various alignment marks included on the master mask for aligning the different layers during the photolithography steps.



(a)        (b)        (c)        (d)
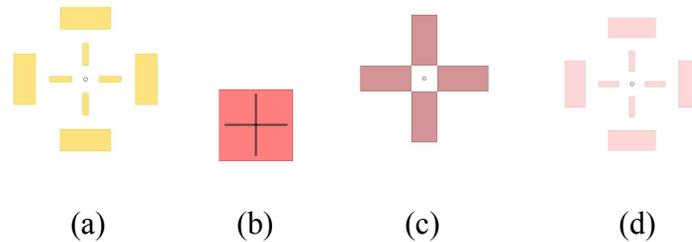
Figure 35.     Various alignment marks on mask for (a) present on "KOH" mask for front to back alignment of "KOH" mask with "Indent" mask, (b) present of "Indent" mask, (c) present on "Metal" mask, and (d) present on "DRIE" mask.

Three sets of chip sizes measuring 14 mm X 8.5 mm, 7.5 mm X 7.5 mm, 7.5 mm X 12 mm, 8.5 mm X 8.5 mm were designed in the mask. These chip sizes were chosen to correspond to the PolyMUMPs chip sizes and were designed considering the fact that a minimum chip dimension of 1 cm. sq. is required by the chip bonding tool used in this research. In addition to the above, thin rectangular streets were included in the "Indent" layer to work as visual aids for demarcating individual chips during dicing alignment.

The master mask hence designed was later replicated onto iron oxide photoplates to make working copies of the various design layers. This process was carried out to ensure longevity of the master mask. The process followed for replicating the chrome mask on the iron oxide photoplate is given in Table 13.

3.4.    Integration methods

Bonding techniques are implemented at two different stages in the micromirror fabrication process described above. In MEMS technology, the available bonding

51

methods are commonly classified into three categories: (a) direct bonding, (b) anodic bonding, and (c) intermediate layer bonding. Indirect bonding involves usage of an intermediate material layer (metal films, polymers, solders, etc.) to bond two components while direct bonding does not use any intermediate materials and relies on application of high temperature (800 – 1200 °C) to produce fusion bonding of similar materials [39]. The above two methods of bonding are further classified into various categories based on the type of material used as bonding agent and processes involved in bond formation.

Both wafer scale (Section 3.2 step viii) and chip scale (Section 3.2 step xviii) bonding need to be carried out at different stages in the micromirror process flow. The particular requirements of the bonding steps and the processes best suited to them are discussed below.

## 3.4.1. Wafer-level bonding

In the micromirror fabrication process, a 'handle' wafer is required to support the device wafer during the deep DRIE step and hold the etched devices in place during the dicing and chip level bonding steps. In addition, a handle wafer is also essential for avoiding helium leak during the DRIE process. Due to the presence of deep etched features on the reverse side of the wafer, a high probability of helium leakage exists in which case the computer controlled DRIE process does not proceed further. Helium is required for uniform thermal conduction of heat from the substrate since presence of local high temperatures results in uneven etch profiles in DRIE. The bonding of such handle wafer with device wafer will obviously require a wafer level bonding process.

Since, the handle wafer is required to be released after the transfer of the micromirror array on to the rotary stages (see Figure 31 c); it is pertinent that the wafer-level bond of the handle wafer with the silicon wafer should be of a temporary nature. This implies that it should be easy to de-bond the handle wafer from the silicon wafer by means of wet or dry etching techniques. The method of transfer of micromirror chip on to the rotary stage chip might require a high temperature process. The temporary bond material should therefore be capable of enduring the elevated permanent bonding temperatures.

As direct bonding forms very strong bonds that are not easy to break, indirect bonding is more suitable for this process. Adhesive bonding is an attractive option given the presence of the above constraints. It is a low temperature process and can be used to join a wide variety of materials. Waxes, photoresist, solder, glass frit, and polymer adhesives are some of the commonly used intermediate materials for temporary bonding in MEMS fabrication [40].

Photoresist and polymer adhesives are not easily removable once subjected to high temperature processes. The temporary bonding agent required here needs to be such that it is possible to uniformly coat it on a substrate. This is required because during the process of bonding the micromirror chip on the rotary stage chip it is important that both chips be aligned properly. A non-uniform thickness of the intermediate bonding layer between the handle wafer and the device wafer could result in non-uniform levels of the mirror structures. In addition to the possibility of introducing misalignment, the non-uniform levels of the mirrors would also cause non-uniform distribution of bonding pressure on the mirrors, which will eventually affect the bond quality. An investigation of

possible bonding techniques was done to find the most suitable process for our purpose. Experiments for the wafer scale bonding step were conducted using the EVG 501 Universal Bonder tool.

### 3.4.1.1. PiRLIII bonding

In view of the above issues, a specialty material PiRLIII was considered for the temporary bonding step. PiRL®III is a polyimide manufactured by Brewer Science, Inc. especially as a high temperature release layer and lift-off layer. PiRLIII is highly resistant to acid etchants, organic solvents and high temperatures. In addition, it has the distinctive property of maintaining solubility in positive resist developers after being subjected to imidization bakes at temperatures up to 400° C. PiRLIII can be evenly deposited on a substrate by means of a regular spinner and gives thickness range of 0.8 μm to 10 μm [41].

In order to determine the parameters for a strong and void-free bonding of substrates using PiRLIII as an intermediate layer, a set of experiments were conducted. In these experiments, a 400 μm thick, 100 mm silicon wafer patterned with 100 μm deep V-grooves formed by anisotropic wet etching was bonded to a 400 μm thick, 100mm Pyrex wafer under various temperature and pressure conditions. A Pyrex wafer was used for convenient visual inspection of the bond quality.

From the experiments hence performed, the following procedure of wafer preparation was found to produce the best result for a void-free and strong PiRL bonding:

i)         Spin Adhesion promoter APX-K1 on the patterned Si wafer at 4000 rpm for 30 sec.

ii)       Soft bake Si wafer at 90° C for 60 seconds on a hotplate.

iii)      Spin APX-K1on the Pyrex wafer at 4000 rpm for 30 sec.

iv)      Soft bake Pyrex wafer at 90° C for 60 seconds on a hotplate.

v)       Spin PiRLIII on Pyrex wafer at 4000 rpm for 30 sec.

vi)      Soft bake Pyrex wafer at 90° C for 60 seconds on a hotplate.

vii)     Stack the Pyrex and silicon wafers and roughly align along the flats.

After completion of the above process, wafer to wafer thermocompression bonding was performed in the following process conditions:

i)        Temperature: 200 °C, Force: 250 N, Bonding time: 10 min.

ii)      Temperature: 150 °C, Force: 250 N, Bonding time: 10 min.

iii)     Temperature: 150 °C, Force: 500 N, Bonding time: 10 min.

A detailed listing of the program used for PiRL bonding can be found in Table 9. The best parameters determined for successful bonding were: Temperature: 150 °C; Force: 500 N; Bonding time: 10 min. In order to ensure excellent contact of the bonding surfaces, clamps were used for removal of trapped air. Excellent bonding was obtained with the procedure described above. Figure 36 shows a digital photograph of a PiRL bonded wafer pair.
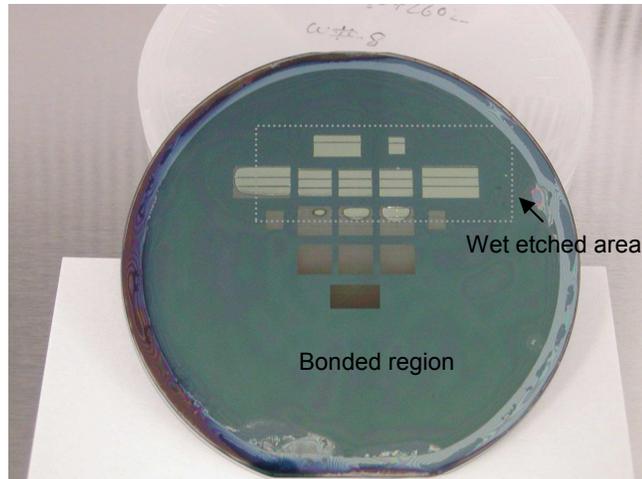
Figure 36.    Digital image of patterned silicon wafer after successful PiRL bonding with a pyrex wafer, as seen through the pyrex wafer side.

Upon satisfactory bonding, the silicon-Pyrex wafer pair was diced to ascertain the bond strength. Figure 37 presents a SEM image of two silicon wafers bonded with a PiRL interlayer. A 3.5 µm thick layer of PiRL can be observed sandwiched between two silicon layers in this figure.
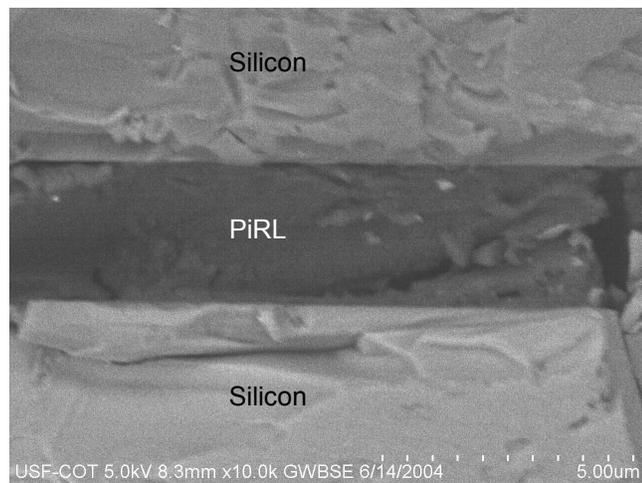


Figure 37.    SEM image of two silicon wafers bonded with PiRL interlayer.

The PiRL bonded wafer pair survived the dicing process very well and none of the chips came apart during or after the dicing. In spite of the success of the above

described experiments, another set of wafers (shown in Figure 38) developed cracks after undergoing PiRL bonding
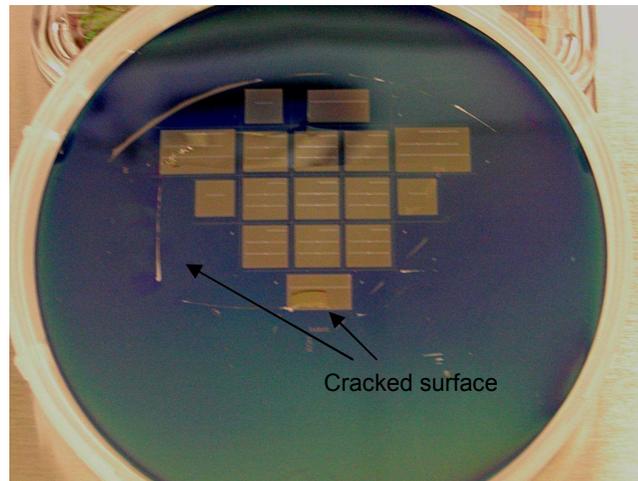


Figure 38.    Digital image showing silicon wafer breakage after unsuccessful PiRL bonding, as seen from the silicon wafer side.
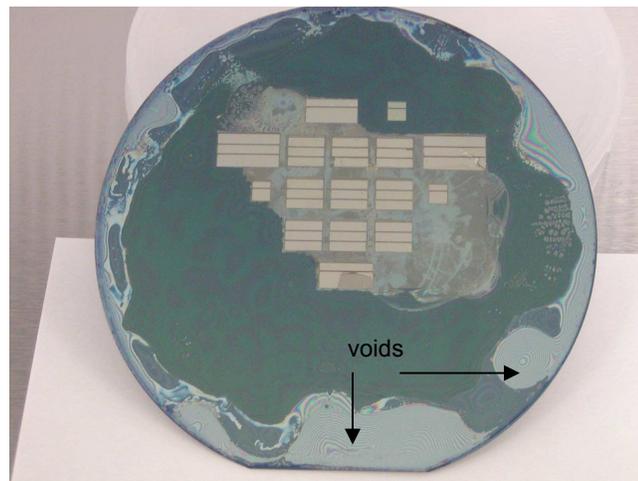


Figure 39.    Digital image of silicon wafer after unsuccessful PiRL bonding showing voids in the bonded region, as seen through the pyrex wafer.

The described PiRL bonding process worked well in the following scenarios: (i) for a mask design having wet etched areas (180 µm deep) distributed all over the 100 mm wafer surface, and (ii) for a wet etched area (180 µm deep) with the extent of etched area highlighted in Figure 36. Probable reasons of wafer breakage and bonding failure could

be: uneven distribution of the deep wet etched region and stresses developed due to metal

thin film deposition and PECVD oxide deposition. The exact cause of this anomalous

behavior could not be comprehended during the scope of this research. However, the

advantages of PiRL bonding method and the initial encouraging results provide enough

motivation for solving the stated problem in the future.


3.4.1.2. Anodic bonding


Anodic bonding is a very popular process in MEMS packaging. Anodic bonding,

also referred to as field assisted thermal bonding, can be used to bond a sodium-rich glass

with any conductive substrate. Corning #7740 (Pyrex) is widely used for anodic bonding

with silicon. Table 5 highlights some of the important material properties of pyrex [42].

Table 5.        Material properties of pyrex [42].

| Property | Value | Unit |
|---|---|---|
| Density | 2.23 | g/cm$^3$ |
| Young's modulus | 62.75 | GPa |
| Poisson's Ratio | 0.20 | |
| CTE | 3.25 | °C x 10$^{-6}$ |
| Softening point | 821 | °C |
| Annealing point | 560 | °C |
| Strain point | 510 | °C |
| Dielectric const. (20 °C, 1MHz) | 4.6 | |
| Alkali content | 4.2 | wt% |

An advantage of using pyrex for anodic bonding in MEMS applications is that the

thermal expansion coefficient (CTE) of silicon and pyrex is comparable over a wide

temperature range and as a result there is little residual stress after bonding. Anodic

bonding can be carried out by applying high temperature (180 - 500 °C) and high d.c.

voltage (200 - 1200 V) to a silicon-Pyrex wafer stack for a short time (10 – 20 min) in atmosphere or vacuum conditions.

Figure 1 presents a schematic of a typical anodic bonding set-up. The silicon wafer is biased positive with respect to the Pyrex wafer. At high temperatures, the $Na^+$ ions present in the Pyrex wafer migrate to the cathode. As a result of this phenomenon, a space charge region develops at the glass/Si interface. The electrostatic forces built across this space charge region due to the applied high voltage act to pull the silicon and Pyrex wafers into intimate contact thereby initiating the bonding process. The process stops when a depletion region is formed at the mating interface. An irreversible chemical bond is formed at the Si-glass interface due to a combination of electrostatic, electrochemical and thermal mechanisms [1].
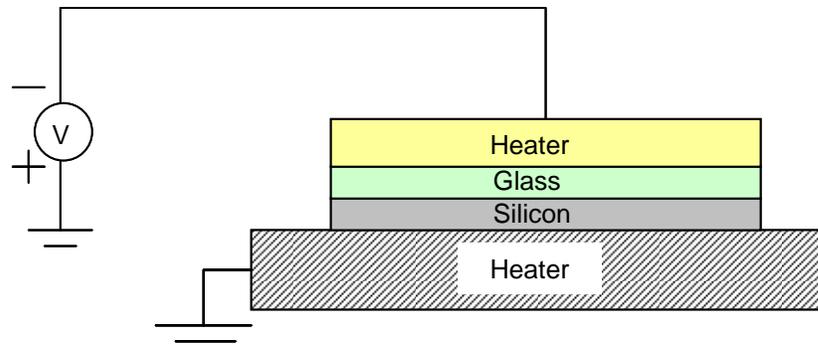


Figure 1.      Schematic of a typical anodic bonding set-up.

Anodic bonding produces very strong bonds and is generally not pursued as a temporary bonding process. However in the complete micromirror fabrication process, the final release of the surface micromachined devices needs to be carried out in a 49% HF solution. The pyrex wafer cap can be etched away simultaneously at this step ensuring release of the bulk micromirror device from the handle wafer. In view of above,

the applicability of the anodic bonding method was investigated and experiments were carried out to determine the anodic bonding parameters suitable to the micromirror design. The quality of wafer surfaces influences the anodic bonding process. The presence of particles and residue on the mating surfaces can lead to voids in the bonded area hence cleanliness of the wafer surfaces was ensured prior to initiating the bond process. Firstly, a bare Si wafer (n-type, 350 µm, DSP, 1-20 Ω-cm) was bonded to a pyrex wafer in vacuum with the various bonding parameters set as follows: Temperature: 400 °C; Voltage: 1000 V; Bonding Time: 10 min; Piston Force: 500 N. Table 8 lists the step by step program used for the anodic bonding procedure.

After success of the above experiment a Si wafer, deposited with 100 nm LPCVD nitride and etched with KOH solution, was bonded with a pyrex wafer. The bonding parameters used were the same as above. Again, excellent bonding was obtained in the above condition (see Figure 41) even with the presence of the silicon nitride layer.
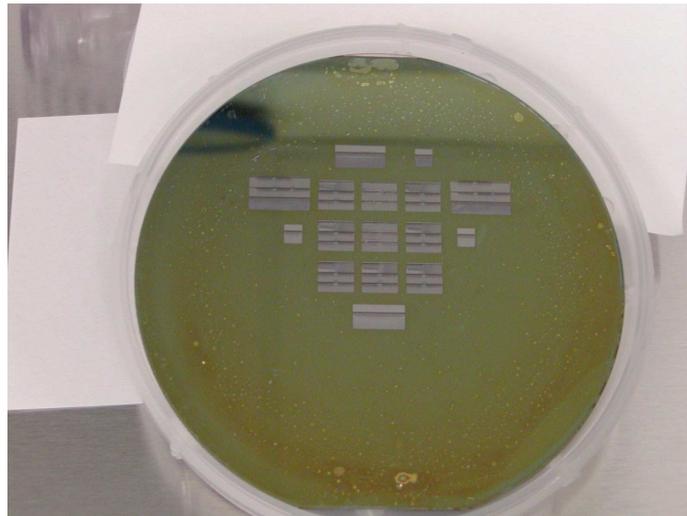


Figure 41.　　Silicon wafer successfully bonded to Pyrex wafer.

Figure 42 and Figure 43 show the graphical plots for variation of current, charge, voltage and temperature with time for the case of the anodic bonding experiment described above.



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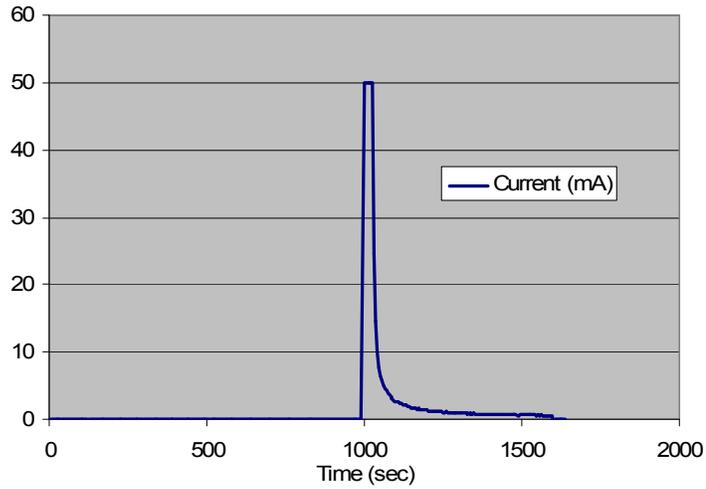
Figure 42.    Plot of current vs. time for anodic bonding with nitride layer thickness of 100 nm.
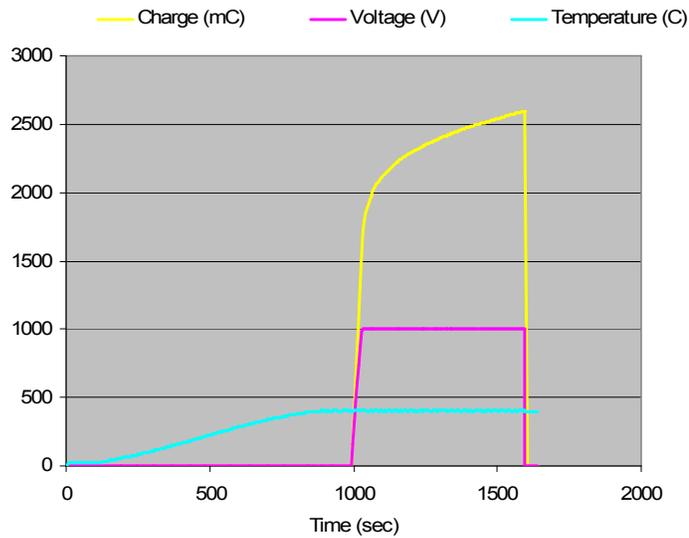


Figure 43.    Plot of charge, voltage, and temperature vs. time for anodic bonding with nitride layer thickness of 100 nm.

An issue in the current fabrication process design is that, the Si (111) sidewalls could suffer damage due to the DRIE etch steps. It was thereby proposed that a silicon oxide layer be deposited on the V-grooves that would serve as an effective masking layer for DRIE. Since the V-groove depth is 180 µm in the current design, a 1.2 µm thick PECVD oxide layer (considering a Si: oxide selectivity of 150:1 in DRIE) was deposited on a Si wafer patterned with V-grooves. The said wafer was then bonded to a pyrex wafer using the parameters mentioned above. Figure 44 and Figure 45 present the X-Y plot of the variation of current, voltage, charge, and temperature as a function of time in case of the anodic bonding experiment described above.
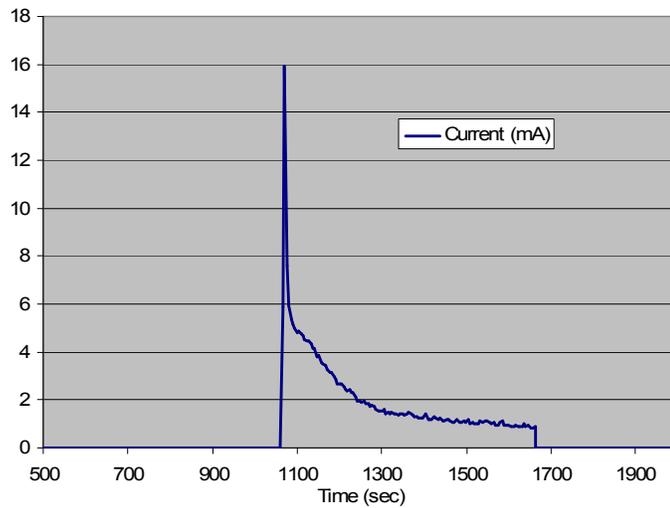


Figure 44.    Plot of current vs. time for anodic bonding with 100 nm nitride layer and 1.2 µm oxide layer.
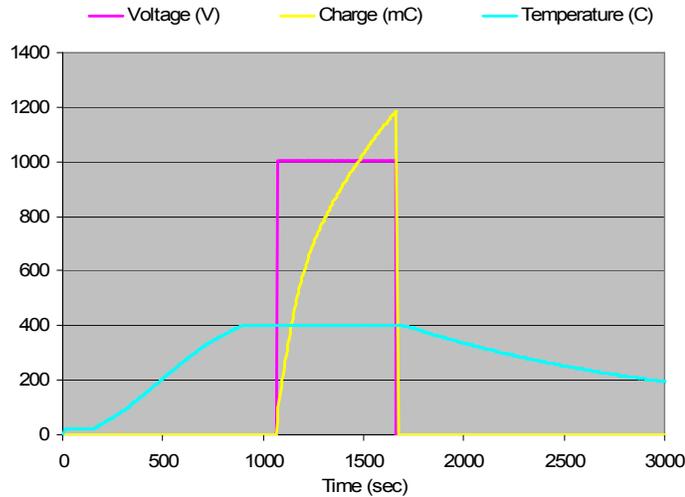
Figure 45.    Plot of voltage, charge, and temperature vs. time for anodic bonding with nitride layer and 1.2 µm oxide layer.

The result of this experiment (shown in Figure 46) was not promising. The bonding appeared good on the wafer periphery but the center region of the wafer showed a large void. As discussed above, anodic bonding requires the flow of an anodizing current through the pyrex-wafer conductive path. The presence of a 100 nm LPCVD nitride layer and 1.2 µm PECVD oxide layer between the silicon and pyrex surfaces provided a high resistance path to the current and consequently led to bond failure.
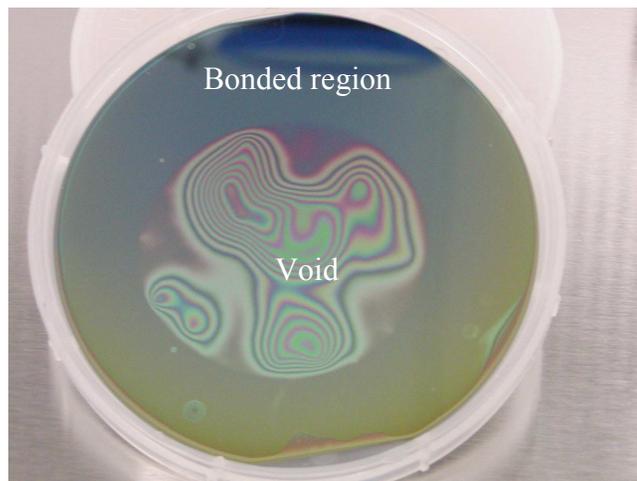


Figure 46.    Anodic bonding failure with 1.2 µm oxide layer on silicon.

63

Plaza et al [43] have shown that in anodic bonding, the electrostatic pressure required to pull the bonding surfaces together decreases with an increase in the thickness of the intermediate silicon oxide layer. Application of a high voltage during anodic bonding can possibly compensate for such loss of electrostatic pressure. Additionally, it has been demonstrated in [44] that anodic bonding becomes easier with application of high temperatures due to an increase in the deformability of oxide at higher temperatures. Therefore, the application of a higher voltage and higher temperature can be investigated in the future in order to successfully bond silicon to Pyrex with an intermediate layer of oxide.

Alternatively, an investigation can be carried out to determine the minimum thickness of oxide layer sufficient for protecting the mirror surface. Since the tilted mirror surface is not in line of sight of the reactive gas ions, there is a fair possibility that the surface will experience a very slow etch rate in the directional DRIE. In view of this, a thinner (< 1.2 μm) oxide layer might prove to be of sufficient thickness for protecting the mirror surface.

Since PiRL bonding demonstrated unresolved issues while bonding patterned Si wafers, anodic bonding was considered for the process steps. However, the idea of protecting the sidewalls with oxide layer deposition was not implemented at this stage.

3.4.2. Chip-level bonding

The chip scale bonding step, in the process flow described earlier, requires a permanent bond to transfer the micromirror array on to the rotary stage. Figure 31 is a

schematic illustration of the chip bonding step. Once the mirror array is transferred (bonded) to the surface micromachined device, the PolyMUMPs rotary stage and actuation mechanism need to be released in a 49% HF solution [19]. Hence it is important that the permanent bonding agent used here should be resistant to the concentrated HF solution. The Finetech FINEPLACER® Pico bonder[4] tool (shown in Figure 47) was used for the chip-level bonding step. Maximum applicable temperature and force in this tool are 400 °C and 120 N [45]. Hence it was essential that the process requirements of the chip bonding step should be within the above range of temperature and applied force.



Figure 47.     Finetech® FINEPLACER Pico bonder. Courtesy [45].

In summary, the key requisites of the bonding process were identified as following:

i)     Provide a strong and permanent bond.

ii)    Resistance to concentrated HF solution.

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[4] Finetech GmbH & Co. KG, Wolfener Str. 32/34 Haus L, Berlin, Germany.

iii)     Required temperature and pressure should not be very high (< 400 °C and 120 N respectively).

iv)     Tolerant to small surface impurities and imperfections.

Direct fusion bonding of silicon to poly-Si was not feasible in this case since surface roughness of poly-Si might be detrimental to bond formation. The very high temperature and pressure required for direct bonding might be detrimental to the positioning mechanism structures that are made of polysilicon and gold. Additionally, the application of very high temperature and force is not possible using the available chip bonding tool. Indirect bonding methods were hence investigated. The various approaches considered are described in the following paragraphs. Experiments carried out prior to finalizing the bonding process are also presented.

3.4.2.1. Adhesive bonding - epoxy

Epoxy is the most widely used material for device encapsulation in the IC industry and is particularly attractive for chip scale bonding applications [46]. Hence experiments were carried out with the aim of investigating the applicability of epoxy bonding for the micromirror chip bonding step. The epoxy EPO-TEK™ H20E used in the experiments is a two component thermally and electrically conductive epoxy designed for microelectronic chip bonding [47].

Patterned silicon chips measuring 1cm X 1 cm and having features similar to the PolyMUMPs rotary stage device were used as bonding substrates. A silicon wafer was patterned with the rotary stage mask, etched by 3 μm using DRIE, and diced into 1 cm.

sq. chips to prepare the chips. The two components (part "A"- epoxy resin and silver powder and part "B"- hardener and silver powder) of the H20E were mixed thoroughly in equal proportions to prepare the bonding paste. This paste was then spread uniformly on a glass slide with a knife edge. Individual chips, prepared as described above, were then inverted (pattern facing down) and dipped into the epoxy paste and placed on a clear glass slide for bonding. This was done in order to investigate the bonding interface. The epoxy was then cured at a temperature of 80 °C with an applied force of 80 N. The bonded chips, as shown in Figure 48, displayed very strong bond formation and could not be pulled apart.
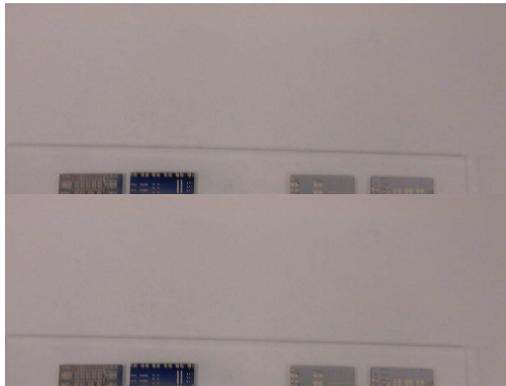


Figure 48.      Silicon chip bonded to glass using epoxy

A bonded chip-stack (two Si chips bonded using epoxy) was then immersed in a 49% HF solution to find the resistance of epoxy in the acid. It was found that the bond broke off (epoxy etched away) in 50 seconds. It was determined from the above process that the epoxy bond will not hold during the PolyMUMPs chip release step. In addition, a thin and uniform layer of epoxy is required to facilitate even and precise application of epoxy on the bonding surface. This requirement is extremely difficult to meet by means of manual application. In view of the issues discussed above, the epoxy bonding method

was not pursued further. However, an anhydride base epoxy that can be spin deposited on a substrate can potentially be used for the micromirror chip-level bonding step.

3.4.2.2. Adhesive bonding – BCB

Benzocyclobutene (BCB), also known as Cyclotene is a thermoset polymer material produced by the Dow Chemical company. BCB has reportedly been used as a bonding agent in numerous MEMS and IC applications [48], [49]. The particular properties of BCB that make it a very attractive alternative for the application here are that it is resistant to acids, most organic solvents, and alkaline solutions, and produces very strong bonds upon curing with zero outgassing. BCB has low sensitivity to surface preparation and can withstand temperatures as high as 350 °C. It can be spin coated to form very uniform and thin layers and is also available in photo-imageable kind.

The accurate alignment of the micromirror array with the rotary stage devices entails precise application of the bonding agent on either one or both the chips. Lithographic patterning of photo-imageable BCB can be done to precisely define the BCB layer on a substrate. Unfortunately, in the fabrication process described here, the bonding substrates were 1 cm X 1 cm chips. Performing photolithography operations on such chips could prove to be very challenging. Moreover BCB and its adhesion promoter have a very short shelf life and at the time of this research work the facility of long term storage of BCB was not available. In view of the above factors and time limitations of this research, the BCB bonding option was not pursued further. However, BCB remains a viable alternative for permanent bonding of micromirrors to the rotary stages.

3.4.2.3. Eutectic bonding - Si-Au

Gold-silicon eutectic bonding has been widely used in packaging VLSI chips. This process involves bonding of Si to gold at a temperature exceeding the eutectic temperature of Au-Si binary system [50]. Figure 49 presents the binary phase diagram of Au-Si system.
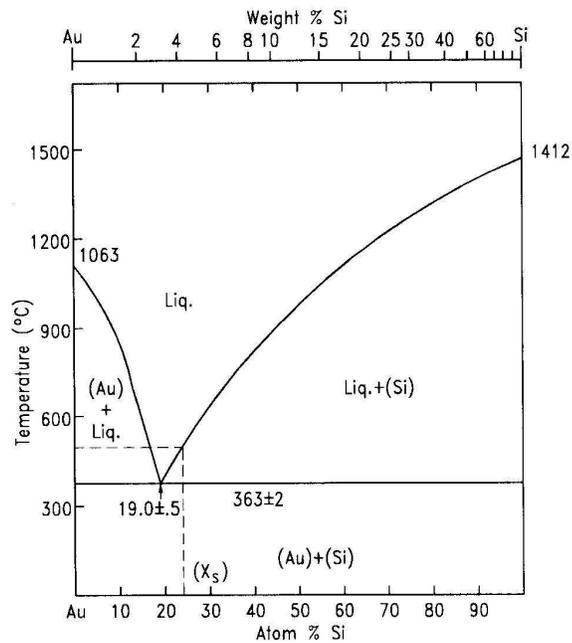


Figure 49.      Binary phase diagram of Au-Si [50].

Gold and silicon form a eutectic alloy containing 19 at % Si at a temperature of 363 ° C which is far lower than the melting temperatures of both Au (m.p. 1064 °C) and silicon (m.p. 1410 °C) [51]. In order to carry out the bonding, a thin layer of Au is required on either of the bonding surfaces. The PolyMUMPs process allows the deposition of a metal (Cr 200 Å /Au 5000 Å) layer on the Poly2 layer. This Au layer can be used as one of the bonding surfaces. Features on the bulk-micromachined Si

69

micromirror can be designed in order to provide the other bonding surface. Hence eutectic bonding can be easily incorporated as a bonding step here.

Eutectic bonding places stringent requirements on surface preparation. Any native oxide present on the surface of the bonding substrate results in bonding failure [52]. Silicon substrates similar to those described in the epoxy bonding discussion above were prepared for the experiments here. Another set of substrates was prepared by sputter depositing 200 Å Ti (since Cr deposition was not available) and 3000 Å Au on a Si wafer patterned similar to the above substrates. This wafer was then diced into 1 cm. sq. chips. A 2 min 6:1 BOE etch was performed on the Si chips immediately before bonding to etch away any oxide present of the Si surface. Eutectic bonding was carried out at the following conditions:

i)    Temp: 380 °C; Force: 80 N, Bonding time: 2 min.

ii)    Temp: 200 °C (2 min) + 380 °C (2 min); Force: 80 N, Bonding time: 4 min.

iii)    Temp: 200 °C (2 min) + 390 °C (2 min); Force: 80 N, Bonding time: 4 min.

iv)    Temp: 390 °C (2 min); Force: 80 N, Bonding time: 2 min.

None of the above set of parameters resulted in a strong bond formation. However, partial transfer of the gold pattern on to the silicon surface (see Figure 50) was observed. The transfer of the gold pattern on to the silicon surface at certain sites suggests that some silicon-gold eutectic formation occurred at those sites but a strong bond did not form due to the poor adhesion of gold layer with the underlying substrate (chip with

70

rotary stage). The adhesion failure can be possibly overcome by depositing a thicker gold layer on the rotary stages.
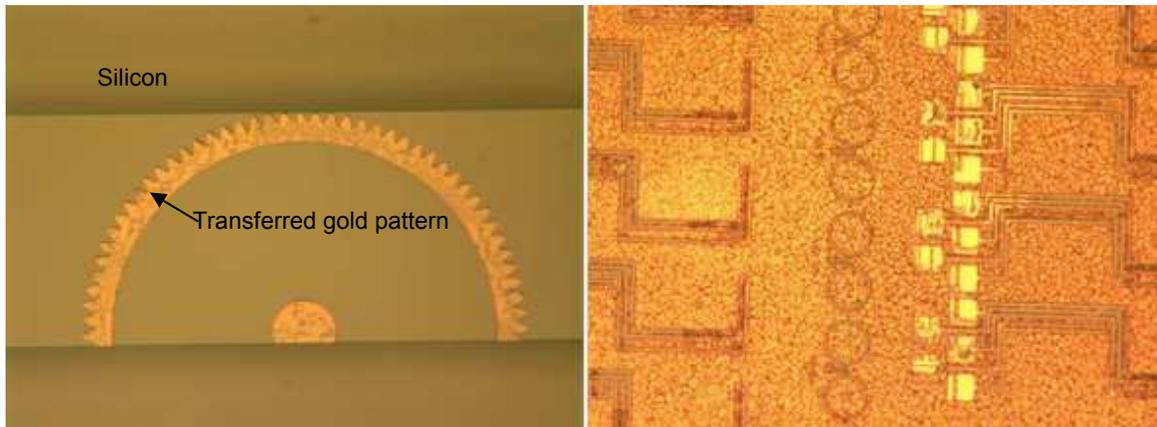


Figure 50.    Eutectic bonding results showing transfer of gold pattern on silicon.

The overall eutectic bonding failure observed in the described circumstances could be due to any combination of the following conditions: improper surface preparation, high surface roughness, insufficient thickness of Au layer or its adhesion layer, and insufficient bonding temperature. In conclusion, optimization of the above bonding parameters is required in order to obtain satisfactory eutectic bonding for the chip level bonding step.

3.4.2.4. Thermocompression bonding – Au-Au

Thermocompression (TC) bonding involves bonding of like materials in the presence of high temperature and high applied force. Bonding of materials with a low melting point is more viable in this method. As mentioned earlier, PolyMUMPs fabrication allows for a Au (Metal) layer as the top layer on poly-Si structures hence Au-Au TC bonding was considered as an option. Since Au has a negligible etch rate in 49%

71

HF, it is suitable for the application here as the PolyMUMPs device release process will have no negative effects on the bonding interface of the micromirrors and the rotary stages. Au-Au TC bonding has previously been used as an excellent bonding strategy in MEMS applications [53].

Experiments were next carried out to determine the optimum parameters for Au-Au TC bonding. The bonding substrates were prepared by patterning bare Si wafer with the "Metal" mask from the PolyMUMPs mask set. DRIE etching of Si (4 μm) was then done with photoresist as the mask material to fabricate structures similar to the actual Rotary Stage devices. A thin (200 Å) Ti adhesion layer was then sputtered on the patterned wafer followed by a 5000 Å Au layer. These thicknesses were chosen to conform to the standard thicknesses of PolyMUMPs processing. The Si wafer was then diced into 1 cm X 1 cm chips. A protective layer of photoresist was deposited on the wafer prior to dicing in order to prevent deposition of dicing debris on the chip surfaces. The photoresist layer was stripped off by acetone-methanol-DI water rinse after dicing.

Experimental bonding was carried out with applied force of 80 N, bonding time of 2 min and temperatures of 380 °C, 350 °C, 320 °C and 300 °C. A range of temperatures was considered here in order to determine the lowest possible temperature at which a good bonding can be achieved. It was found from the experiments that a temperature of 320 °C, force of 80 N and bonding time of 2 min gave excellent results. Figure 51 is a graphical representation of the applied and observed temperature profile for a successful Au-Au thermocompression bonding as obtained using the WinFlipChip bonding software.
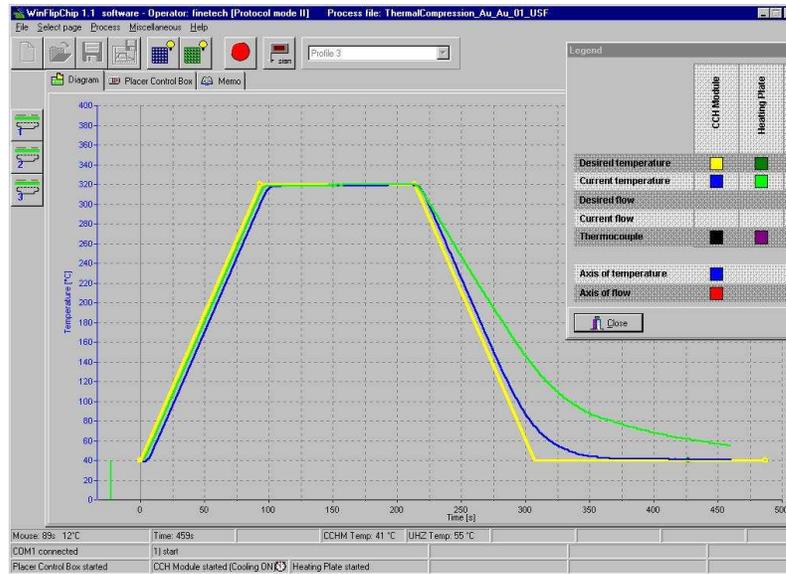
Figure 51.    Temperature profile for successful Au-Au thermocompression bonding.

A point to note here is that the cleanliness of the bonding surfaces is vital for obtaining good bonding. A few experimental chips failed to bond because of the presence of particles and debris on the chip surfaces. However, Au-Au thermocompression does not place stringent requirements on the cleaning procedure. A simple Acetone-Methanol soak followed by DI water rinse and drying was found to be sufficient for ensuring good bond quality.

An experimental fact overlooked at this stage was the high etch rate (> 10 kÅ/min) of sputtered titanium films in 49% HF [54]. Alternatively, chromium (200 Å) can be used here as an adhesion layer for Au since it is known to have a negligible etch rate in HF [55]. In consideration of the low temperature and force requirements for bond formation, excellent resistivity of Au to concentrated HF solution, and convenient surface preparation, Au-Au thermocompression bonding was found to be the most suitable method for chip scale bonding in the RMA fabrication process.

An overview of the micromirror array fabrication process flow was described earlier in this chapter. In the next chapter, various details of the fabrication process are discussed and the results obtained at different processing stages are presented.

CHAPTER 4


FABRICATION OF MICROMIRROR ARRAY


4.1.    Introduction


An outline of the micromirror fabrication process flow and an investigation of a variety of relevant bonding techniques were presented in Chapter III. The following sub-sections elaborate on the choice of particular elements in the process flow. The various details pertaining to the implementation of the process steps is given in section 4.2.


4.1.1.  Substrate selection


In the process steps described here, an n-type Si wafer was preferred here since p-type doping slows down the anisotropic etch rate of silicon [37]. Silicon wafers of thickness 300-350 μm were employed due to ease of handling and ready availability. However a thinner wafer (near 180 μm) will eventually be better here since the device reflective area per unit volume will be higher for micromirrors fabricated using a thinner wafer. The same process flow can be used for both thick and thin wafers with a minor modification in the Bosch DRIE etch time.

### 4.1.2. Nitride deposition

The methods available for silicon nitride layer deposition were PECVD (Plasma –
Enhanced CVD) and LPCVD (low pressure CVD). PECVD thin films are deposited at
low substrate temperatures (300 – 400 °C) and have a higher pinhole density than films
deposited by LPCVD [1]. Besides this, PECVD deposition systems have limited wafer
intake capacity. On the other hand, LPCVD deposition provides excellent film uniformity
and a large number of wafers can be processed simultaneously in a LPCVD furnace. In
addition, LPCVD silicon nitride is known to work as an excellent masking material with
negligible etch rate in KOH [56], hence it was used here as the hard mask for the
anisotropic wet etch. The patterning of this masking layer was done by lithographically
defining the various structures using positive photoresist and etching the open areas in
RIE (see Table 11).

### 4.1.3. Anisotropic wet etching

The aqueous alkaline solutions most commonly used for anisotropic etching of
silicon are: potassium-hydroxide (KOH), tetramethylammonium hydroxide (TMAH), and
ethylenediamine-pyrocatechol-water (EDP). EDP etching was not chosen here due to
safety concerns [57]. A 25 wt. % TMAH solution at 90 °C can be used for the anisotropic
etching with silicon oxide as the hard mask. It has been reported that TMAH solution
with strength greater than 22 wt. % should be used to obtain the smoothest Si surfaces
[58]. However, the undercut obtained with TMAH etch solutions is reportedly much

76

higher as compared to that obtained with KOH since the (100):(111) selectivity ratio is lower in TMAH [37]. The addition of IPA to a TMAH solution has been reported in [37] to be effective in reducing the undercut ratio.

A KOH solution was preferred here since in addition to lower undercutting anisotropic etching using KOH is known to produce very smooth mirror-like (111) surfaces [59], [37]. The following reaction sequence has been suggested for reaction of silicon with alkali metal hydroxides [37]:

$$Si + 2OH \rightarrow Si(OH)_2^{2+} + 4e^- \qquad (4.1).$$

$$4H_2O + 4e^- \rightarrow 4OH^- + 2H_2 \qquad (4.2)$$

$$Si(OH)_2^{2+} + 4OH^- \rightarrow SiO_2(OH)_2^{2-} + 2H_2O \qquad (4.3)$$
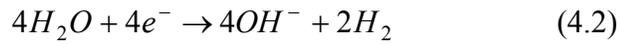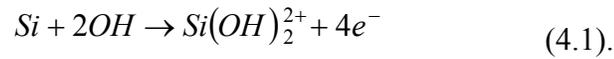
The overall reaction is,

$$Si + 2OH^- + 2H_2O \rightarrow Si(OH)_2^{2+} + 2H_2 \qquad (4.4)$$

As can be seen from equation (4.4), the overall reaction consumes water and hydroxyl ions and results in the formation of hydrogen gas. The accumulation of the released hydrogen gas bubbles on the silicon surface can result in slower etch of the underlying silicon surface thus causing what is known as "micromasking" effect. This phenomenon leads to the formation of localized hillocks that roughen the etched surface. Agitation of the etchant using ultrasonic methods [59] or magnetic stirring has been found to be very effective in avoiding micromasking. Magnetic stirring at the rate of 200 rpm was used here for the KOH etching step.

The maximum etch rate of silicon in KOH solutions has been observed at a concentration of 15%. However, a KOH solution with concentration below 20% is

generally not preferred in MEMS applications since it tends to produce rough surfaces and deposits insoluble white residues on the silicon surface [56]. Seidel has shown that for KOH solution concentrations above 20%, the etch rate of Si (100) decreases. It is also known that the silicon etch rate increases with an increase in temperature of the aqueous alkaline etching solution. The selection of the right combination of temperature and concentration of the KOH solution should be done based upon the particular requirements of the device being fabricated.

Besides low surface roughness, another important criteria for etch parameter selection was the anisotropy ratio. Anisotropy Ratio (AR) is defined as $R_{\{100\}}/R_{UE}$ where $R_{\{100\}}$ is the etch rate of Si (100) plane and $R_{UE}$ is the underetch rate [60]. This ratio influences the reproducibility and accuracy of the anisotropic etch process. Ideally the value of AR should be infinite. However factors like alignment errors, quality and type of masking material used and properties of etchant lower the practically feasible AR.

An experiment was carried out to determine KOH etch conditions that produce the least amount of undercut. The etch depth measurements in the described experiments were done by the "depth-of-focus" method. In this method, the height/depth of a structure is measured by alternately focusing on the top and bottom surface of the structure. Calibrated optical microscope micrometer readings pertaining to the two focus positions are then subtracted to calculate the height difference. The results from the experiment are summarized in Table 6. A magnetic stirrer rotating at the rate of 200 rpm was used to stir the KOH solutions used in all the experiments discussed above.

It can be observed in Table 6 that a 45 wt % KOH solution at 80 °C gives the least undercut and the smoothest surfaces. The smoothness of the Si (111) surface was

78

evaluated by visual inspection using an optical microscope. It was thereby concluded that such solution would be most favorable for the wet anisotropic etch step.

Table 6.        KOH etch conditions.

| KOH conc. (%w/w) | Temperature (°C) | Etch Rate (μm/min) | Selectivity (100):(111) |
|---|---|---|---|
| 30 | 60 | 0.185 | 29:1 |
| 30 | 80 | 1.21 | 37:1 |
| 45 | 80 | 0.622 | 150:1 |

4.1.4.  Oxide deposition


A silicon oxide layer was used as the dry etching hard mask since it has excellent selectivity (150:1) in DRIE and unlike Al it does not form any residues in the process. Since the thickness of Si wafer was 350 μm, a 2 μm thick oxide (considering a photoresist layer of at least 1 μm will be present) layer was required for the etch mask. PECVD deposition was preferred here since it is a fast and low temperature process and has known to be adequate for DRIE masking.


4.1.5.  DRIE


In DRIE, areas having larger openings etch faster than areas with smaller openings for a given number of process cycles. This phenomenon is termed as the "microloading" effect [1]. Hence care should be taken during the mask design stage to ensure equal distribution of open areas for features that need to be etched to equal depths.

### 4.1.6. HF release etch

The etch rate of Pyrex 7740 was determined prior to the actual release step. A 1 cm X 1 cm chip of a silicon-Pyrex bonded wafer stack was immersed in 49% HF to determine the etch rate of Pyrex. As shown in Figure 52, 165 µm Pyrex was etched by within 25 min in HF, giving the etch rate as 6 µm/min.
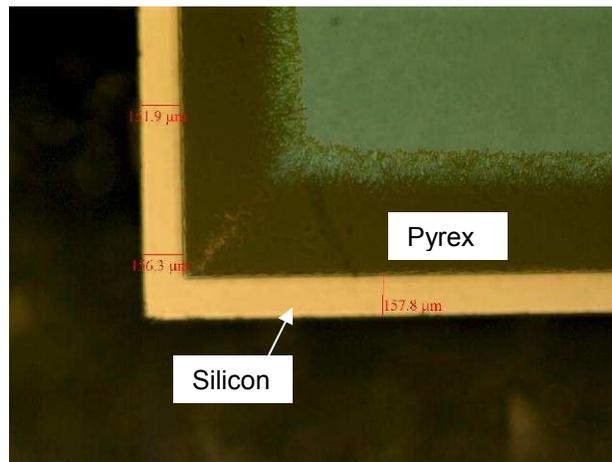


Figure 52.      Pyrex wafer cap etched after 25 min.

At the rate of 6 µm/min, the Pyrex wafer cap bonded to the micromirror top region will etch away in approximately 5 min. However, the PolyMUMPs process recommends just a 2 min etch in 49% HF. Hence the area of the extruded structure on the micromirror top should be reduced to 18 X 12 $\mu m^2$ to fully release the Pyrex cap in less than 2.5 min. Additionally, a thin layer of PECVD oxide (etch rate in 49% HF = 1.4 µm/min) deposited on the top of the silicon nitride (etch rate in 49% HF = 52 Å/min) layer before anodic bonding may help in faster release of the "handle wafer" [54].

4.2.    Detailed process flow and results

The various details of the process steps that were used to fabricate the micromirror array
are described below.

i)      Deposit 100 nm LPCVD silicon nitride on a 350 μm thick, double side
        polished (DSP), n-type, high resistivity (1-20 Ω-cm), Si (100) wafer.

ii)     Spin photoresist PR1-2000A on wafer front side at 3000 rpm for 40 sec
        and soft bake at 120 °C for 60 sec.

iii)    Align "KOH" mask with wafer flat parallel to the Si <110> direction and
        expose for 6 sec in EVG 620 mask aligner. Develop in RD6 for 25 sec.
        Rinse in DI (de-ionized) water and dry. Step height of 1.9 μm is observed.

iv)     Etch 100 nm silicon nitride in RIE for 2 min. Refer Table 11 for process.

v)      Etch silicon by 180 μm in 45 wt% KOH solution heated to 80 °C for 5
        hours using magnetic stirrer at > 200 rpm for best results. Figure 53 is a
        SEM micrograph of a V-groove surface formed by KOH etching.
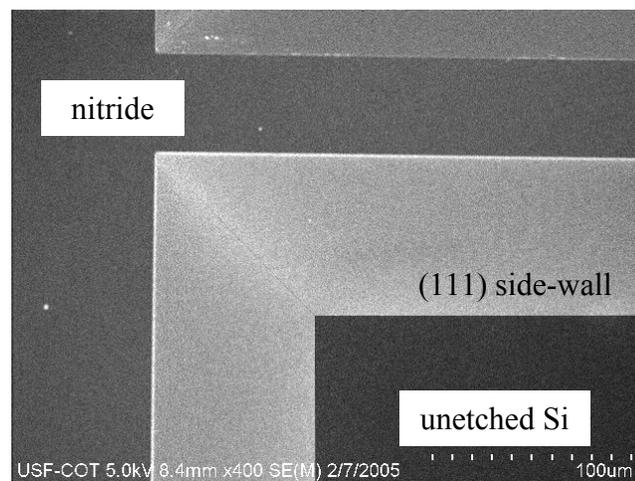


Figure 53.     V-groove formed after KOH etching.

81

vi)     Spin photoresist PR1-2000A on wafer backside at 3000 rpm for 30 sec. Soft bake at 120 °C for 60 sec.

vii)    Align "Indent" mask with features on wafer using backside alignment and expose for 6 sec. Develop in RD6 solution for 25 sec. Rinse with DI water and dry. Step height of 1.9 μm is observed.

viii)   Etch 100 nm silicon nitride on wafer backside in RIE for 2 min.

ix)     Etch 4 μm silicon using Non-Bosch DRIE process for 2 min 30 sec.

x)      Strip photoresist by Acetone-Methanol rinse follow by rinse in DI water and dry.

xi)     Descum for 4 min in RIE using oxygen plasma.

xii)    Anodically bond wafer front-side with Pyrex wafer. See Table 8 for run program.

xiii)   Sputter 200 Å Cr (20 sec) followed by 3000 Å Au (6 min) on wafer bottom side. Process variables: 29 sccm Ar, 360 W RF power, 2 mT pressure.

xiv)    Spin photoresist S1813 at 3000 rpm for 30 sec on metal deposited surface. Soft bake at 90 °C for 60 sec.

xv)     Align "Metal" mask with features on wafer and expose for 2.9 sec. Develop in MF319 for 40 sec. Rinse in DI water and dry. Step height of 1.3 μm is observed.

xvi)    Bake photoresist at 130 °C for 90 sec. Etch for 40 sec in Au etchant solution. Etch Cr layer in Cr etchant solution. Rinse in DI water and dry. Strip PR in acetone – methanol followed by rinse in DI water and dry.

xvii) Deposit 2 μm PECVD oxide for 42 min on wafer backside (side with metal pattern). Refer to Table 10 for process parameters.

xviii) Spin photoresist S1827 at 3000 rpm for 40 sec on the oxide layer. A thick photoresist is used here for use as additional DRIE masking layer. Soft bake at 90 °C for 60 sec.

xix) Align "DRIE" mask with wafer features and expose for 4.7 sec. Develop in MF319 for 60 sec. Rinse with DI water and dry.

xx) Etch 2 μm oxide in RIE for 70 min. Refer to Table 11 for process. Etch through wafer in approximately 500 cycles of DRIE. Refer to Table 12 for process parameters. Figure 54 below shows the SEM image of the bottom side of the micromirror array after through wafer DRIE. The cyclic process steps involved in the Bosch process resulted in scalloping of the vertical sidewalls of the etched feature as highlighted in Figure 55 below.
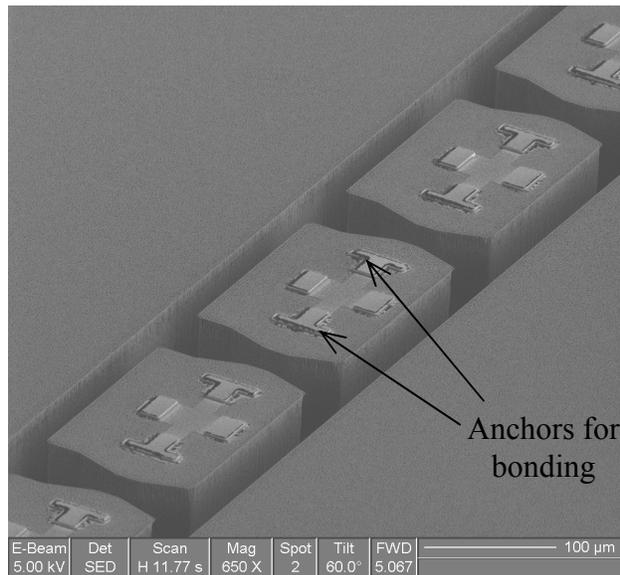


Figure 54.    SEM image showing bonding stands of micromirror array.
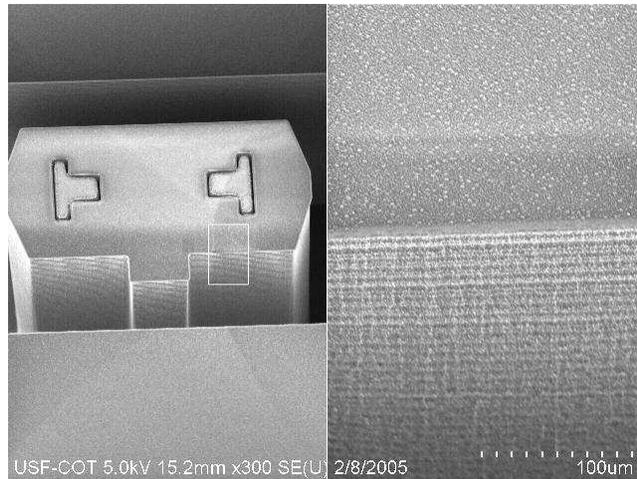
Figure 55.        Scalloping of sidewalls

xxi)    Confirm using SEM imaging and visual inspection whether through-wafer

etch is achieved. In case any more DRIE etching is not required proceed to

the next step Figure 56 shows the SEM image of a micromirror that is not

completely etched through.
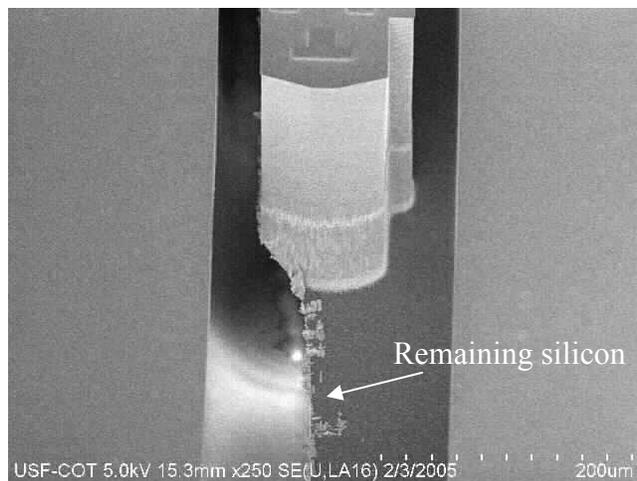


Figure 56.        SEM of micromirrors indicating incomplete etch-through.

Figure 57 shows the optical image for a completely etched micromirror

array as observed through the Pyrex wafer cap. The clear regions between

the mirrors confirm that through wafer etch has been achieved.

84
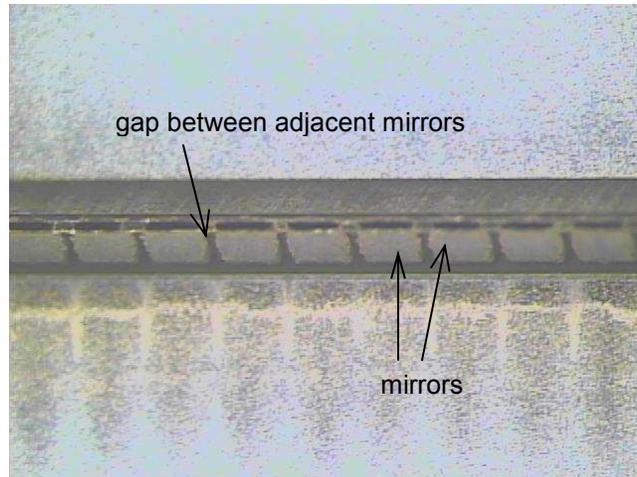
Figure 57.    Optical microscope image of micromirrors observed through Pyrex.

The SEM image in Figure 58 represents a micromirror for which

satisfactory through wafer etching is accomplished.
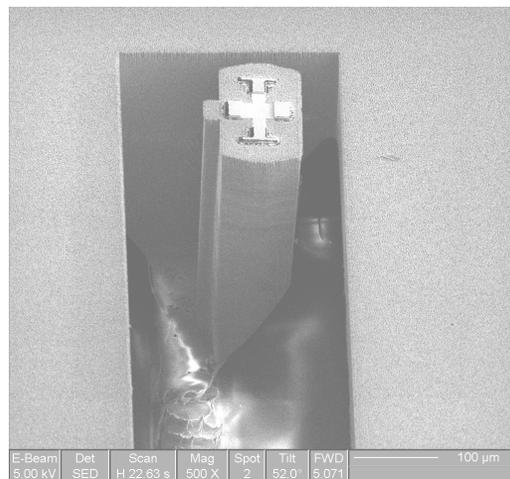


Figure 58.    Micromirror after completion of through-wafer etch.

xxii)   Etch oxide in RIE for 70 min.

xxiii)  Spin photoresist S1827 on etched wafer surface. Soft bake at 90 °C for 60

sec. This photoresist layer will work as a protective layer during the dicing

step that follows next.

xxiv)   Dice the wafer into the required number of chips.

xxv)   Strip photoresist from chips by soaking for 3 min in Acetone followed by Methanol.

xxvi)  Rinse with DI water and dry.

xxvii) Align features on chip bottom surface with rotary stage features in the flip-chip bonding tool. Thermocompression bond the micromirror chip with the PolyMUMPs chip substrate (see Figure 59). The size of the micromirror array chip shown in Figure 59 is 14 mm X 8.5 mm. The two horizontal lines that can be seen on the chip are two arrays of micromirrors. Alignment was difficult in the flip chip bonder due to poor contrast between the mirror stands and the rest of the mirror area. Hence a slight misalignment was observed in the micromirror bonded to the substrate as shown in Figure 60.
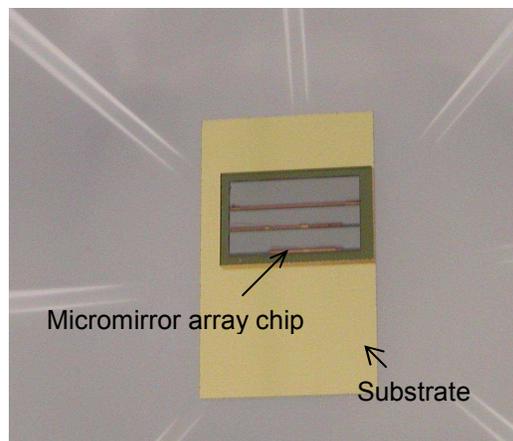


Figure 59.    Micromirror array chip bonded to substrate.
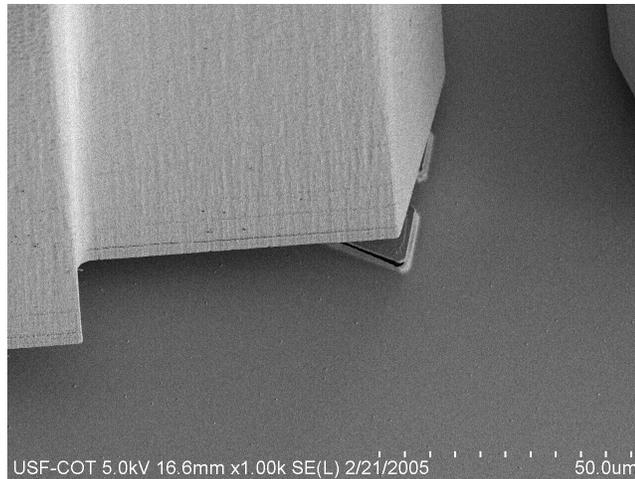
Figure 60.     Misalignment of micromirror during flip-chip bonding.

xxviii) Release the Pyrex wafer by immersing the bonded chip pair in 49% HF

solution for 20 min. Figure 61 presents an SEM image of the micromirror

array after the release of the Pyrex wafer. In order to carry out

simultaneous release of the Pyrex cap and the PolyMUMPs devices, a HF

etch of 2 min should ideally be sufficient. As described in section 4.1.6,

the time required for etching the Pyrex cap can be reduced by decreasing

the size of the bonding area on top of the micromirror and depositing a

PECVD oxide layer on the silicon surface exposed by KOH etching. Since

Cr deposition was not available at the time of fabrication of the

micromirror array shown in Figure 61, a Ti adhesion layer was deposited

beneath the gold layer. Upon immersion into 49% HF solution, this Ti

layer started etching off after 90 seconds. Most of the micromirrors got

debonded from the substrate due to this phenomenon. Figure 61 shows the

few micromirrors that were left over. Although the choice of adhesion

layer material does not affect the performance of the Au-Au

thermocompression bonding, it is recommended that a material resistant to concentrated HF solution e.g. Cr should be used in the micromirror fabrication process.
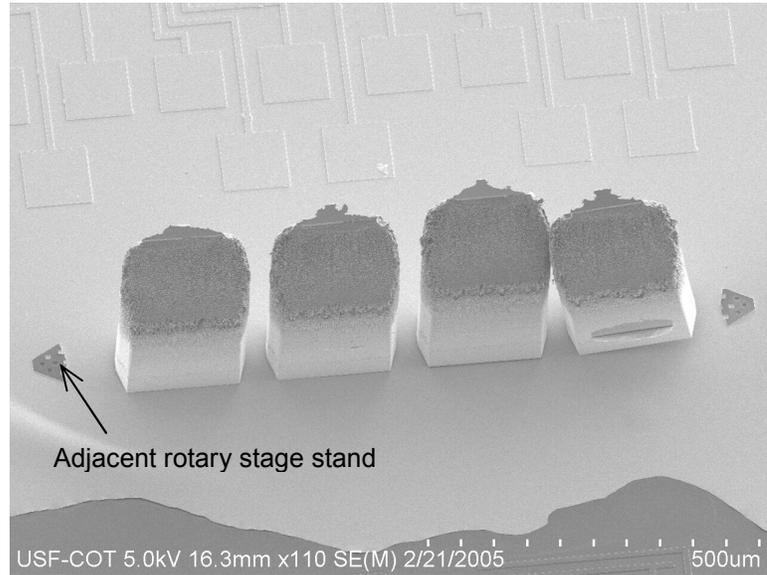


Figure 61. Micromirror array after release of Pyrex wafer cap.
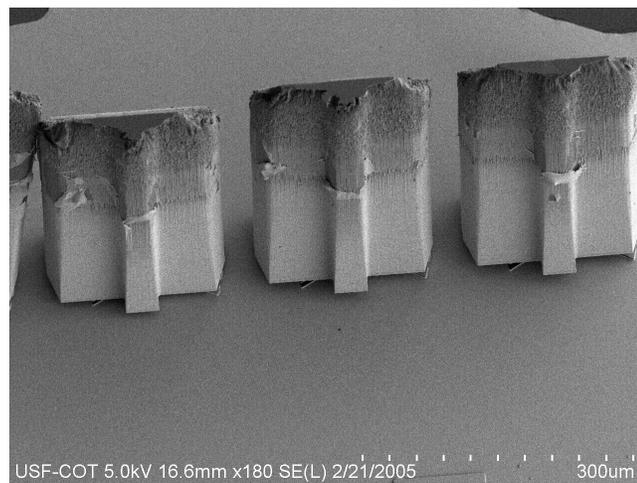


Figure 62. SEM image of micromirror array backside

It can be observed in Figure 61 and Figure 62 that the silicon surface underwent some damage which caused an increase in the mirror surface roughness. A possible cause

of this roughening is the exposure of silicon to HF solution for a long period of time (20 min). The etch rate of silicon in a 48 % HF solution at room temperature has been found to be approximately 0.3 Å/min [1]. Although the roughening effect of the HF solution is not expected to be high, a method for protection of the silicon micromirror from the HF solution needs to be determined in order to obtain the smoothest possible mirror surfaces. A possible solution for protecting the silicon surface here could be the deposition of a PECVD oxide layer on the silicon V-grooves prior to the anodic bonding step. Since the PolyMUMPs structures require a release etch time of 2 min, the ideal thickness of the protective PECVD oxide layer should be approximately 2 µm for guaranteed protection of the silicon surface.

Another reason for the blackening of the mirror device surface both at the front-side (see Figure 61) and the backside (see Figure 62).could be the deposition of residues in the DRIE tool. It was observed that other devices etched in the DRIE tool at the time of fabrication of this device showed similar depositions (see Figure 63). The similarity in the residue deposition on other devices and the micromirror array was that a blackish substance could be observed only in the deep etched region of the silicon structure. This problem can be addressed by cleaning the DRIE chamber before proceeding with the through-wafer etch.
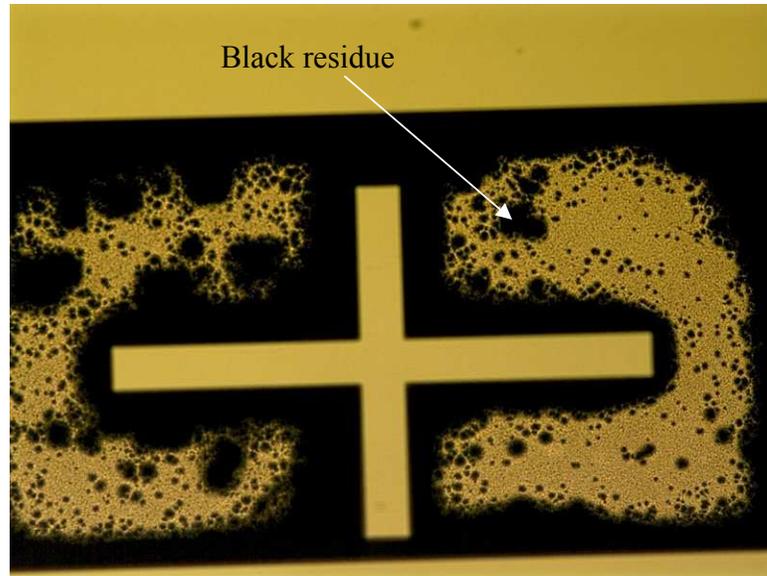
Figure 63.    Optical image of a DRIE etched structure showing deposition of residues.
Courtesy [32].

# CHAPTER 5

## CONCLUSION AND FUTURE WORK

5.1.    Conclusion

This thesis presented the design and fabrication of a re-configurable micromirror assembly for an optical microspectrometer. The particular contributions of this thesis are summarized below:

i)      Design and analysis of unidirectional rotary stage.

ii)     Design and analysis of modified thermal actuators.

iii)    Fabrication of bulk-micromachined mirror array.

iv)     Investigation and verification of micromirror chip transfer methodology.
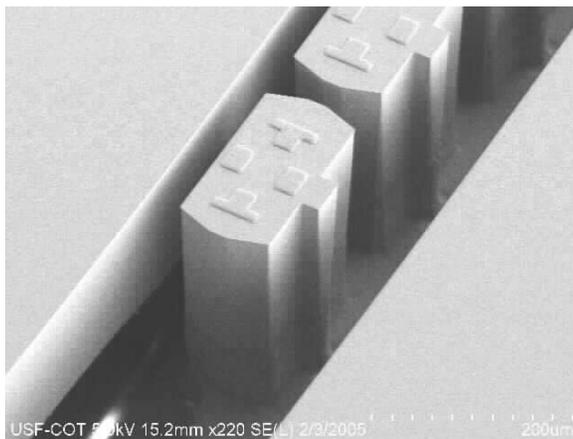


Figure 64.        SEM image of micromirrors.

The principal dimensions of the RMA system designed in this work are summarized in
Table 7 below.

Table 7.        Principal dimensions of the RMA.

| No. | Dimension and Unit | Value |
|---|---|---|
| 1 | Mirror width, μm | 200 |
| 2 | Mirror height, μm | 350 |
| 3 | Mirror thickness, μm | 100 |
| 4 | Mirror % reflective area | 100 |
| 5 | Rotary stage base diameter, μm | 163 |
| 6 | Mirror array pitch, μm | 230 |
| 7 | Linear fill-factor, % | 86.9 |
| 8 | Device foot-print, mm | 1.73 |

5.2.    Future work


The active performance of the unloaded and loaded (integrated with the mirror)
rotary stage driving mechanism and modified thermal actuator could not be tested in the
scope of this research. Wherever required, this work utilized simulated passive test parts
with patterns similar to the ones designed for PolyMUMPs fabrication. The designs of the
surface-micromachined components presented here have been submitted for PolyMUMPs
fabrication in run number 65. Upon completion of the fabrication, the testing of the active
devices can be done in the future to validate the theories presented here.

The rotary stages, as described earlier, need to be precisely positioned in order to
achieve control over the mirror angular deflection. Dickey et al [61] have demonstrated
an optical feedback method that can be employed for measuring rotation rate, intra-period
fluctuations in rotation rate, phase of the rotation relative to drive signals and rotation
direction of micromachined gears. Figure 65 illustrates the feedback system design

suggested by Dickey et al. A similar mechanism can be implemented in the turn-table designs discussed in this thesis.
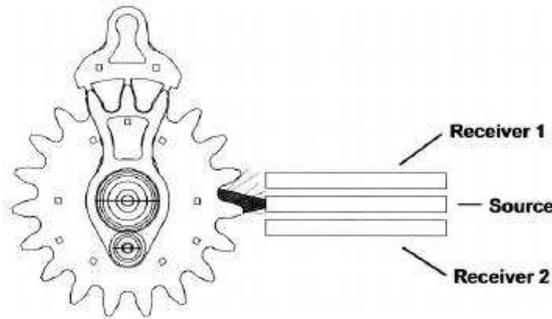
The bulk micromachined micromirrors presented here are relatively massive for the surface micromachined driving mechanism. The use of thinner wafers could significantly reduce this load. The ideal wafer thickness for the design presented here would be $185 - 190$ µm.

The current mask designs for the bulk micromachined mirror array allow only the usage of only about a third of the total wafer surface area. For production purposes, the yield of a single wafer needs to be increased by modifying the mask designs appropriately.

The optical quality of mirror fabricated by the proposed method depends largely upon the uniformity of the anisotropic etch process. Figure 66 shows the SEM micrograph of the (111) surface obtained after KOH etching. The Si (111) surface can be further improved by several means reported in literature. Addition of IPA (iso-propyl alcohol) and oxidizers, and ultrasonic agitation [59] are some of the methods that could be included in the KOH etching process described earlier to obtain smooth and defect

free mirror-like surfaces. Experiments need to be conducted to find out the optimum amount of these additives and other process parameters in order to achieve the lowest surface roughness in the anisotropic etching step.
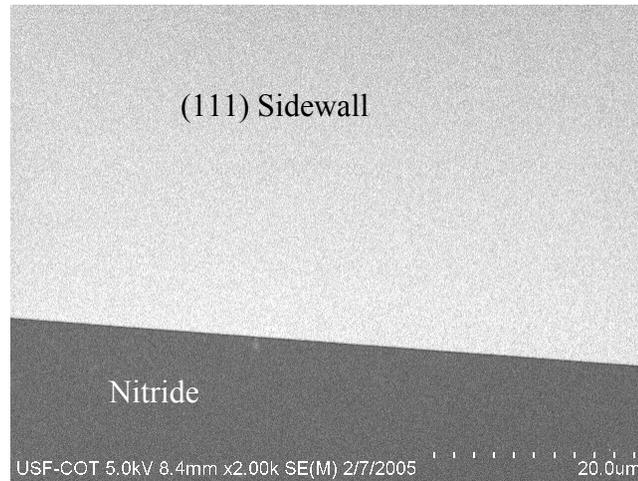


Figure 66.        V-groove sidewall surface

The V-groove mirror surface was observed (see Figure 61) to undergo damage due to the effects of DRIE etching and prolonged exposure to concentrated HF solution. The combination of these effects resulted in very rough mirror surfaces. A low surface roughness is naturally the primary requirement of any mirror surface. Therefore, some method needs to be determined for protecting the mirror surfaces during the DRIE and HF etch processes. As discussed earlier, a layer of ~2 μm thick PECVD oxide should suffice as a protective layer in the above cases. An experiment was carried out in this work in which first a PECVD oxide layer was deposited on a Si substrate and next this wafer was subjected to anodic bonding. However, the anodic bonding was not entirely successful in this case. Further experiments need to be carried out in order to determine the optimum thickness of protective PECVD oxide. Further research can also be done to

94

find any alternate material that could protect the silicon mirrors and at the same time allow anodic bonding to occur.

Figure 67 below shows the SEM image of a micromirror array fabricated in a wafer that underwent breakage during PiRL bonding. It can be seen here that the DRIE etch rate varies significantly in adjacent areas.
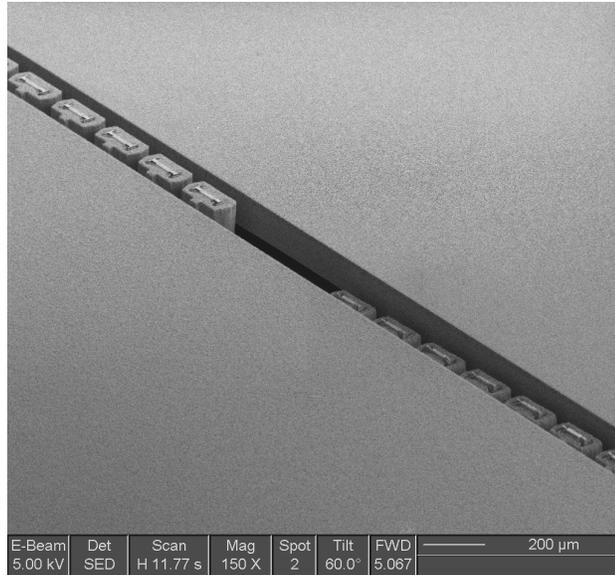


Figure 67.    Micromirror array showing uneven DRIE etch rates.

In spite of the extremely uneven etch profiles, a few good devices were found on the etched wafer (see Figure 68) in certain localized regions that were bonded properly to the Pyrex wafer. This important observation implies that PiRL bonding can be pursed as an attractive alternative to anodic bonding in the micromirror fabrication process. The behavior of thermocompression bonding using PiRL should not be affected by the deposition of any intermediate metal /dielectric layers on silicon. This feature in turn allows excellent flexibility in selecting a protective material for the silicon mirrors. The inconclusive results obtained with the PiRL bonding experimentations have been already

95

discussed in Section 3.4.1.1. Further investigation is therefore required to solve the issues associated with PiRL-Si thermocompression bonding.



| E-Beam | Det | Scan | Mag | Spot | Tilt | FWD | | 100 µm |
| 5.00 kV | SED | H 22.63 s | 654 X | 2 | 52.0° | 5.179 | 15.5um undercut | |
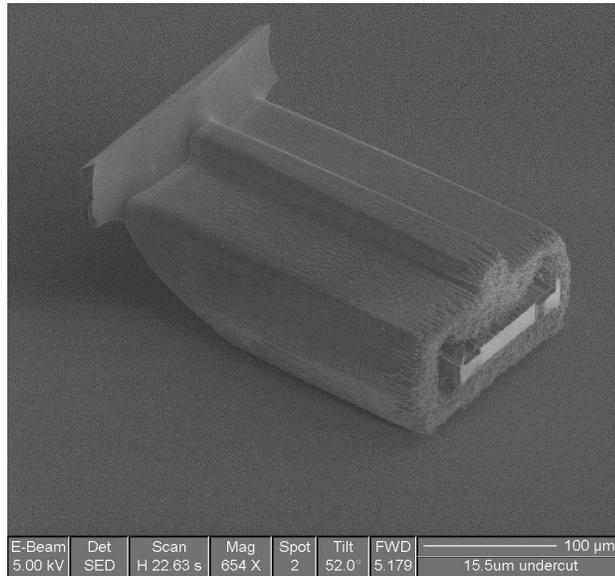
Figure 68.    Micromirror fabricated by etching PiRL bonded Si wafer.

The micromirror process flow described earlier does not include the deposition of any metal layer on the Si (111) surface. Although Si (111) plane has been employed as a mirror surface in earlier applications, the reflectivity of the mirror will certainly improve upon deposition of a suitable metal layer on the mirror [62]. Selective deposition of metal on the mirrors while avoiding the exposed [100] planes could be a problem since it is difficult to perform photolithography operations on surfaces with topology measuring hundreds of microns. A solution here could be the use of shadow masks as suggested by the work of Kim et al [63]. With the usage of shadow masks, different metal layers can be deposited for different operational wavelengths. For instance, aluminum films can be used for visible light wavelengths since it has excellent reflectivity for visible light and gold layer can be used for IR due to its excellent reflectivity in this region of the optical spectrum [64].

The various designs and fabrication process steps described in this thesis are primarily aimed at "proof-of-concept". Refined fabrication techniques and additional designs can be further investigated to optimize the micromirror device. Other potential useful applications (e.g. optical scanning, optical switching) of the re-configurable micromirror array described here can also be explored in the future.

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APPENDICES

Appendix A. Process recipes

The following is the detailed program used for carrying out anodic bonding of Silicon

and Pyrex using EVG 501 Universal Bonder.

Table 8.          Program used for anodic bonding.

| Step No. | Command | Parameter 1 | Parameter 2 |
|---|---|---|---|
| 1 | Pump on | high vacuum | 1.00 E-05 mbar |
| 2 | Wait | pressure | 1.00 E-02 mbar |
| 3 | Pump off | | |
| 4 | Purge on | | |
| 5 | Wait | time | 30 sec. |
| 6 | Purge off | | |
| 7 | Piston down | 500 N | |
| 8 | Heating | 400 °C | |
| 9 | Set temp. top | 400 °C | |
| 10 | Wait | temp. top | 400 °C |
| 11 | Wait | temp. bottom | 400 °C |
| 12 | Pump on | high vacuum | |
| 13 | Wait | pressure | 1.00 E-03 mbar |
| 14 | Voltage on | intern negative | 1000 V |
| 15 | Wait | time | 10 min. |
| 16 | Voltage off | | |
| 17 | Piston up | | |
| 18 | Cooling | 40 °C | |
| 19 | Pump off | | |
| 20 | Purge on | | |
| 21 | Wait | time | 30 sec. |
| 22 | Purge off | | |
| 23 | Wait | temp. bottom | 60 °C |

The following is the detailed program used for carrying out thermocompression bonding using PiRLIII as intermediate layer using the EVG 501 Universal Bonder.

Table 9.        Program used for thermocompression bonding using PiRLIII.

| Step No. | Command | Parameter 1 | Parameter 2 |
|---|---|---|---|
| 1 | Pump on | High vacuum | 1.0 E-05 mbar |
| 2 | Wait | Pressure | 1.0 E-02 mbar |
| 3 | Pump off | | |
| 4 | Purge on | | |
| 5 | Wait | Time | 30 sec |
| 6 | Purge off | | |
| 7 | Pump on | High vacuum | 1.0 E-05 mbar |
| 8 | Wait | Pressure | 1.0 E-02 mbar |
| 9 | Pump off | | |
| 10 | Purge on | | |
| 11 | Wait | Time | 30 sec |
| 12 | Purge off | | |
| 13 | Pump on | High vacuum | 1.0 E-05 mbar |
| 14 | Wait | Pressure | 1.0 E-02 mbar |
| 15 | Waferbow | | |
| 16 | Wait | Time | 20 sec |
| 17 | Flags out | All | |
| 18 | Piston down | 100 N | |
| 19 | Heating | 150 °C | |
| 20 | Set temp. top | 150 °C | |
| 21 | Wait | Temp. bottom | 150 °C |
| 22 | Wait | Temp. top | 150 °C |
| 23 | Wait | Time | 2 min |
| 24 | Piston down | 500 N | |
| 25 | Wait | Time | 10 min |
| 26 | Piston up | | |
| 27 | Cooling | 60 °C | |
| 28 | Pump off | | |
| 29 | Purge on | | |
| 30 | Wait | Time | 30 sec |
| 31 | Purge off | | |
| 32 | Wait | Temp. bottom | 60 °C |

The following are the process parameters used for PECVD oxide deposition.

Table 10.    PECVD oxide deposition parameters.

| Parameter | Value | Units |
|---|---|---|
| $SiH_4$ (2% in $N_2$) | 400 | sccm |
| $N_2O$ | 900 | sccm |
| Pressure | 900 | mTorr |
| Power | 25 | Watts |
| Deposition Rate | 400 | Å/min |

The following are the process parameters used for RIE etching of silicon nitride and silicon oxide thin films in the Unaxis RIE tool.

Table 11.    RIE process parameters for silicon nitride/oxide etch.

| Parameter | Value | Units |
|---|---|---|
| $CHF_3$ | 45 | sccm |
| $O_2$ | 5 | sccm |
| Pressure | 40 | mTorr |
| Power | 200 | Watts |
| DC bias | 440 | V |
| Temperature | 25 | °C |
| Etch Rate | 400 - 500 | Å/min |

The following are the process parameters used for Bosch DRIE process.

Table 12.    DRIE Bosch process parameters.

| Parameter | Deposition | Etch 'A' | Etch 'B' |
|---|---|---|---|
| Time | 5 sec | 2 sec | 6 sec |
| Pressure | 22 mT | 23 mT | 23 mT |
| $C_4F_8$ | 70 cc | 0.5 cc | 0.5 cc |
| $SF_6$ | 0.5 cc | 50 cc | 100 cc |
| Ar | 40 cc | 40 cc | 40 cc |
| RIE Power | 1 W | 9 W | 9 W |
| ICP Power | 825 W | 825 W | 825 W |

Appendix A (Continued)

The following are the process steps used for replication of chrome mask on to iron oxide photoplates.

Table 13.        Mask replication process parameters.

| No. | Process | Comment | Time |
|---|---|---|---|
| 1 | Get iron oxide photoplate | positive PR coat is already present | |
| 2 | Align with chrome mask | | |
| 3 | Expose | in EVG mask aligner | 1.8 sec |
| 4 | Develop | using developer MF319 | 40 sec |
| 5 | DI water rinse and dry | | |
| 6 | Etch iron oxide | Iron oxide etchant ($FeCl_3$+HCl+$H_2O$) | 60 sec |
| 7 | DI water rinse and dry | Clear areas should have no yellowish appearance. | |

## Appendix B. PolyMUMPs design rules

The following tables present a snapshot of the various design rules that need to be frequently referred to while designing any PolyMUMPs based device [19].

Table 14.    PolyMUMPs layer names, thicknesses, and lithography levels.

| Material Layer | Thickness (µm) | Lithography level name |
|---|---|---|
| Silicon Nitride | 0.6 | - |
| Poly 0 | 0.5 | POLY0 |
| First Oxide | 2.0 | DIMPLE ANCHOR1 |
| Poly 1 | 2.0 | POLY1 (HOLE1) |
| Second Oxide | 0.75 | POLY1_POLY2_VIA ANCHOR2 |
| Poly 2 | 1.5 | POLY2 (HOLE2) |
| Metal | 0.5 | METAL (HOLEM) |

Table 15.    PolyMUMPs masking levels.

| Mask Level Name | Field Type | Purpose |
|---|---|---|
| POLY0 | Light | Pattern ground plane |
| ANCHOR1 | Dark | Holes for Poly1 to Nitride/Poly0 connection |
| DIMPLE | Dark | Create dimples for Poly1 |
| POLY1 | Light | Pattern Poly1 |
| P1_P2_VIA | Dark | Holes for Poly1 to Poly2 connection |
| ANCHOR2 | dark | Holes for Poly2 to Nitride/Poly0 connection |
| POLY2 | light | Pattern Poly2 |
| METAL | light | Pattern Metal |
| HOLE0 | dark | Holes for Poly0 |
| HOLE1 | dark | Holes for Poly1 |
| HOLE2 | dark | Holes for Poly2 |
| HOLEM | dark | Holes for Metal |

Table 16.    Nominal and minimum features and spaces for various masking levels.

| Level Name | Nominal space | Minimum feature | Minimum space |
|---|---|---|---|
| POLY0 | 3.0 | 2.0 | 2.0 |
| DIMPLE | 3.0 | 2.0 | 3.0 |
| ANCHOR1 | 3.0 | 3.0 | 2.0 |
| POLY1 | 3.0 | 2.0 | 2.0 |
| P1_P2_VIA | 3.0 | 2.0 | 2.0 |
| ANCHOR2 | 3.0 | 3.0 | 2.0 |
| POLY2 | 3.0 | 2.0 | 2.0 |
| METAL | 3.0 | 3.0 | 3.0 |
| HOLE0 | 3.0 | 2.0 | 2.0 |
| HOLE1 | 4.0 | 3.0 | 3.0 |
| HOLE2 | 4.0 | 3.0 | 3.0 |
| HOLEM | 5.0 | 4.0 | 4.0 |

Table 17.    PolyMUMPs interlayer design rules.

| Level 1 | Level 2 | Enclose | Spacing | Cut-in | Cut-out |
|---|---|---|---|---|---|
| POLY0 | - | | | | |
| | ANCHOR1 | 4 | 4 | | |
| | POLY1 | 4 | | | |
| | ANCHOR2 | 5 | 5 | | |
| | POLY2 | 5 | | | |
| POLY1 | - | | | | |
| | POLY0 | | | | |
| | ANCHOR1 | 4 | | | |
| | ANCHOR2 | | 3 | | |
| | POLY2 | 4 | | | |
| | DIMPLE | 4 | | | |
| | POLY1_POLY2_VIA | 4 | | | |
| POLY2 | - | | | | |
| | POLY0 | | | | |
| | POLY1 | | | | |
| | VIA | 4 | 3 | 5 | 4 |
| | ANCHOR2 | 5 | | | |
| | METAL | 3 | | | |
| HOLEM | HOLE2 | 2 | | | |
| HOLE2 | HOLE1 | 2 | | | |

Creating double thickness PolyMUMPs structures

The following procedure is recommended by PolyMUMPs for designing the layout of structures having a thickness of 3.5 µm which is the sum of the thicknesses of poly1 and poly2 layers.

    i)       Draw a continuous sheet in poly1 layer.

    ii)      Draw a continuous poly1_poly2_via that encloses poly1 by 5 µm.

    iii)    Draw the poly2 structure over the poly1 sheet.

This procedure is based on the fact that an over-etch of the poly2 layer is sufficient to completely etch the underlying poly1 layer. While designing double thickness PolyMUMPs structures, care should be taken that the size of all design features is greater than 3.5 µm.