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An Implementation of the USF/ Calvo Model in Verilog-A to Enforce Charge Conservation in Applicable FET Models

Joshua Nicodemus
University of South Florida

An Implementation of the USF/ Calvo Model in Verilog-A to Enforce Charge Conservation in Applicable FET Models

by

Joshua Nicodemus

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Department of Electrical Engineering
College of Engineering
University of South Florida

Major Professor: Arthur David Snider, Ph.D.
Lawrence P. Dunleavy, Ph.D.
Thomas M. Weller, Ph.D.

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DEDICATION

To my Lord and Savior, Jesus Christ, who has kept me from falling and has given me a new purpose and meaning in my life and for whom I live.

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ABSTRACT

The primary goal of this research is to put into code a unique approach to addressing problems apparent with nonlinear FET models which were exposed by Calvo in her work in 1994. Since that time, the simulation software for which her model was appropriate underwent a significant update, necessitating the rewriting of her model code for a few applicable FET models in a 'Verilog-A,' making it more compatible with the new versions of software and simulators.

The problems addressed are the inconsistencies between the small-signal model and the corresponding large-signal models due to a factor called transcapacitance. It has been noted by several researchers that the presence of a nonlinear capacitor in a circuit model mathematically implies the existence of a parallel transcapacitor, if the value of its capacitance is a function of two bias voltages, the local and a remote voltage. As a consequence, simulating small-signal excursions with a nonlinear model produces data which are inconsistent with the simulations using the linear model, if the latter does not include the transcapacitance, which is inevitably present. The Calvo model attempted to

improve the performance of these models by modifying terms in the charge source equations which minimize these transcapacitances. Thanks to the present effort, Calvo's theory is now incorporated in the Angelov Model and can also be implemented in some other popular existing models such as Curtic, Statz and Parker Skellern models.

CHAPTER 1

INTRODUCTION

It has been noted by several researchers [1-6] that the presence of a nonlinear capacitor in a circuit model mathematically implies the existence of a parallel capacitor or 'transcapacitor', if the value of its capacitance is a function of a remote voltage. This situation occurs in common FET modeling applications. The extracted values of all three capacitances, gate-to-source, gate-to-drain and drain-to-source (C_{gs}, C_{gd} and C_{ds}) in the simplified small-signal MESFET model are functions of two voltages, local and remote voltage (usually taken to be V_{gs} which is the gate-to-source voltage and V_{ds} which is the drain-to-source voltage for the gate-to-source capacitor) and, therefore, the effects of transcapacitance must be considered. Otherwise, simulating small-signal excursions with a non-linear model may produce data that is inconsistent with the simulations of the corresponding small-signal model (associated linear model).

In the next section we will review the mathematical and physical origins of these discrepancies. The subsequent section critiques the methods usually implemented to overcome these difficulties. Finally we present the solution to the problem proposed by Calvo ; it imposes no additional complexity on the parameter extraction process, it renders the linear and nonlinear models consistent, and as seen by Calvo in her simulations, it vastly improves the convergence of the harmonic balance algorithm. This research was carried out in an attempt to put this technique into code for an already existing Angelov transistor model in a software 'Verilog-A'.

In this document, we will show the techniques that can be used to alter empirical nonlinear models of MESFETS (metal-semiconductor field-effect transistor) to improve their performance, which we document in the subsequent chapters. Broadly, models are categorized as physical models, empirical models and data based models each of which is used for different applications and has its own advantages and disadvantages [1].

We deal with empirical models in this document. Most of the traditional models referred to have similar circuit topology but differ in the analytic formulas that describe the circuit elements as functions of bias [1]. Most models work fairly well describing the performance of a device with large signals. However, implicit errors arise because of the way the nonlinear capacitors are modeled. The normal approach of modeling three nonlinear capacitances with only two elements in the nonlinear simulator forces interrelationships between the capacitances to make sure they obey charge conservation [1]. There is no certainty that the extracted capacitances will obey charge conservation at different bias values and for various devices. This ultimately causes inconsistency between the large signal and small signal models.

These discrepancies arise due to the fact that the capacitances have bivariate dependence. These capacitance values not only depend on the voltage across their own terminals but also depend on another voltage in the circuit called the remote voltage. While modeling these capacitances, another capacitive element called transcapacitance must be included in the small signal model [1]. This is the primary cause for the inconsistency between the large signal model and its corresponding small signal model. Inserting this transcapacitance in the small signal models is difficult for various reasons which will be described in the subsequent chapter. Leaving the transcapacitance out also may cause the divergence of harmonic balance as observed by Calvo: this is not dealt in this document.

Calvo formulated a mathematical solution which reduces the effects of transcapacitance immensely and virtually sets it equal to zero at the quiescent or bias point. She used the continuous bound integrals in her charge source equations extracted from capacitance equations. We take advantage of her contribution to tweak the existing charge source equations in applicable FET models and minimize the ill effects of transcapacitance. The simulating software which was being used at the time by Calvo is not being implemented as much now, necessitating the rewriting of the equations in this software ‘Verilog-A’. The latter is more simulator independent and portable which in turn makes the usability factor much higher.

In this research chose a typical case to observe how this stratagem works and to show how effective it would be with this new technique. We recode the charge source equations in the Angelov model with certain modifications in an attempt to make it more charge conservative and minimize the ill effects of transcapacitance. We ran two test cases, one with the charge model and the other being the capacitance model. We used Calvo's stratagem to modify the charge source equations in order to make the two above mentioned models perform closer to each other than they did prior to these modifications.

This technique can be applied to a lot of applicable FET models, which have their charge source equations derived from the corresponding capacitance equations. This trick can also be used to model other bivariate capacitances and bivariate inductances [1].

In the following chapter, we will show the origins of these discrepancies, followed by traditional methods which are currently being implemented to avoid this situation and the complications arising from them. Then we will present our implementation of Calvo's solution to this problem along with some simulations to check our theory.

In chapter 3 we describe the way the charge source equations are worked out from the capacitance equations and suggest how the equations in certain popular models like Angelov, Curtice, Parker-Skellern etc. can be modified to obey charge conservation. Unfortunately, there does not seem to be any other way of getting around these restrictions by measuring the combined effects of the two capacitors without much complexity. As will be shown in chapter 3, modeling elements that are functions of a remote voltage causes mathematical complications that make the large signal and small signal inconsistent. Therefore, we illustrate how Calvo's mathematical construction removes this error at the DC quiescent bias point and minimizes the associated errors as the signal swings away, ensuring better charge conservation.

Chapter 4 describes the code we modified using Calvo's strategy, which accounts for the transcapacitance by mathematically finessing the charge source equations. We describe how the modified code works in the proximity of the operating bias voltages and ensures charge conservation. Also, we document charge source equations from a few other applicable

FET models and apply our stratagem to those formulas. They now account for the ignored transcapacitance.

To test that the stratagem works we describe in chapter 5 how we simulate using the original Angelov code with small and large signals, not accounting for the transcapacitance; and we simulate using our code with the same small and a large signals accounting for those elements. We show the output curves of the revised model for both, capacitive and the charge models.

Chapter 6 concludes the document and suggests the scope of usage of this mathematical formulation in some other applicable FET models.

CHAPTER 2

DESCRIPTION OF MIRIAM CALVO'S NONLINEAR FET MODEL

A Field Effect Transistor (FET) is basically a voltage-controlled resistor, as the word "transistor" itself was derived by putting together "transfer resistor". So, a FET essentially is a three terminal device inside which the transfer of charge or current through any two nodes or terminals is controlled by the potential at the third terminal.

It has been noted by several researchers that the presence in a FET of a nonlinear capacitor in a circuit model mathematically implies the existence of a transcapacitor in parallel with the primary capacitor, if the value of the capacitance depends on a remote voltage [8].We note that a nonlinear capacitance whose value is C changes with bias and has to be interpreted as a small-signal linearization of a nonlinear charge source Q, with C as the derivative of Q with respect to the terminal voltage or local voltage or applied voltage V_1 as seen in equation 2.1:

$$dQ = C(V_1)\, dV_1 = (dQ / dV_1)\, dV_1 \tag{2.1}$$

But, if the remote voltage has an effect on C, Q automatically changes and its mathematical relationship becomes :

$$dQ = (\partial Q(V_1 , V_r) / \partial V_1)\ dV_1 + (\partial Q(V_1,V_r)/\partial V_r)\, dV_r \tag{2.2}$$

Comparing both equations we understand that the value of the capacitor has to paired with a transcapacitor C_T as written in equation 2.4.

$$C = (\partial Q\ (V_1,V_r))/\partial V_1 \tag{2.3}$$

$$C_T = (\partial Q(V_1,V_r))/ \partial V_r \quad (2.4)$$

As a consequence of this, large signal simulation of small signal excursions by various modelers yields data inconsistent with their simulations on their small signal models, if the latter do not consider the transcapacitance [8].

The "Equating mixed partial condition" by which equations (2.3) and (2.4) are interlocked to ensure charge conservation is shown below in (2.5):

$$\partial C/\partial V_r = \partial C_T/\partial V_1 \quad (2.5)$$

This means that the original capacitor should be paired with its corresponding transcapacitance delivering charge in accordance with the equation:

$$dQ_{transcap} = C_T\, dV_r \ [6] \quad (2.6a)$$

The total charge then would be equal to 'dQ' shown in equation (2.6b):

$$dQ = dQ_{cap} + dQ_{transcap} = C\, dV_1 + C_T\, dV_r \quad (2.6b)$$

Root and Hughes [9] acknowledge this inconsistency and insert the transcapacitance in their small signal models to resolve the discrepancy. However the inclusion of a transcapacitor is undesirable for the following reasons: [1]

1. The inclusion of the transcapacitance does not guarantee the improvement in the small-signal model's ability to simulate small signal performance of that device.
2. The inclusion of the transcapacitance automatically increases the complexity of the small signal model topology.
3. The values of transcapacitance can only be extracted from the small signal measurements with difficulty, using optimization codes.
4. Even under the assumption that the transcapacitance can be extracted there is no guarantee for the transcapacitance to obey charge conservation (equality of mixed partials of Q. See equation 2.5 or the compatibility condition) with its corresponding capacitance due to experimental error, and numerical smoothing as described in [16] will be needed in order to compute the values for the charge source Q.

5. (For reasons not known) previous attempts to incorporate transcapacitance seemed to confound the convergence of the harmonic balance simulation algorithm for large signals in nonlinear simulations [8].
6. Closed-form schemes for extracting element values from S-parameter measurements have not been worked out with these additional circuit elements [6].

We now wish to interject several observations concerning the need, the interpretation and the importance of the transcapacitance[6].

1. The effect of transcapacitance in every nonlinear two-voltage model is not optional but, it is an inevitable feature whether or not explicitly recognized. The math undeniably implies that the nonlinear charge source Q which depends on the local and remote voltage is governing the charge transfer according to equation 2.2 and not 2.1. Modelers do not have a choice as to whether or not to incorporate transcapacitance in their nonlinear models, as it already exists. Therefore for a linear model to be consistent with its corresponding nonlinear model which we call "mother" model, the former must incorporate the transcapacitance element.
2. Root and Hughes [9] have stated in their work that Green's theorem, when applied to the loops traversed in the (V_l, V_r) plane during an alternating current operation, implies that the net transfer of charge across the charge source per cycle need not be zero, if the mixed partial condition (2.5) is violated in the large-signal model. They term it the "violation of charge conservation" but Snider and Calvo in [6] suggest as an alternate nomenclature, "invalidation of charge as state variable," as they believe that "charge conservation" in the physics community means something different.
3. At any rate, we agree that a nonzero transfer of ΔQ (any small amount of charge) Coulombs per cycle across a MESFET gate is undesirable in a simulator, inasmuch as it is nonphysical (such behavior would more than likely drive a real transistor into cutoff or saturation.) [6].
4. A transparent physical model of a capacitance which is dependent on a remote voltage was described in [10], where the remote voltage controls a motor which

relocates a dielectric slab between the capacitor plates. The analysis reinstate the importance of the compatibility condition (2.5) for the conformity to “charge as a state variable”.

Now we would like to consider the customary small-signal model for Fig 2.1; its large-signal version appears as Fig 2.3. Fig 2.2 is the “Industry-Standard” small-signal intrinsic model for the MESFET.

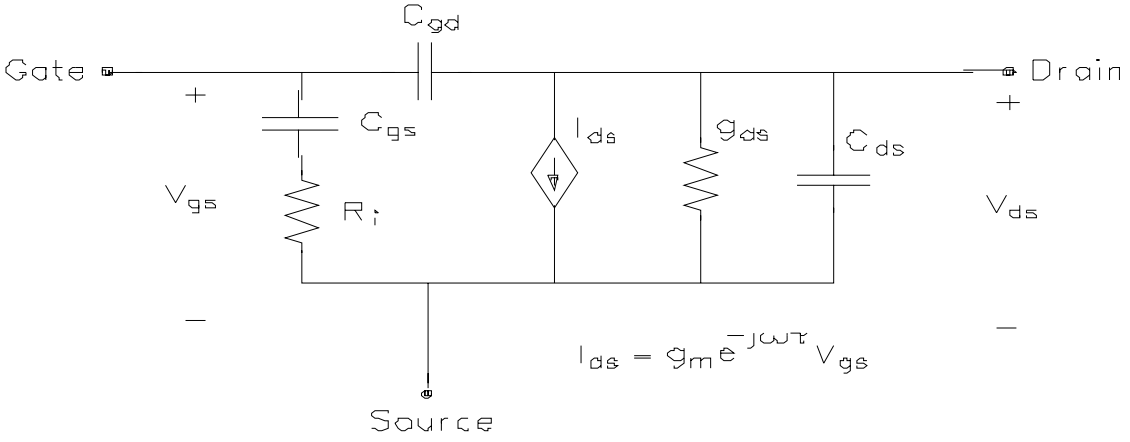

Figure 2.1 Traditional Small Signal MESFET Model (SSM) [6]

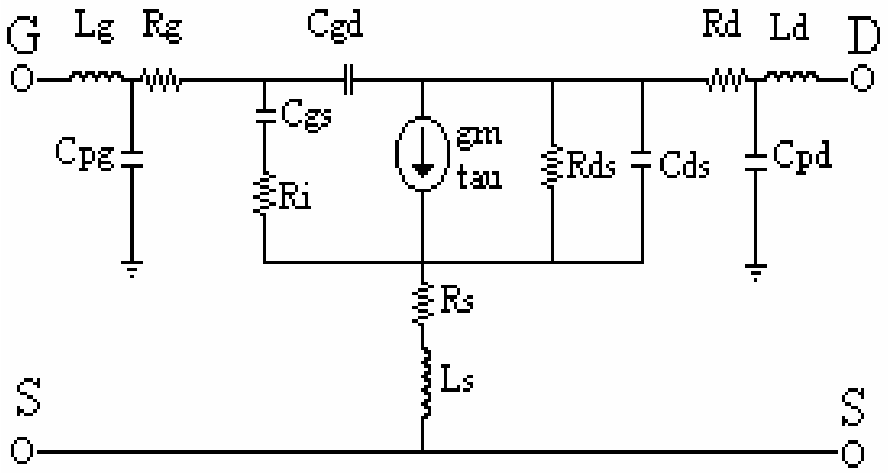

Figure 2.2 "Industry-Standard" Small Signal Intrinsic Model for the MESFET

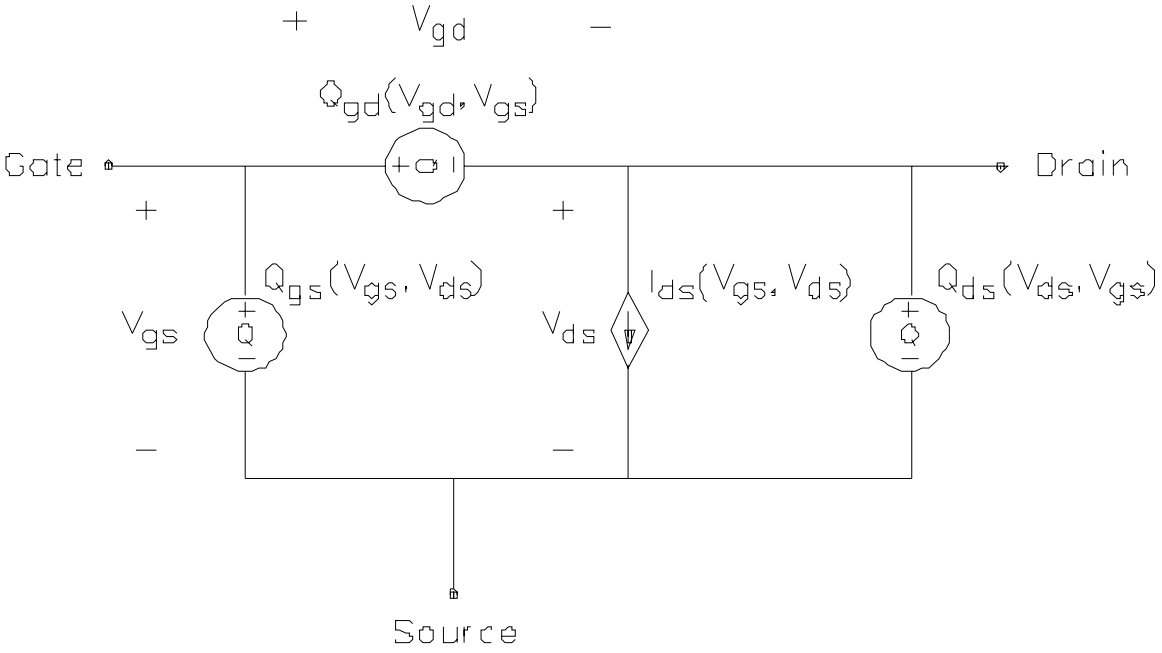

Figure 2.3 Classical Large Signal Intrinsic MESFET Model (Simplified) [6]

We shall now describe Calvo's mathematical solution for the (nonlinear) transcapacitance which renders the transcapacitance equal to zero at a selected operating

(quiescent) point. This results in the transcapacitance being negligible for moderate signal excitations therefrom (and thus validates the omission of the transcapacitance from the small-signal model, at the operating point) [8].

For this reason, we now pick a classic example from the work of Calvo and Snider [6] to show that the numerical value of the capacitance itself can differ based on what the reference remote voltage was taken to be.

We consider, for example, the gate-drain charge source in Fig. 2.3:

$$Q_{gd} = Q_{gd}\,(V_{gs}, V_{ds}) \tag{2.7}$$

For our demonstration purposes, the functional form

$$Q_{gd}\,(V_{gs},V_{ds}) = V^{m}_{gs} / V^{n}_{ds} \tag{2.8}$$

was postulated in [6,2]

Here the local voltage is:

$$V_{gd} = (V_{gs} - V_{ds}) \tag{2.9}$$

We defines V_{gs} as the remote voltage here, so the source formula (2.8) is rewritten as

$$Q_{gd}(V_l, V_r) = V_r^{m} / (V_r - V_l)^{n} \tag{2.10}$$

Therefore the equations of the capacitance and transcapacitance look like:

$$C = \partial Q_{gd} / \partial V_l = nV_r^{m} / (V_r - V_l)^{n+1} = nV_{gs}^{m} / V_{ds}^{n+1}. \tag{2.11}$$

$$C_T = \partial Q_{gd} / \partial V_r = \ldots = mV_{gs}^{m-1} / V_{ds}^{n} - nV_{gs}^{m} / V_{ds}^{n+1}. \tag{2.12}$$

On the other hand if assume V_{ds} to be the remote voltage here, the source formula (2.10) changes to the form

$$Q_{gd}(V_l, V_r) = (V_l + V_r)^{m} / V_r^{n} \tag{2.13}$$

and

$$C = \partial Q_{gd} / \partial V_l = m(V_l + V_r)^{m-1} / V_r^{n} = mV_{gs}^{m-1} / V_{ds}^{n}. \tag{2.14}$$

$$C_T = \partial Q_{gd} / \partial V_r = mV_{gs}^{m-1} V_{ds}^{n} - nV_{gs}^{m} / V_{ds}^{n+1}. \tag{2.15}$$

As we see here clearly, the numerical value of the *capacitance* has changed. Transcapacitance, too, can be shown to change by picking a different drain to source voltage.

Therefore when considering nonlinear systems controlled by two control voltages, we should not presume that the capacitance is "reality-based" and the transcapacitance as "mathematical constructed;" both of them are mathematical constructions [6].

So, we observe that the integrity of charge as a state variable depends upon equation (2.5). If the charge source given is $Q_{gd}(V_l, V_r)$, C and C_T are given by equations (2.14), (2.15); but if only C is given, the compatible C_T is only unique up to a function $f(V_r)$ of V_r [6].

OUR APPROACH IN RESOLVING THESE INCONSISTENCIES

Rather than starting from a small-signal model containing transcapacitance, our approach is to redesign the charge-source function $Q(V_l, V_r)$, mathematically, in such a way that its associated transcapacitance is negligible. (We were motivated by the observation that, since most transistor models *neglect* the transcapacitance and many of them are fairly successful, the value of C_T is probably small.) Essentially, we exploit the freedom allowed in the selection of the initial point for the integration of relation (2.5) as shown below [1,6].

Specifically, the procedure is to

1. Neglect C_T in the element extraction process and obtain values for C (and the other circuit elements) from S-parameter measurements as usual, using the model in Fig 2.1, for a number of bias voltages, local and remote voltages.
2. Curve-fit these values with any analytic function $C(V_l, V_r)$ for an applicable FET Model
3. Compute the charge source function for the large signal model according to the formula:

$$Q(V_1,V_r) = \int_{V10}^{V1} C(V_1', V_r)dV_1' \qquad (2.16)$$

where V_{l0} is the value of the *local* voltage at the terminals of the desired capacitor when the FET is biased at the quiescent (operating) point.

Note that the measured values of the capacitance $C(V_l, V_r)$ are recovered exactly; (2.16) implies (2.3). The transcapacitance is derived from (2.4):

$$C_T(V_1, V_r) = \int_{V10}^{V1} [\partial C(V_1', V_r) / \partial V_r] \, d V_1' \qquad (2.17)$$

The resulting linear model is then that of Fig. 3, with the transcapacitance values calculated from (2.17) and the other element values unaltered from their prior determination via 1 or 2.

The merits of this procedure[1,6]:

1. Since the constant of integration in the integral for Q has no effect on the circuit (it corresponds to charge transferred prior to initialization), we are free to set the lower limit in equation 2.16 arbitrarily. Many authors take it to be zero. But note that with the choice V_{l0}, we ensure that Q is very small; compare

$$Q(V_1, V_r) = \int_{V10}^{V1} C(V_1', V_r) dV_1' = O(V_1 - V_{10}) = O(\delta V_1) \quad (2.18)$$

But $$Q(V_1, V_r) = \int_{0}^{V1} C(V_1', V_r)\, dV_1' = O(V_1) \quad (2.19)$$

More importantly, the resulting numerical value of the transcapacitance (2.17) is also $O(\delta V_l)$ and very small (zero, in fact, at the quiescent point). Thus the small-signal models of Figs. 1 and 3 are nearly the same. This is the justification for neglecting transcapacitance in the initial element-extraction process [6].

2. Since the identities (2.3, 2.4) are valid, the compatibility condition (2.5) is now met *exactly*. Thus charge will be a genuine state variable ("charge conservation") in the linearized model of Fig. 2.3, and consequently very nearly so in Fig. 2.1 [6].

3. Because the transcapacitance is small, the charge transferred by it ($\delta Q = C_T \ \delta V_r$) is extremely small - of order $O(\delta V_l \ \delta V_r)$. Apparently this mollifies the deleterious effect of transcapacitance on the harmonic balance algorithm [1].

In short we have constructed, from our presumed linear (small-signal, transcapacitance-free) model, a nonlinear "mother" model which imposes negligible transcapacitance on its linearization and is thus (nearly) consistent with the presumed linear model.

To check our theory, we simulated the responses of Angelov model to the same stimulus - first a small signal input with the original charge and capacitance models, and then replacing his charge source equations with our new equations, we repeated the same simulations.

CHAPTER 3

CAPACITANCE AND CHARGE SOURCE EQUATIONS FOR A CLASSIC NONLINEAR FET MODEL

To confirm this theory, Calvo and Snider in one of their earlier works simulated responses for three models to the same small signal stimulus input. The first was a linear model shown in Fig 3.3. The second model was the associated nonlinear model shown in Fig 3.4 constructed from its corresponding linear model using charge source equations described in the previous chapter. The third model was the associated nonlinear model constructed in the customary manner [4].

The values for C_{gs} and C_{gd} are consistent with typical graphs presented in some classic MESFET models earlier. The value of C_{ds} is rarely discussed in the literature and is usually assumed to be constant [5].

Expressions have been published to describe C_{gs} and C_{gd} as functions of bias voltages by various authors. However, these formulas have poles and/or singularities that can thwart the convergence of harmonic balance simulators discussed by Calvo and Snider in work which is not dealt in this document [5]. The formulas presented herein are bounded, continuous, differentiable, and integrable, so they can readily be adapted to accommodate nonlinear transcapacitance and charge source formulations [1, 4, 6]. Every term in these formulas described below is designed to control a particular behavior/pattern in the curves. We would like to mention that the parameters in these equations are not the same for all the subsequent equations; that is to say, the parameter *a* in the first set of equations is different from the second and so on.

3.1 Capacitance Equations [5]

The C_{gs} formula for the gate-source capacitance as a function of the bias voltages is:

$$C_{gs}(V_{gs}, V_{ds}) = d + c\, e^{bVgs}\ (1 + \tanh(a\, V_{ds})) \tag{3.1}$$

The parameters {a,b,c,d} therein should be fitted to data using one of the standard procedures, such as least-squares. However, values can be extracted using as few as four measurements.

Both the extracted and optimized formulas were plotted with the data in Calvo's work [1, 6].

The C_{gd} formula for the gate-drain capacitance is:

$$C_{gd}(Vgs, V_{ds}) = a + [e + b\,\mathrm{sech}(dV_{gs})][1/\sqrt{(1 + c\, e^{f Vgs}\, V_{ds}^2)}] \tag{3.2}$$

The 6 parameters in the formula can be extracted from the values of C_{gd} measured at the six bias voltages). Curves for these "extracted" values, and subsequently "optimized" values, were displayed in their work in [5].

The C_{ds} formula in the equation (3.3) is the drain-source capacitance.

$$C_{ds}(V_{gs}, V_{ds}) = f + c\,\mathrm{sech}(eV_{gs}) + a\,\mathrm{sech}(dV_{gs})\,\mathrm{sech}(bV_{ds}) \tag{3.3}$$

The six parameters in this formula can be obtained from the measured values at six bias points [5].

3.2 Charge Source Equations [5]

Their corresponding charge source equations for these capacitances are :

$$Q_{gs} = d\,[V_{gs} - V_{gs0}] + (c/d)\,[1 + \tanh(a\, V_{ds})][e^{bVgs} - e^{bVgs0}] \tag{3.4}$$

$$Q_{gd} = a\,[V_{gs} - V_{gs0} - V_{ds} + V_{ds0}] + [(e + b\,\mathrm{sech}\, dV_{gs}) / \sqrt{c e^{f Vgs/2}}]\,.$$
$$\ln[(\sqrt{c}\ e^{Vgs/2} V_{ds} + \sqrt{1+ce^{fVgs}\, V_{ds}^2}) / (\sqrt{c}\ e^{fVgs/2}(V_{ds0} - V_{gs} + V_{gs0}) + \sqrt{(1+ ce^{fVgs}(V_{ds0} - V_{gs} + V_{gs0})^2} \tag{3.5}$$

$$Q_{ds} = [f + c\,\mathrm{sech}(eV_{gs})][V_{ds} - V_{ds0}] + (a/b)\,\mathrm{sech}(dV_{gs})[\arctan(\sinh bV_{ds}) - \arctan(\sinh b\, V_{ds0})] \tag{3.6}$$

These equations are referenced with V_{gs} as the remote voltage. The input signal here was biased at the quiescent point while computing the charge function Q. It was

demonstrated earlier by Calvo and Snider in [6] that the large signal models tracked the small signal models fairly accurately, in contrast to the other models which showed discrepancy. Also, when the input bias voltage swayed away even by about 33.3% the above model showed a lot more accuracy than the other models under test then.

A simple figure for a Bias Dependent Charge Source and a Bias Dependent Capacitance are depicted in Figs 3.1 and 3.2 to help the reader visualize better.

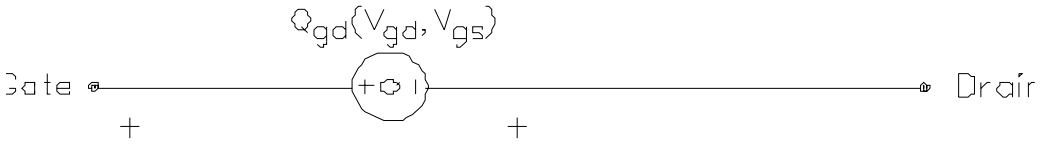

Figure 3.1 Bias Dependent Charge Source

Figure 3.2 Bias Dependent Capacitance

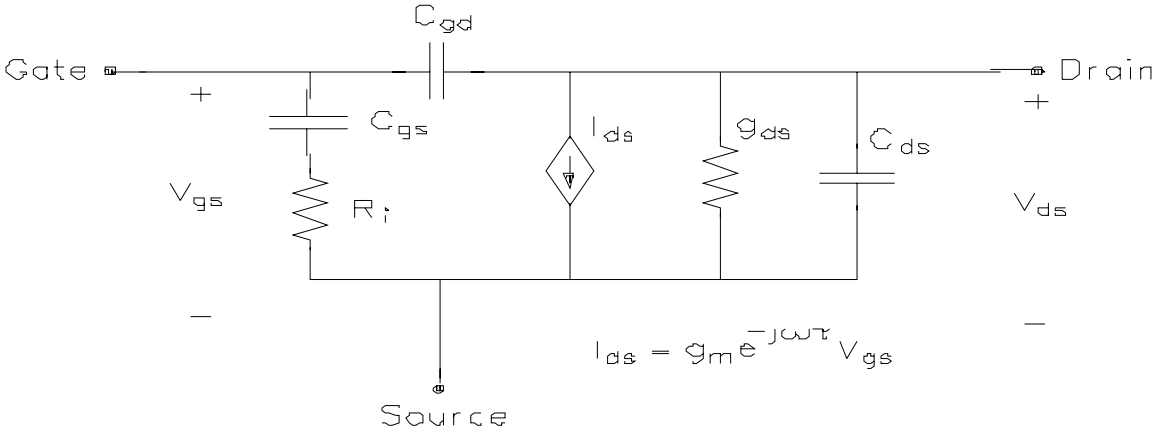

Figure 3.3 Classical Small Signal MESFET Model [6]

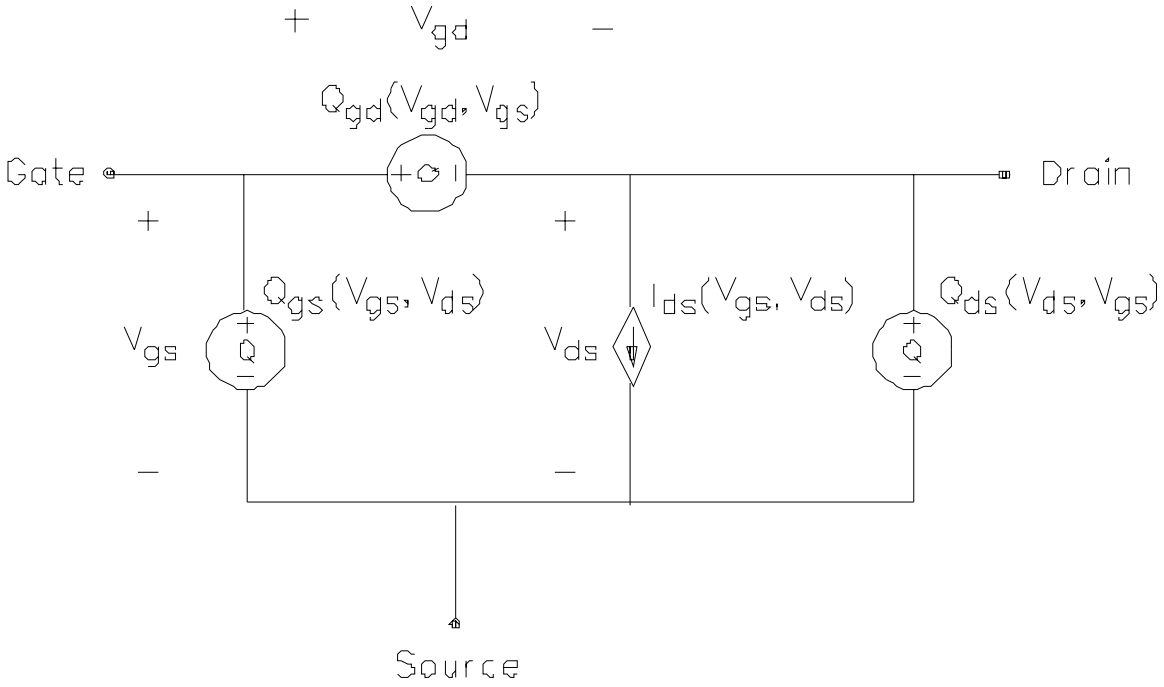

Figure 3.4 Classical Large Signal MESFET Model [6]

CHAPTER 4

CODE DESCRIPTION

We begin by taking a different stand on compatibility condition for charge conservation from the one used by Angelov in his GaAs FET model in [11]. We advocate using Calvo's cross partial compatibility equation as stated in equation (4.2) instead of the mixed partial condition shown in equation (4.1) considered by Angelov. We base our stand on the explanation in chapter 2.

$$\partial C_{gd} / \partial V_{gs} = \partial C_{gs} / \partial V_{dg} \tag{4.1}$$

$$\partial C_{gs} / \partial V_{gd} = \partial C^{T}_{gs} / \partial V_{gs} \tag{4.2}$$

where C_{gs} is be the gate-to-source capacitance, V_{gd} is gate-to-drain voltage, V_{gs} is gate-to-source voltage and C^{T}_{gs} is transcapacitance from gate-to-source.

To ensure charge conservation (or, rather, to avoid invalidation of charge as a state variable) we modified Angelov's charge source equations, as extracted from his corresponding capacitance equations. Thus we account for the transcapacitance but ensure that it is negligible in the small signal model, and in fact would be zero at the quiescent bias point (as explained in the earlier chapters).

Following Calvo's logic, we re-set the lower limit of the integral in the charge source formula equal to the local bias voltage of the capacitor in equations 4.9 and 4.10, when the input signal of the FET was biased at the operating point. Angelov in his work takes the lower limit to be zero. But note that, with the choice V_{l0} (local bias voltage) as the lower limit of integration, we ensure that Q is very small as seen earlier in (2.18) and (2.19).

We display our new charge source equations in (4.7) and (4.8) below, as we incorporated them into the Angelov's code. The details of their calculations follow.

The capacitance and charge source equations documented below are taken from Angelov's work in his GaAs FET model [11]

$$C_{gs} = C_{gsp} + C_{gs0} \bullet (1 + \tanh [P_{10} + P_{11} \bullet V_{gs}]) \bullet (1 + \tanh [P_{20} + P_{21} \bullet V_{gs}]) \quad (4.3)$$

$$C_{gd} = C_{gdp} + C_{gd0} \bullet (1+ \tanh [P_{30} + P_{31} \bullet V_{ds}]) \bullet (1-\tanh [P_{40} + P_{41} \bullet V_{dg}]) \quad (4.4)$$

Here $P_{10}, P_{11}, P_{20}, P_{21}, P_{30}, P_{31}, P_{40}, P_{41}$ are parameters defined by Angelov.

We used values for these parameters supplied by Clausen.

The indefinite integrals of the capacitances in (4.3, 4.4) are read off from Angelov's code where V_{gs} and V_{gd} respectively were the terminal voltages to which these capacitances have been integrated (or, was set as the upper limit of integration).

$$Q_{gs} = \int [C_{gs} (V_{gs}, V_{ds}) dV_{gs}]$$

$$= C_{gsp} \bullet V_{gs} + C_{gs0} \bullet (V_{gs} + (\log [\cosh [P_{10} + P_{11} V_{gs}]]) / P_{11} + V_{gs} \bullet \tanh [P_{20} + P_{21} V_{ds}] + (\log [\cosh [P_{10} + P_{11} V_{gs}]] \bullet \tanh [P_{20} + P_{21} V_{ds}]) / P_{11}) \quad (4.5)$$

$$Q_{gd} = \int [C_{gd} (V_{gs}, V_{gd}) dV_{gd}]$$

$$= C_{gsp} \bullet V_{gd} + C_{gd0} \bullet (V_{gd} + (\log [\cosh P_{40} + P_{41} V_{gd}]) / P_{41} + V_{gd} \bullet \tanh [P_{30} + P_{31} V_{ds}] + (\log [\cosh [P_{40} + P_{41 V_{gs}}]] \bullet \tanh [P_{30} + P_{31} V_{ds}]) / P_{41} \quad (4.6)$$

Our new charge source equations for gate-to-source and gate-to-drain are then given by:

$$Q_{gs} = \int [C_{gs} (V_{gs}, V_{ds}) dV_{gs}] \text{ integrated from } V_{gs0} \text{ through } V_{gs}$$

$$= C_{gsp} \cdot V_{gs} + C_{gs0} \cdot (V_{gs} + (\log [\cosh [P_{10} + P_{11} V_{gs}]]) / P_{11} + V_{gs} \cdot \tanh [P_{20} + P_{21} V_{ds}] + (\log [\cosh [P_{10} + P_{11} V_{gs}]] \cdot \tanh [P_{20} + P_{21} V_{ds}]) / P_{11})$$

$$- C_{gsp} \cdot V_{gs0} + C_{gs0} \cdot (V_{gs0} + (\log [\cosh [P_{10} + P_{11} V_{gs0}]]) / P_{11} + V_{gs0} \cdot \tanh [P_{20} + P_{21} V_{ds}] + (\log [\cosh [P_{10} + P_{11} V_{gs0}]] \cdot \tanh [P_{20} + P_{21} V_{ds}]) / P_{11}) \quad (4.7)$$

$$Q_{gd} = \int [C_{gd} (V_{gs}, V_{gd}) dV_{gd}] \text{ integrated from } V_{gd0} \text{ through } V_{gd}$$

$$= C_{gsp} \cdot V_{gd} + C_{gd0} \cdot (V_{gd} + (\log [\cosh P_{40} + P_{41} V_{gd}]) / P_{41} + V_{gd} \cdot \tanh [P_{30} + P_{31} V_{ds}]$$
$$+ (\log [\cosh[P_{40} + P_{41 V_{gs}}]] \cdot \tanh [P_{30} + P_{31} V_{ds}]) / P_{41}$$
$$- C_{gsp} \cdot V_{gd0} + C_{gd0} \cdot (V_{gd0} + (\log [\cosh P_{40} + P_{41} V_{gd0}]) / P_{41} + V_{gd0} \cdot \tanh [P_{30} + P_{31} V_{ds}]$$
$$+ (\log [\cosh[P_{40} + P_{41 V_{gd0}}]] \cdot \tanh [P_{30} + P_{31} V_{ds}]) / P_{41} \quad (4.8)$$

Here V_{gs0} and V_{gd0} are the local bias voltages (which were set as the lower limit of integration) at the capacitor terminals V_{gs0} and V_{gd0} were set to -0.25V and -3.25V in accordance with the equation (4.9) where V_{ds0} was a known value and the value of V_{gd0} was read off from an Angelov output.

$$V_{gs0} = V_{gd0} + V_{ds0} \quad (4.9)$$

The simulation results are shown in following chapter. Regretably, due to time limitations we did not find an ideal test case in which our model outperformed the original Angelov model but our model was able to produce comparable results.

This technique is immediately adaptable for other applicable FET models whose charge source equations have been extracted from their corresponding capacitance equations. The existing charge source formulas have to be diminished by the same formula with all the terminal voltage values replaced by the local bias voltage values. This should help minimize the ill effects of ignoring transcapacitance and charge conservation.

Another advantage of this method is that it does not require any new parameter extraction (as would be the case if transcapacitance has to be estimated in the small signal model).

A few examples to which this technique can be adapted are documented below but were not coded.

In the normal operating mode of a FET in Parker-Skellern model in [12], the charge source equation from gate-to-source is (4.10):

$$Q_{gs} = 2C_{gs} \Phi (1-\sqrt{} (1-V_{gs}/ \Phi) + C_{gd} . V_{gd} \quad (4.10)$$

Our stratagem when applied to this gate-to-source charge equation would result in equation (4.11).

$$Q_{gsNEW} = 2C_{gs}\,\Phi\,(1-\sqrt{}\,(1-V_{gs}/\,\Phi) + C_{gd}\,.V_{gd}$$

$$- 2C_{gs}\,\Phi\,(1-\sqrt{}\,(1-V_{gs}/\,\Phi) - C_{gd}\,.V_{gd}$$

$$= 2C_{gs}\,\Phi\,(-\sqrt{}\,(1-V_{gs}/\,\Phi + \sqrt{}\,(1-V_{gs0}/\,\Phi) \qquad (4.11)$$

where 'V_{gs0}' is the local bias voltage at that capacitor terminal. It appears that Parker and Skellern formed (4.10) by integrating a *univariate* capacitance formula, which did not require transcapacitance, followed by artificially introducing a transcapacitance equal to the gate-to-drain capacitance. The disappearance of the transcapacitance in this case will be discussed in another paper.

The charge source equation for a FET in the Parker-Skellern model in [12] *when forward biased* is (4.12).

$$Q_{gs} = C_{gs}\,\Phi\{2\,(1-\sqrt{}(1-F_c) + (V_{gs0}/\Phi - F_c)^2 / (4(1-F_c)^{3/2}) + (V_{gs0}/\Phi-F_c)/\sqrt{}(1-F_c)\} + C_{gd}\,.V_{gd} \qquad (4.12)$$

Our modification when applied to equation (4.12) would change shape to (4.13), accounting for the ignored transcapacitance.

$$Q_{gsNEW} = C_{gs}\Phi\{2(1-\sqrt{}(1-F_c) + (V_{gs}/\Phi-F_c)^2/(4(1-F_c)^{3/2}) + (V_{gs}/\Phi-F_c)/\sqrt{}(1-F_c)\} + C_{gd}\,.V_{gd}$$

$$- [C_{gs}\Phi\{2(1-\sqrt{}(1-F_c) + (V_{gs0}/\,\Phi- F_c)^2/(4(1-F_c)^{3/2}) + (V_{gs0}/\Phi-F_c)/\sqrt{}(1-F_c)\} + C_{gd}\,.V_{gd}\,]$$

$$= C_{gs}\Phi\ \{\ (V_{gs}/\Phi-F_c)^2/(4(1-F_c)^{3/2}) + (V_{gs}/\Phi-F_c)/\sqrt{}(1-F_c) - (V_{gs0}/\,\Phi- F_c)^2/(4(1-F_c)^{3/2}) +$$

$$(V_{gs0}/\Phi-F_c)/\sqrt{}(1-F_c)\} \qquad (4.13)$$

We next consider a charge source equation (4.14) from gate-to-drain extracted from its corresponding charge equation in the Curtice model taken from [14,15].

$$Q_{gd} = Cgd0\,/\,\sqrt{}(1-(\,V_{ds}/\,V_{B1}))\,.V_{gd} \qquad (4.14)$$

Using our stratagem, this equation can be modified as shown in (4.15) so that the transcapacitance is accounted for.

$$Q_{gdNEW} = Cgd0\,/\,\sqrt{}\,(1-(V_{ds}/\,V_{B1}))\,.V_{gd}$$

$$- [Cgd0\,/\,\sqrt{}\,(1-(\,V_{ds}/\,V_{B1}))\,.V_{gd0}] \qquad (4.15)$$

The charge source equations for gate-to-source and gate-to-drain used in the Chlamers MESFET Model described in [15] are shown below:

$$Q_{gs} = C_{gsp} \cdot V_{gs} + C_{gs0} \cdot (V_{gs} + (\ln [\cosh [P_{10} + P_{11}V_{gs}]]) / P_{11}) \cdot (1 + \tanh [P_{20} + P_{21}V_{ds}] - C_{gs0} [\ln [\cosh (P_{10} (1+ \tanh P_{20}))]] / P_{11} \quad (4.16)$$

$$Q_{gd} = C_{gdp} \cdot V_{gd} + C_{gd0} \cdot (V_{gd} + P_{400} (\ln [\cosh [P_{40} + P_{11}V_{gd}]]) / P_{41}) \cdot (1 + \tanh [P_{30} + P_{31}V_{gs}]) - (C_{gd0} P_{400} [\ln [\cosh (P_{40} (1+ \tanh P_{30}))]]) / P_{41} \quad (4.17)$$

Where P_{10}, $P_{11,}$ P_{20}, P_{21} etc.. are polynomial coefficient parameters for the capacitances described in [15].

Charge source equations after modification using our stratagem are shown in (4.18) and (4.19).

$$Q_{gsNEW} = C_{gsp} \cdot V_{gs} + C_{gs0} \cdot (V_{gs} + (\ln [\cosh [P_{10} + P_{11}V_{gs}]]) / P_{11}) \cdot (1 + \tanh [P_{20} + P_{21}V_{ds}] - C_{gs0} [\ln [\cosh (P_{10} (+ \tanh P_{20}))]] / P_{11} - [C_{gsp} \cdot V_{gs0} + C_{gs0} \cdot (V_{gs0} + (\ln [\cosh [P_{10} + P_{11}V_{gs0}]]) / P_{11}) \cdot (1 + \tanh [P_{20} + P_{21}V_{ds}] - C_{gs0} [\ln [\cosh (P_{10}(1+ \tanh P_{20}))]] / P_{11}] \quad (4.18)$$

$$Q_{gdNEW} = C_{gdp} \cdot V_{gd} + C_{gd0} \cdot (V_{gd} + P_{400} (\ln [\cosh [P_{40} + P_{11}V_{gd}]]) / P_{41}) \cdot (1 + \tanh [P_{30} + P_{31}V_{gs}]) - (C_{gd0} P_{400} [\ln [\cosh (P_{40} (1+ \tanh P_{30}))]]) / P_{41} - [C_{gdp} \cdot V_{gd0} + C_{gd0} \cdot (V_{gd0} + P_{400} (\ln [\cosh [P_{40} + P_{11}V_{gd0}]]) / P_{41}) \cdot (1 + \tanh [P_{30} + P_{31}V_{gs}]) - (C_{gd0} . P_{400} [\ln [\cosh (P_{40} (1+ \tanh P_{30}))]]) / P_{41}] \quad (4.19)$$

CHAPTER 5

SIMULATION RESULTS

We picked our output curves shown below based on the fact that Calvo had used the same outputs to test her Transcapacitance theory. In section 5.1 we show the output curves for the Angelov capacitance model. For the simulations we ran, transcapacitance was not crucial and hence the outputs did not differ but were comparable throughout.

5.1 Angelov Model Simulations for the Capacitance Model

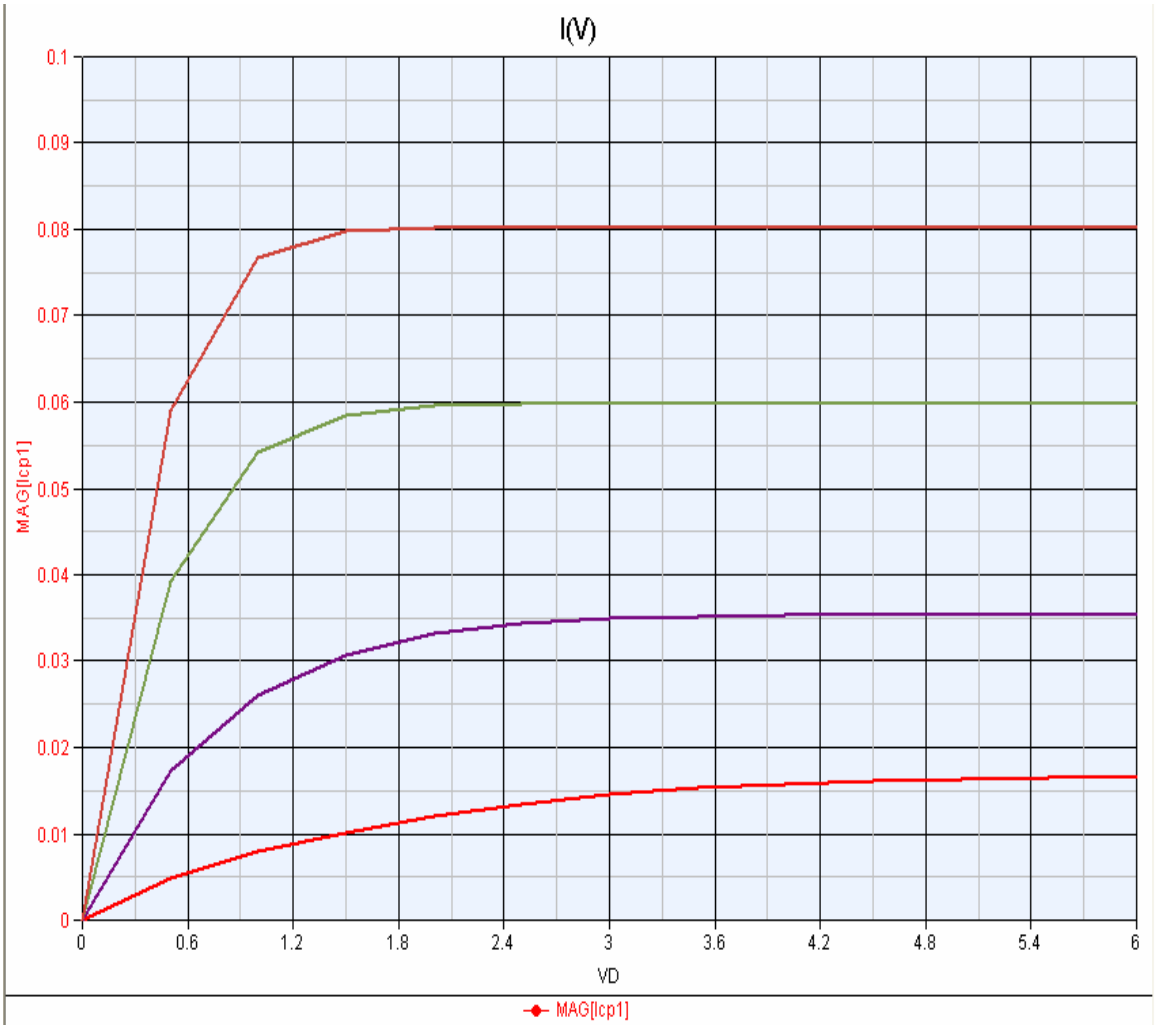

Figure 5.1 I-V Curves for a GaAs Angelov MESFET Model

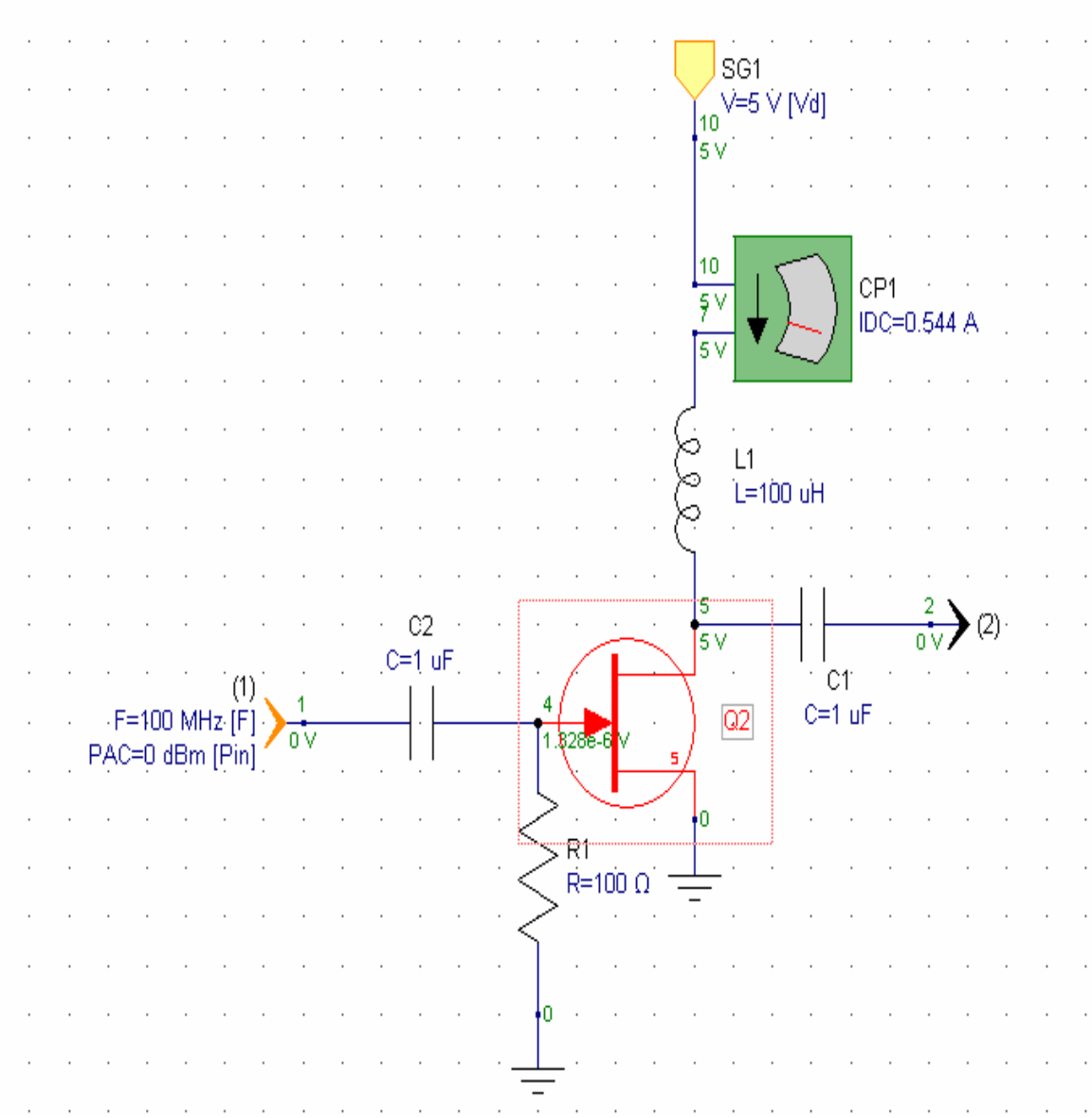

Figure 5.2 Schematic for a GaAs Angelov MESFET Model

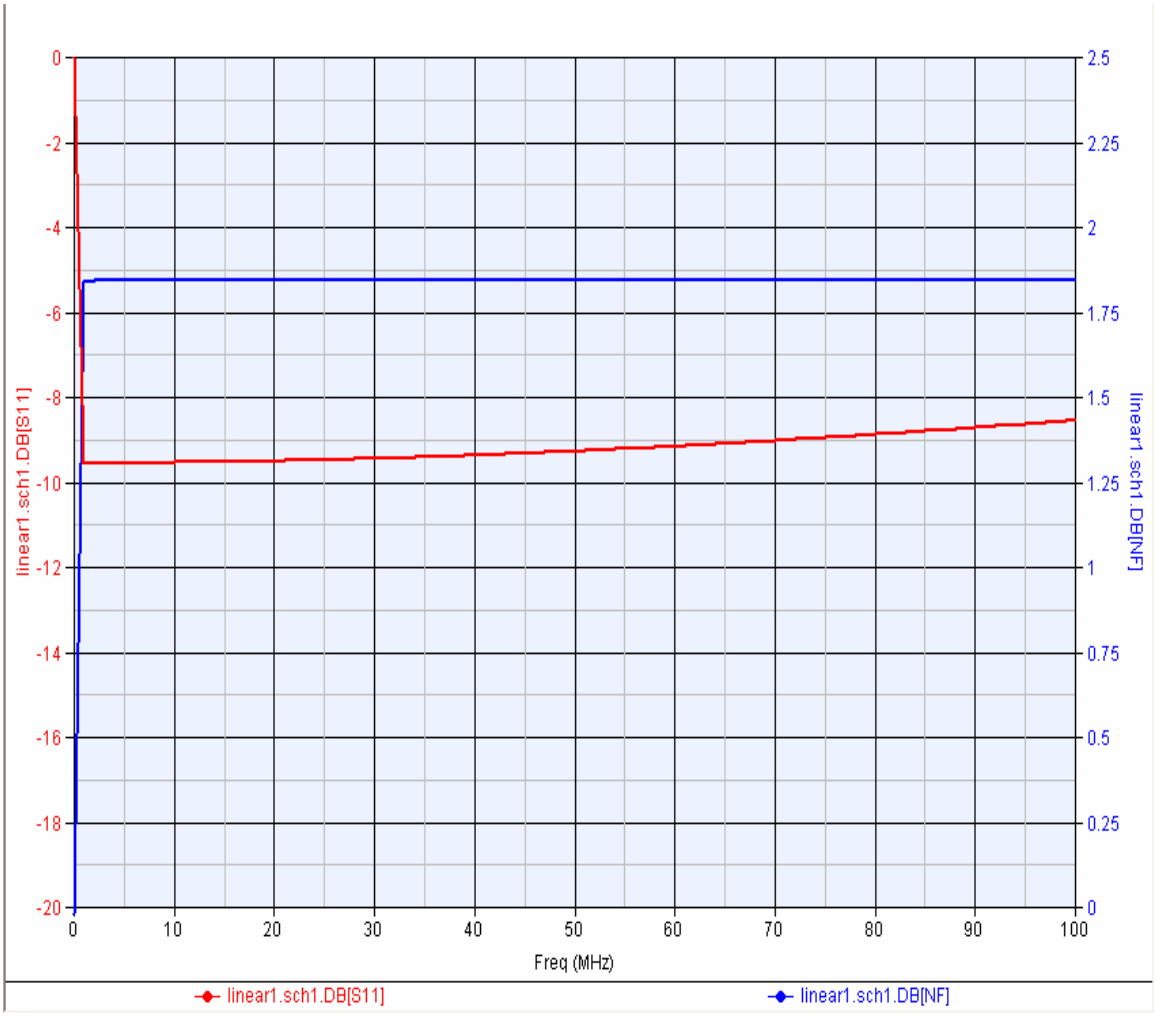

Figure 5.3 S11 & NF Graph for a GaAs Angelov MESFET Capacitance Model

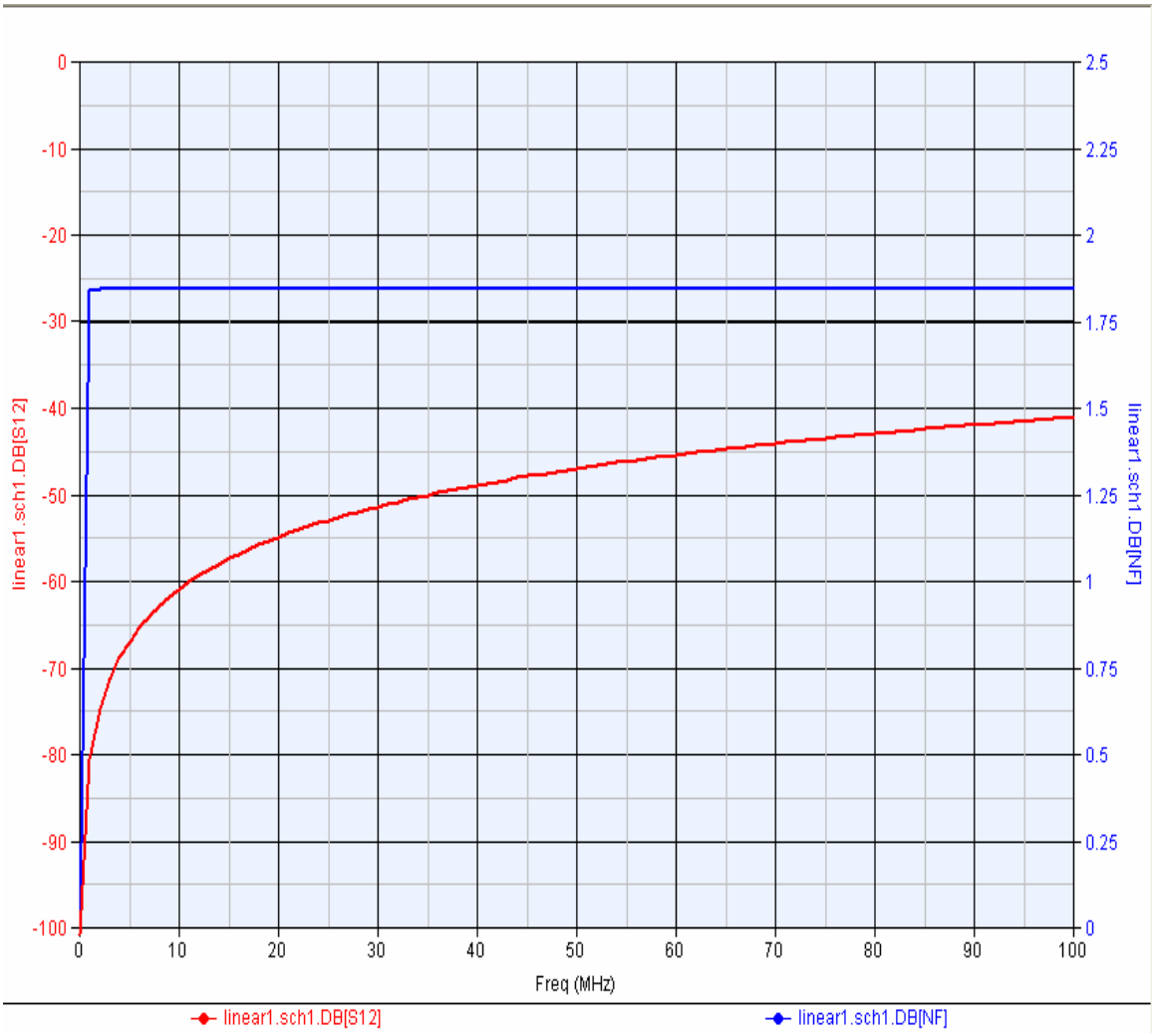

Figure 5.4 S12 & NF Graph for a GaAs Angelov MESFET Capacitance Model

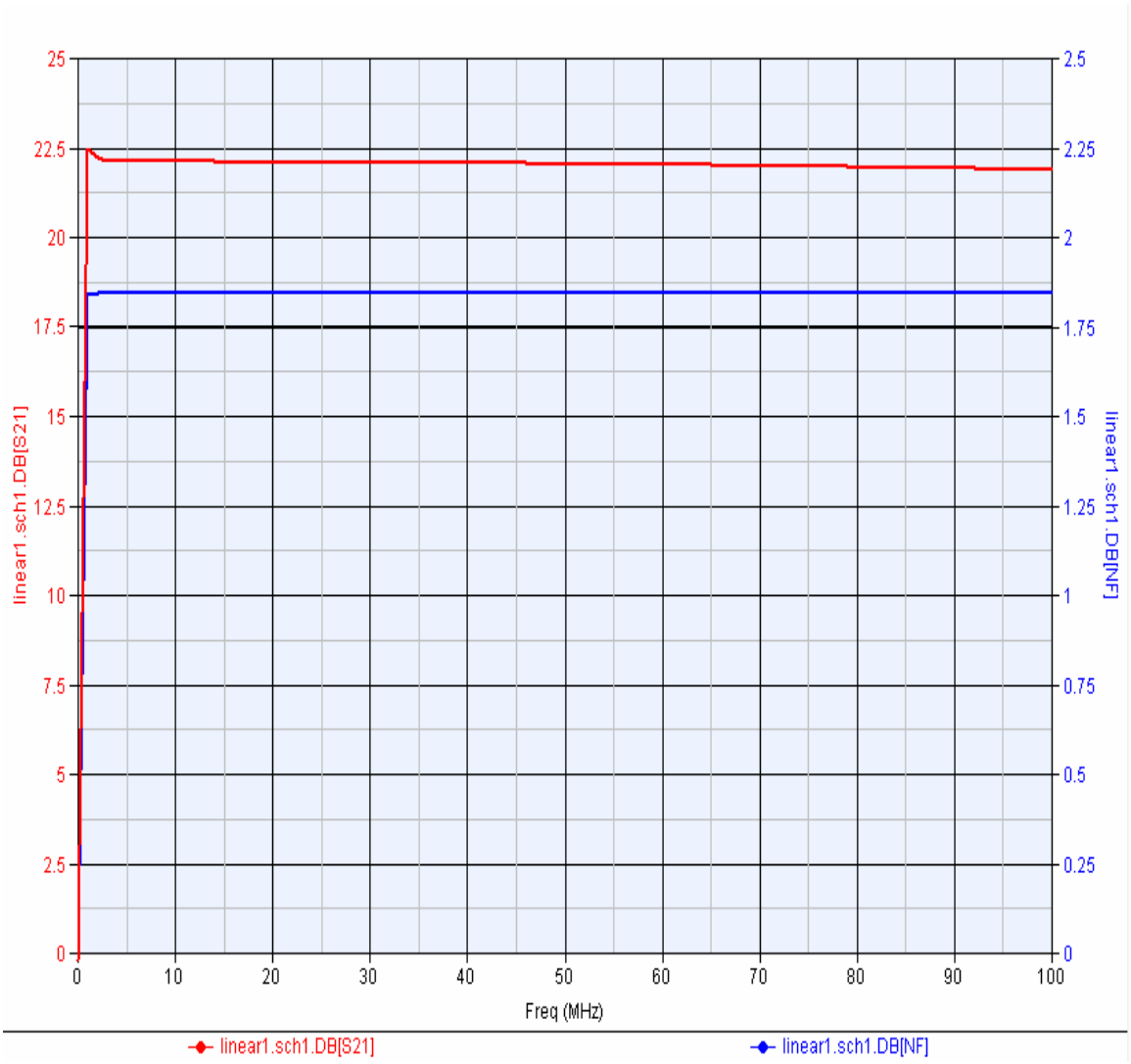

Figure 5.5 S21 & NF Graph for a GaAs Angelov MESFET Capacitance Model

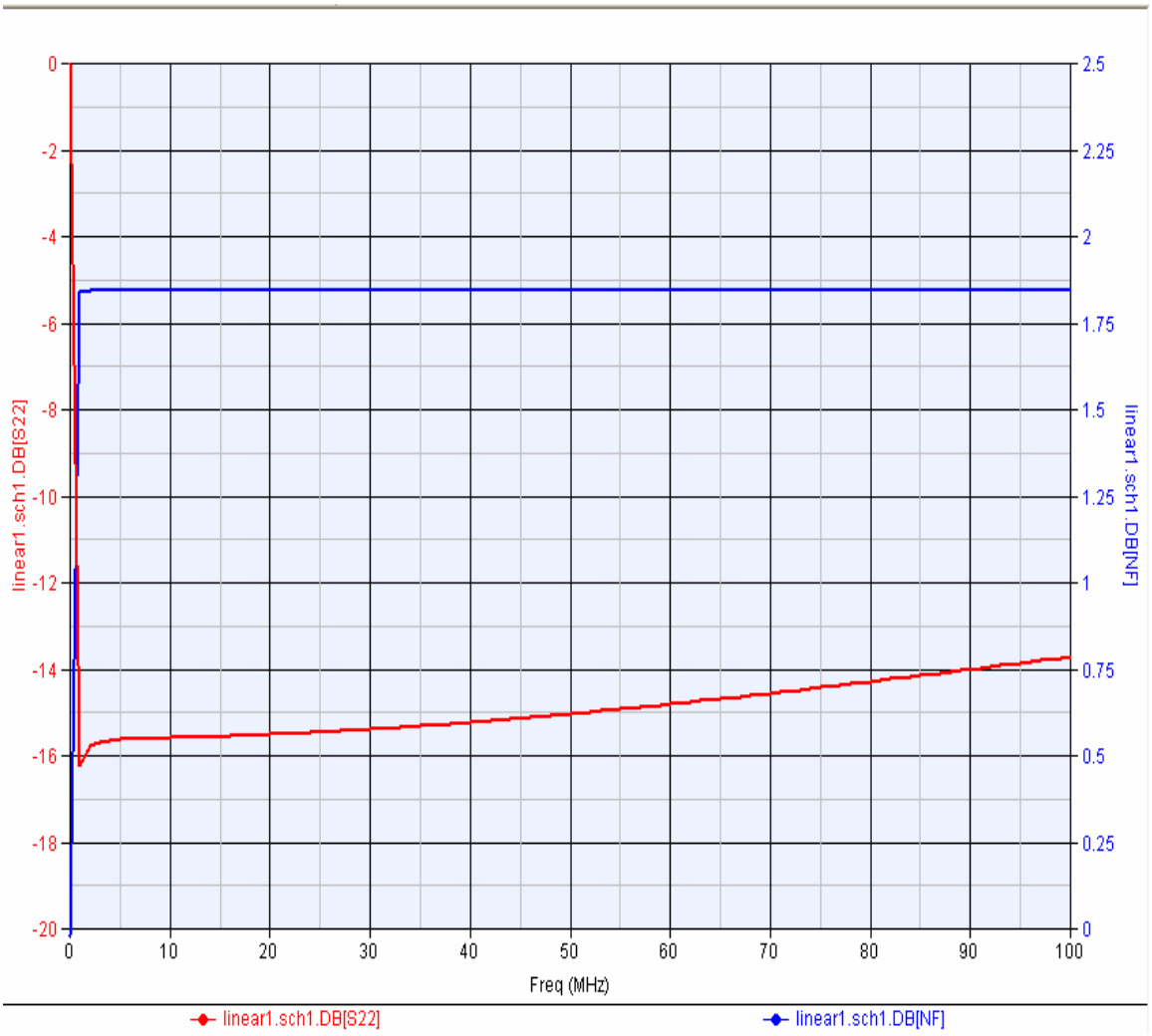

Figure 5.6 S22 & NF Graph for a GaAs Angelov MESFET Capacitance Model

5.2 Angelov Model Simulations for the Charge Model

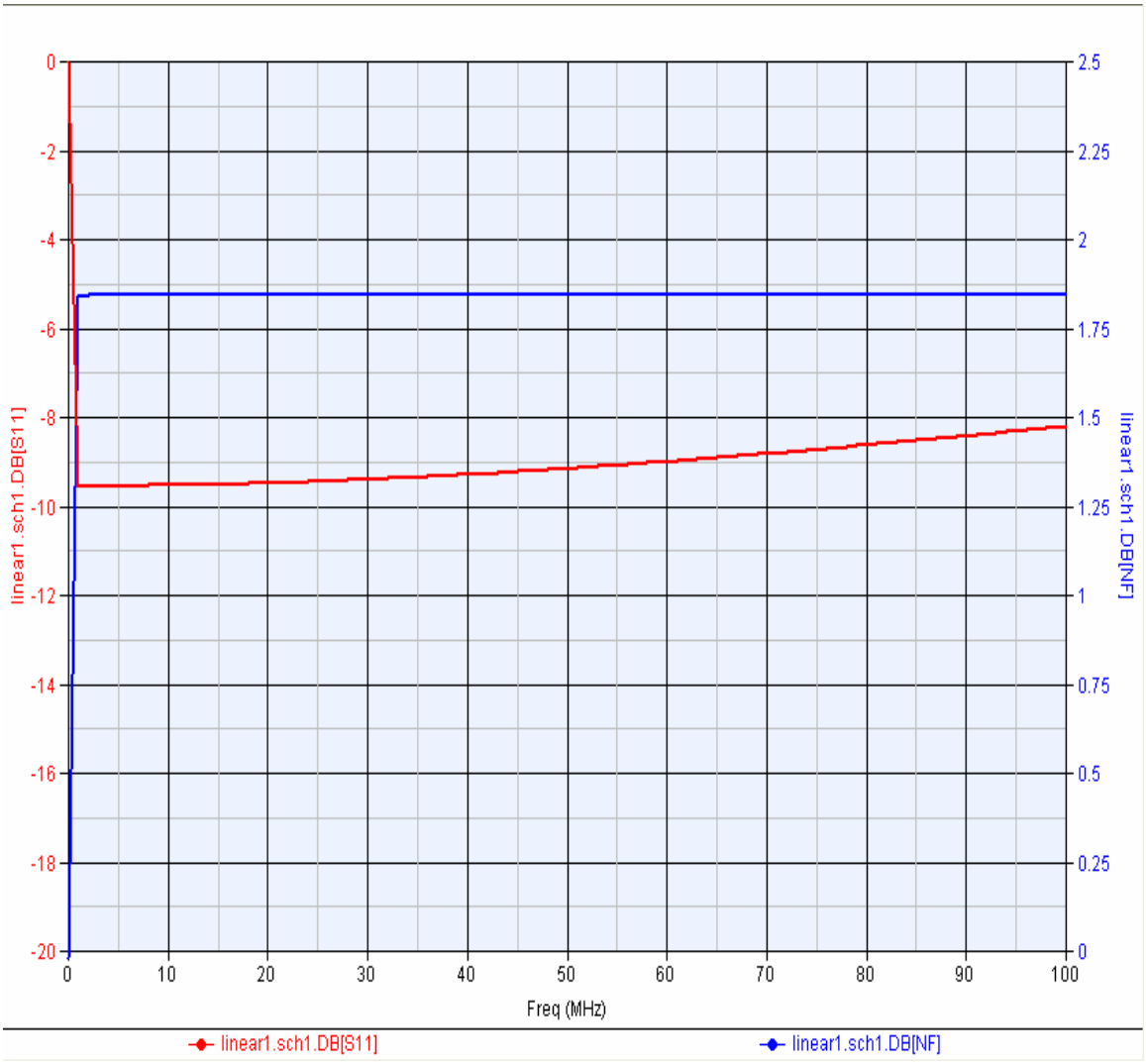

Figure 5.7 S11 & NF Graph for a GaAs Angelov MESFET Charge Model

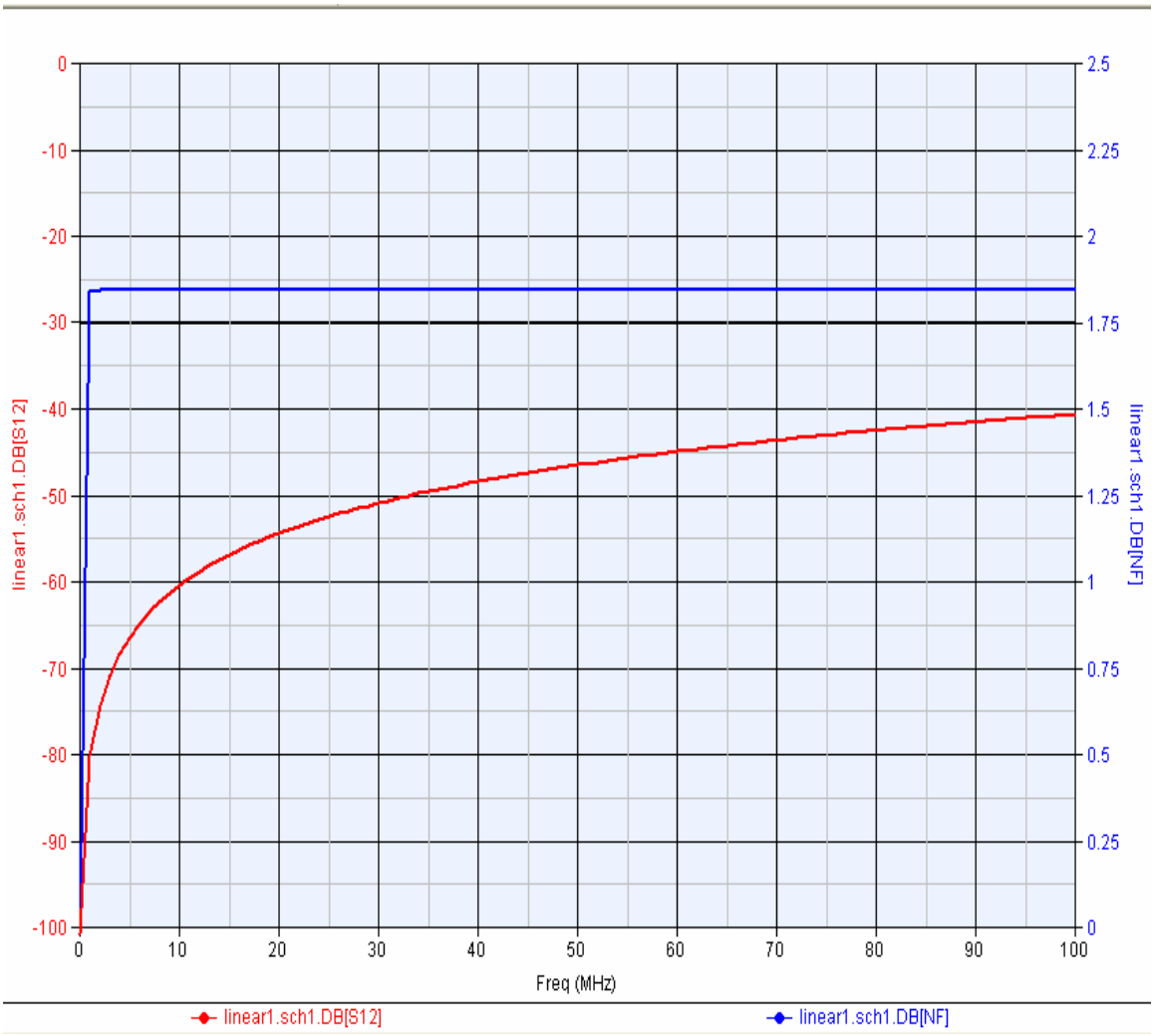

Figure 5.8 S12 & NF Graph for a GaAs Angelov MESFET Charge Model

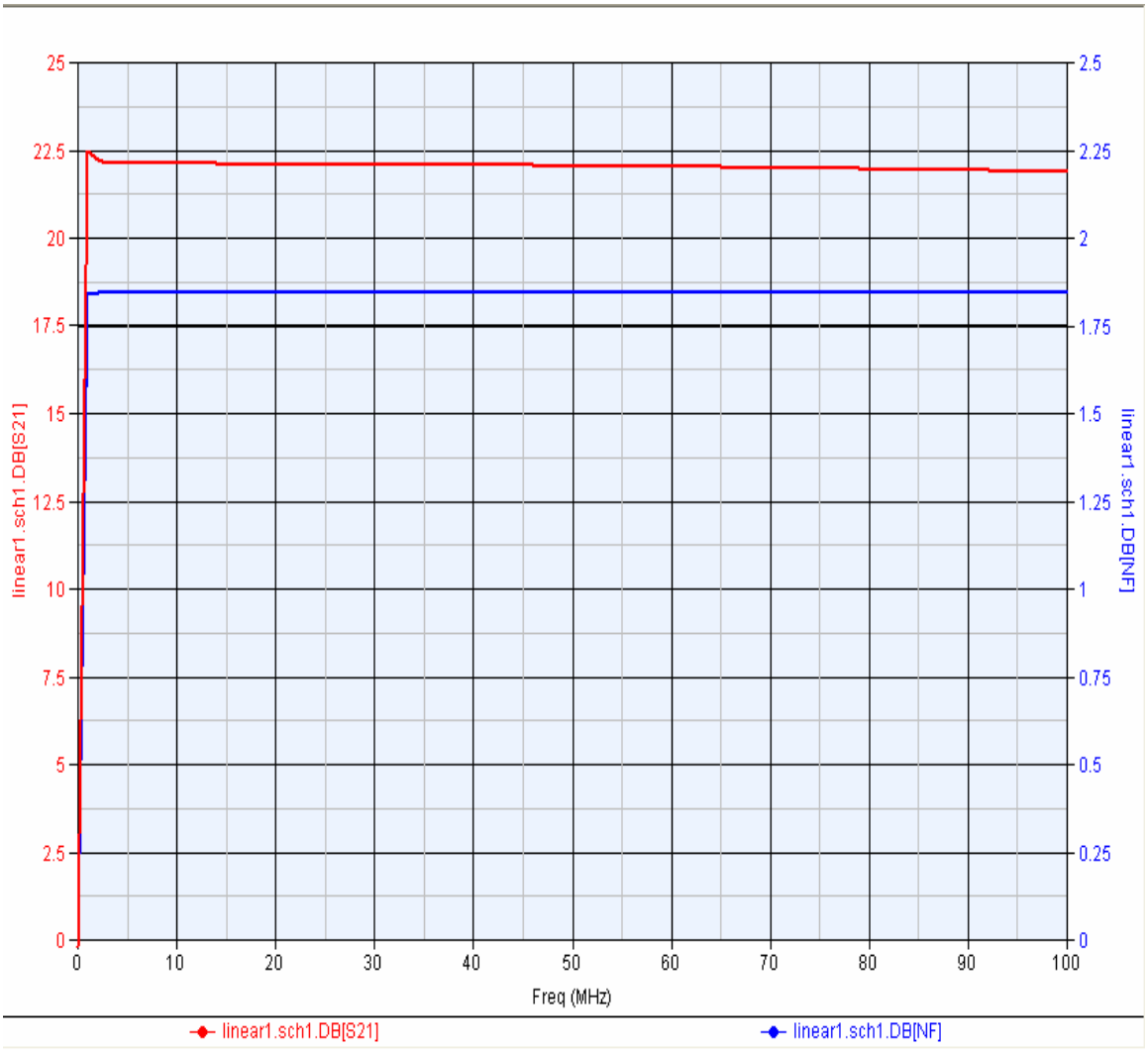

Figure 5.9 S21 & NF Graph for a GaAs Angelov MESFET Charge Model

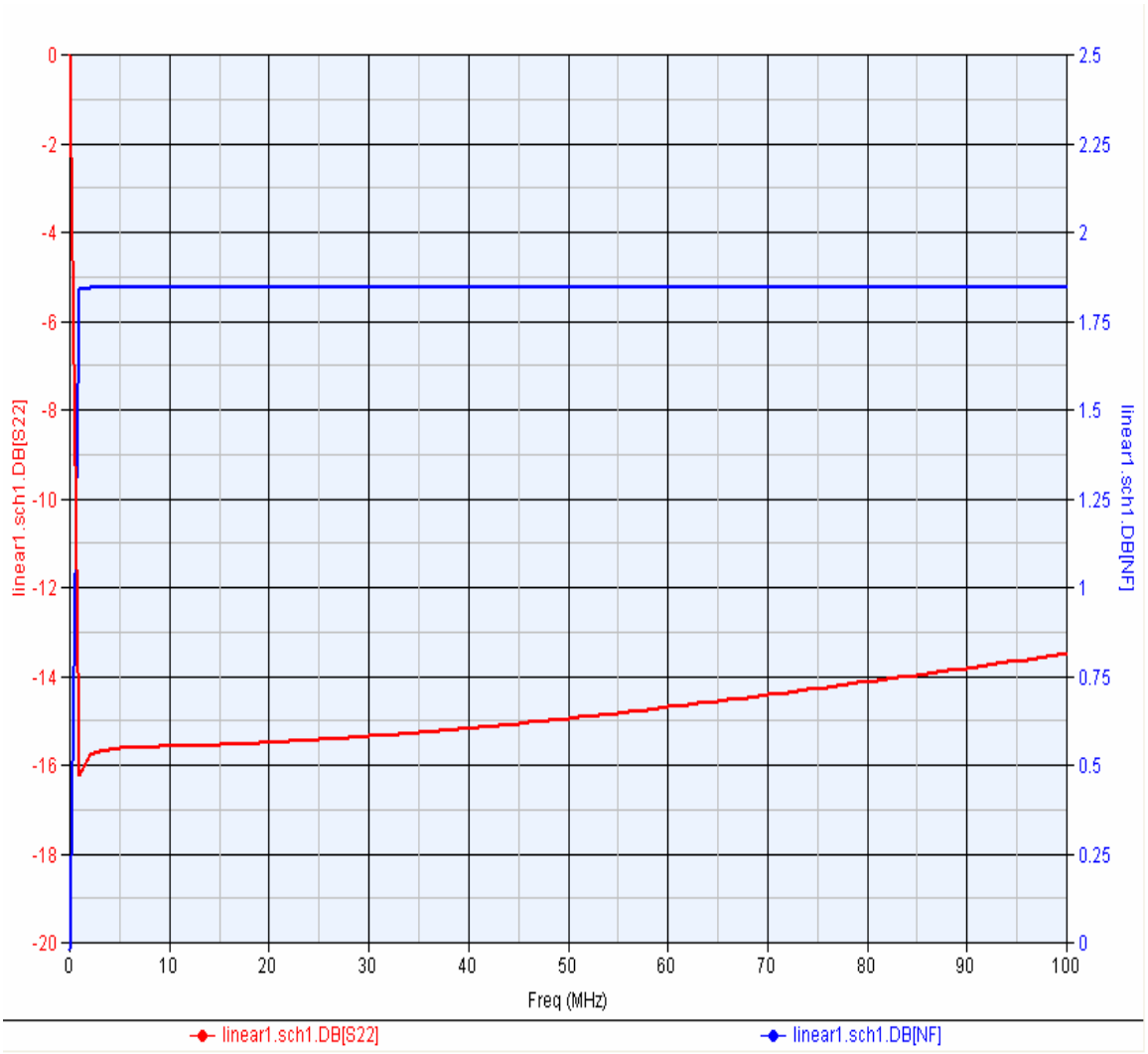

Figure 5.10 S22 & NF Graph for a GaAs Angelov MESFET Charge Model

5.3 Angelov-Calvo (New) Model Simulations for the Capacitance Model

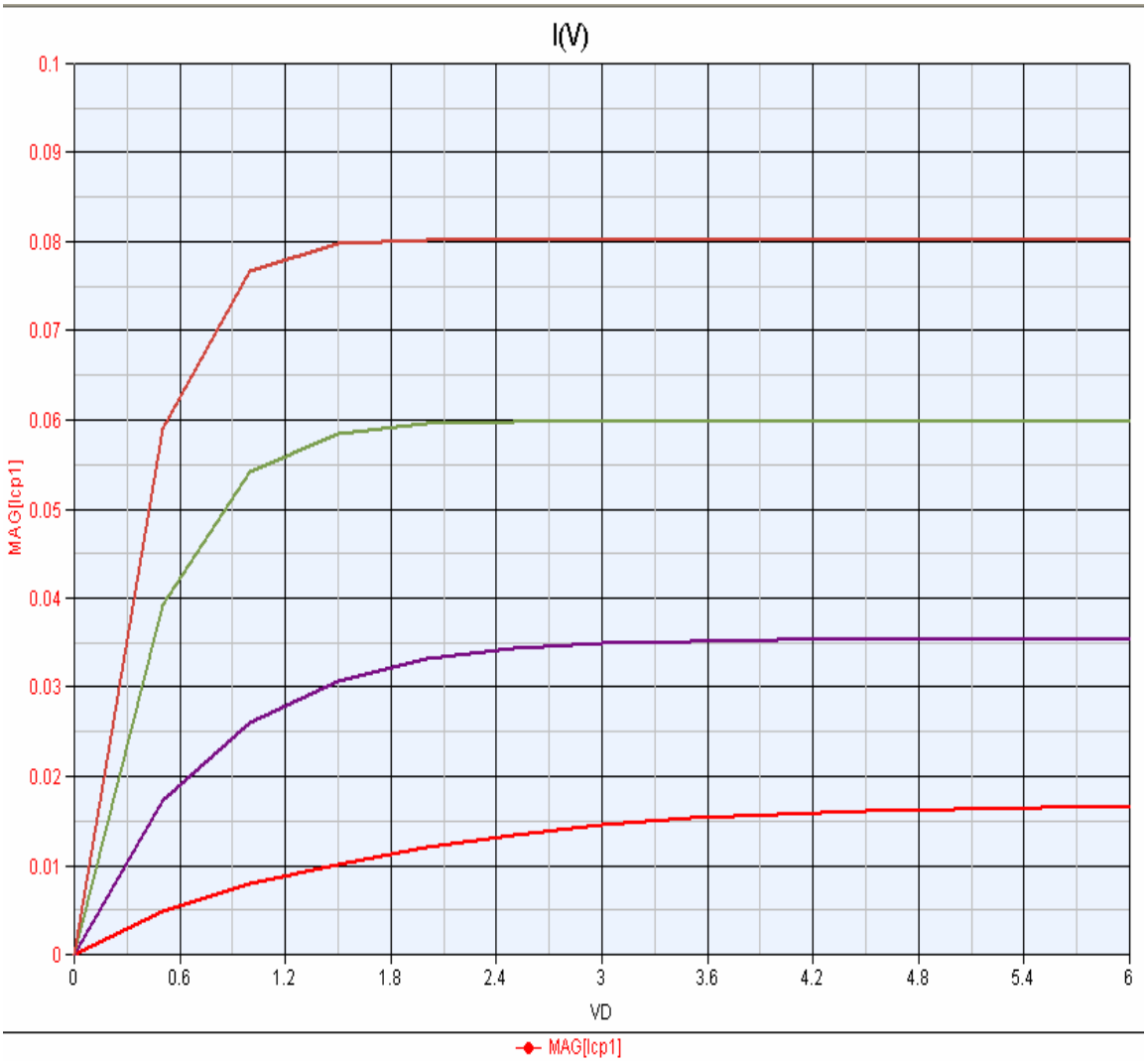

Figure 5.11 I-V Curves for a GaAs Angelov-Calvo MESFET Model

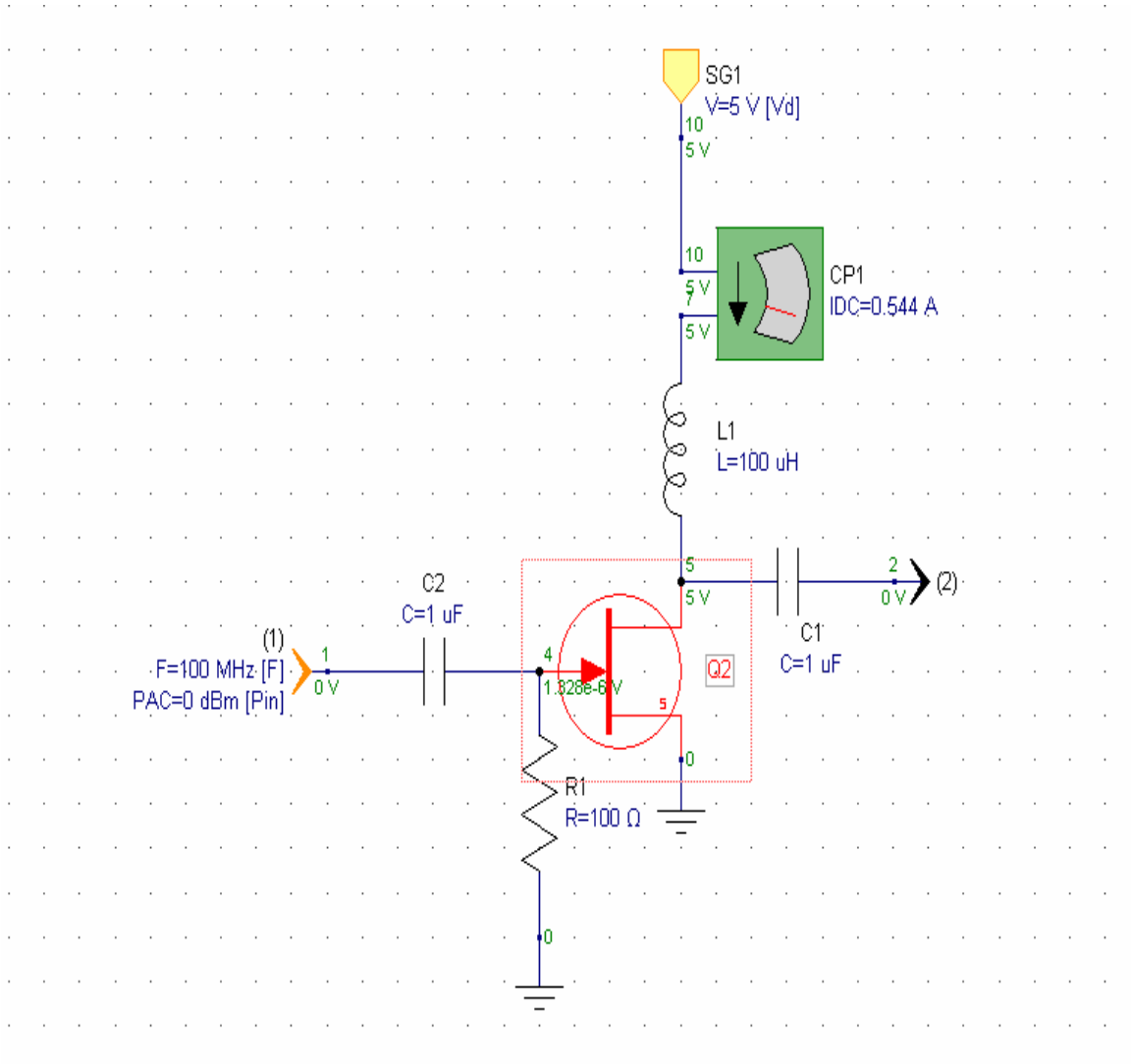

Figure 5.12 Schematic for a GaAs Angelov-Calvo MESFET Model

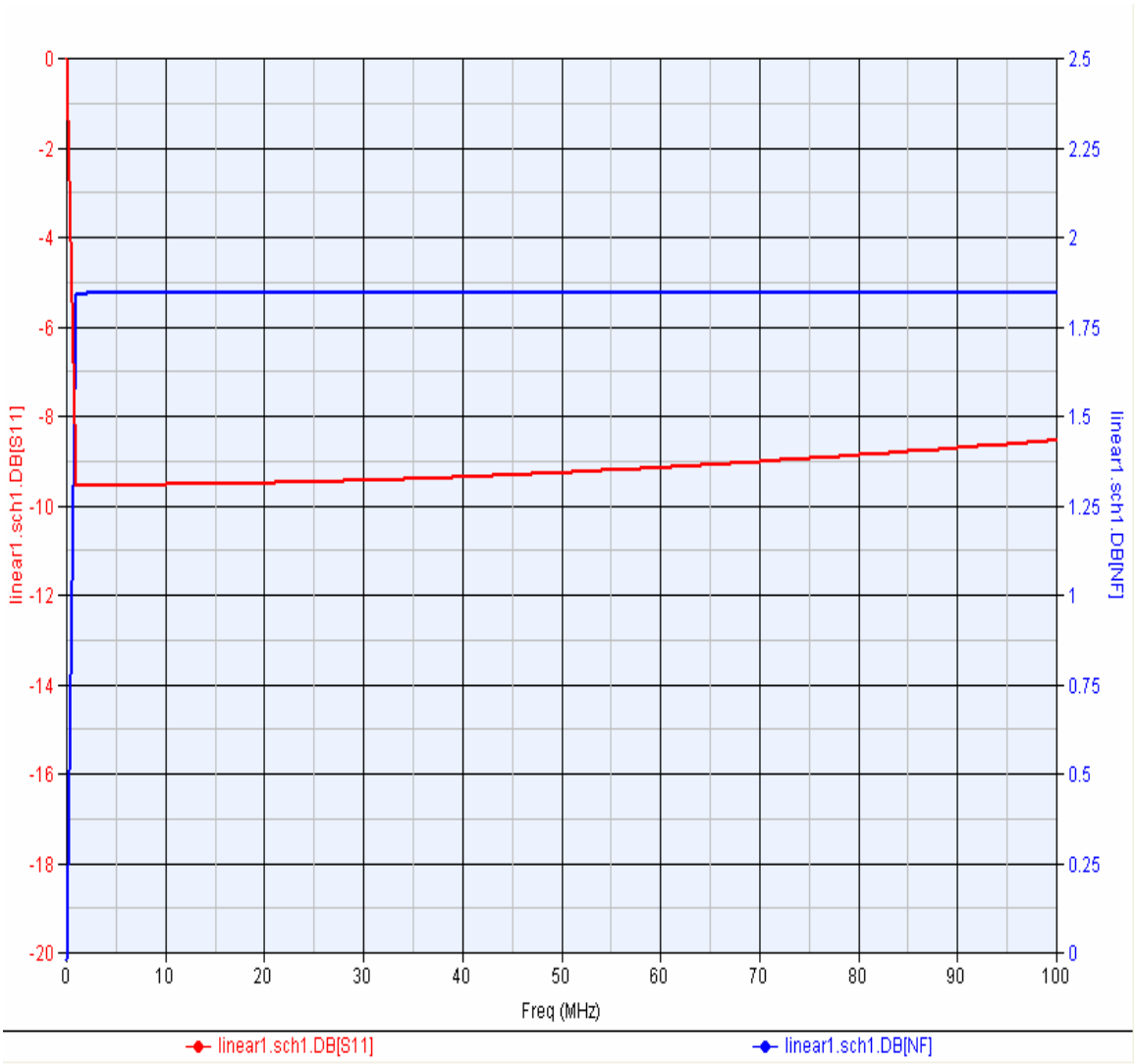

Figure 5.13 S11 & NF Graph for a GaAs Angelov-Calvo MESFET Cap Model

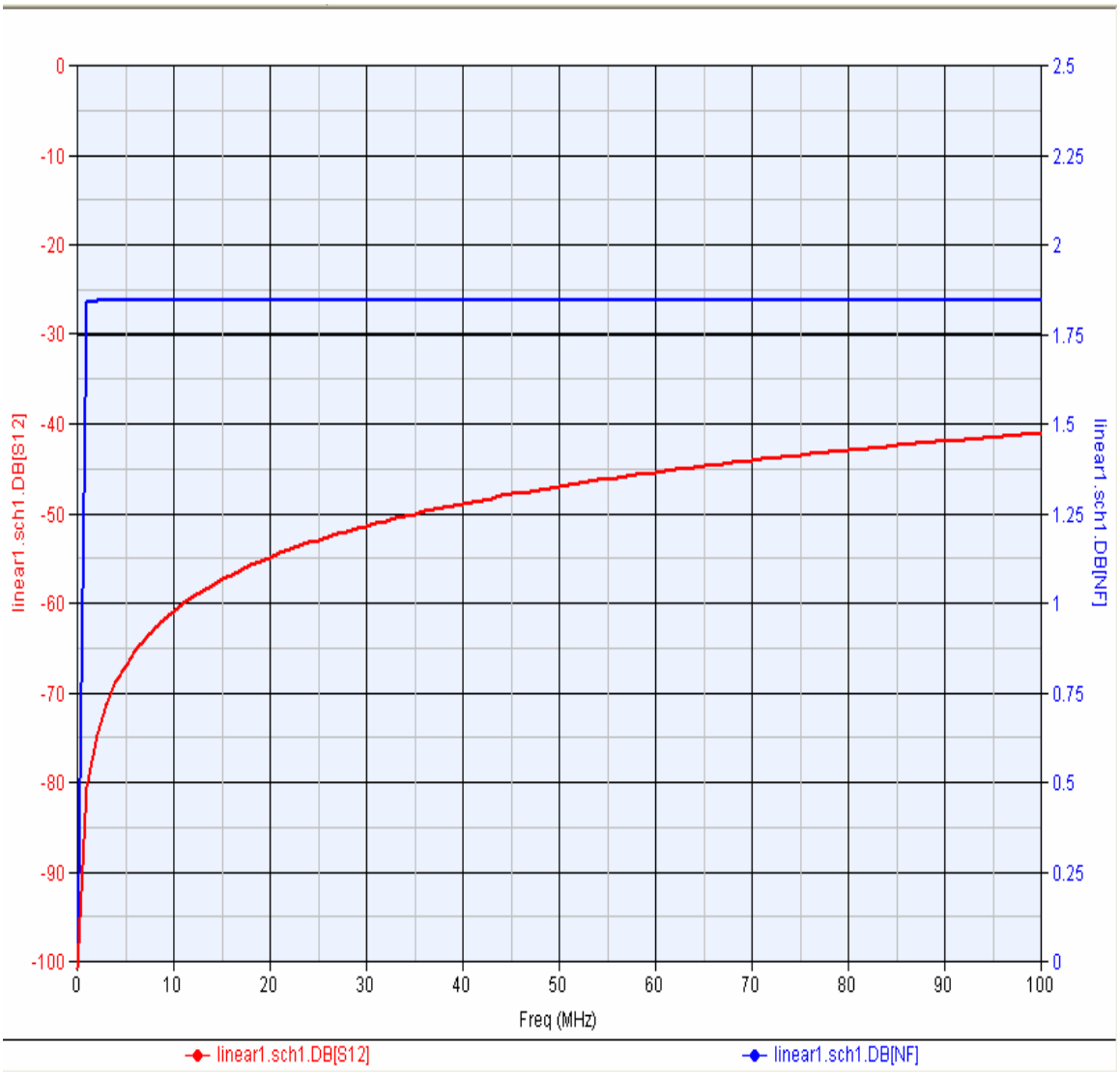

Figure 5.14 S12 & NF Graph for a GaAs Angelov-Calvo MESFET Cap Model

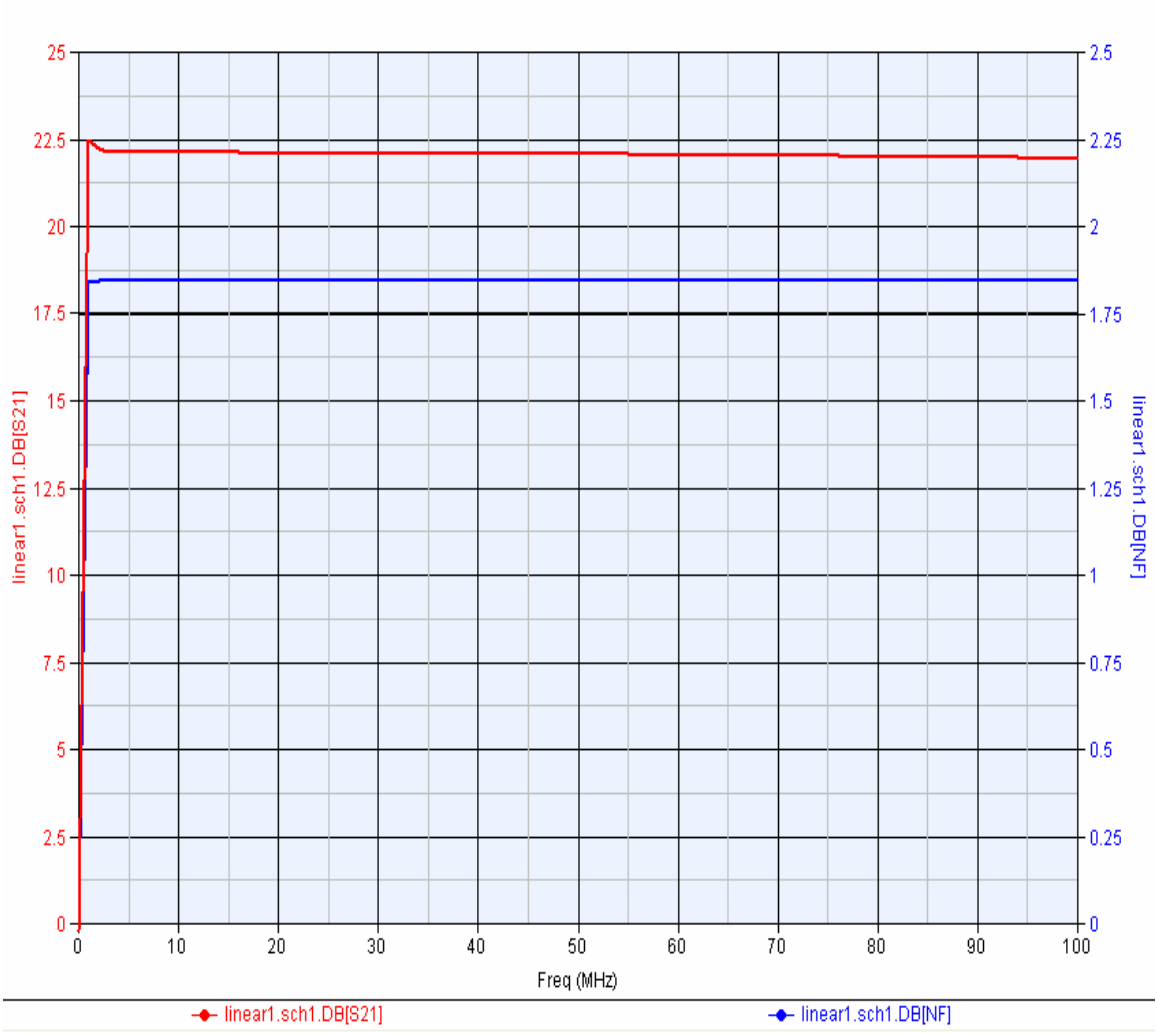

Figure 5.15 S21 & NF Graph for a GaAs Angelov-Calvo MESFET Cap Model

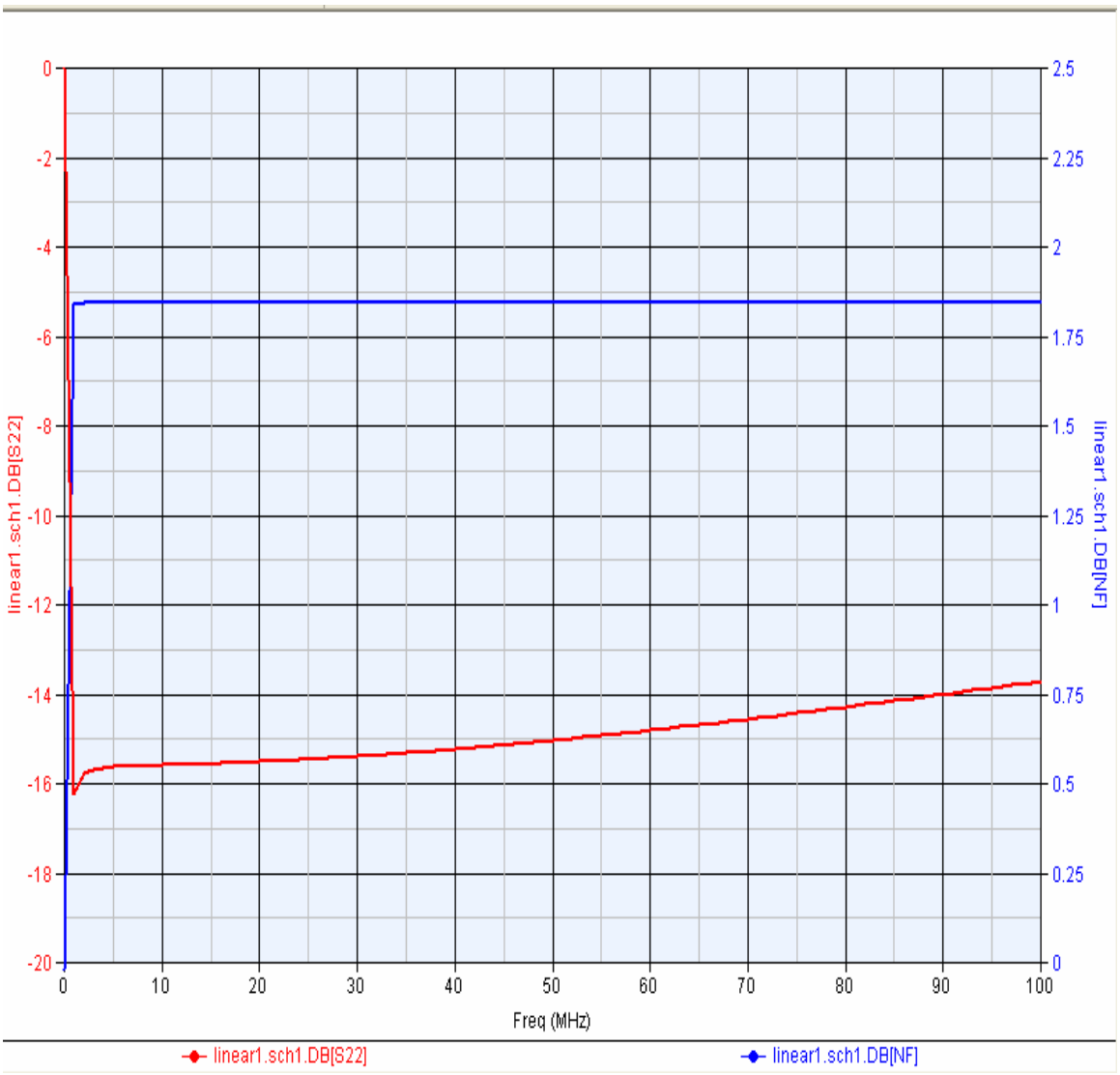

Figure 5.16 S22 & NF Graph for a GaAs Angelov-Calvo MESFET Cap Model

5.4 Angelov-Calvo (New) Model Simulations for the Charge Model

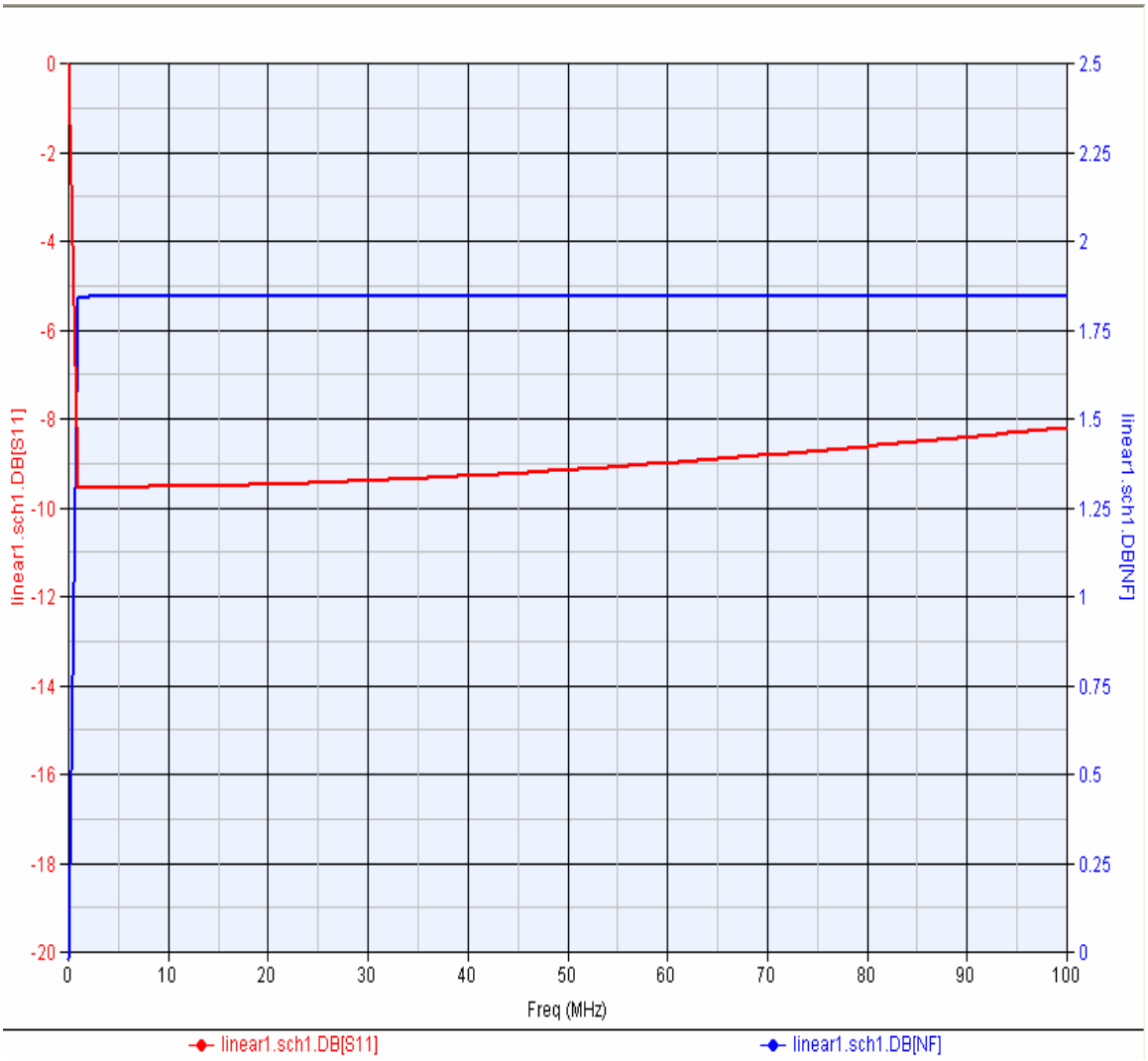

Figure 5.17 S11 & NF Graph for a GaAs Angelov-Calvo MESFET Charge Model

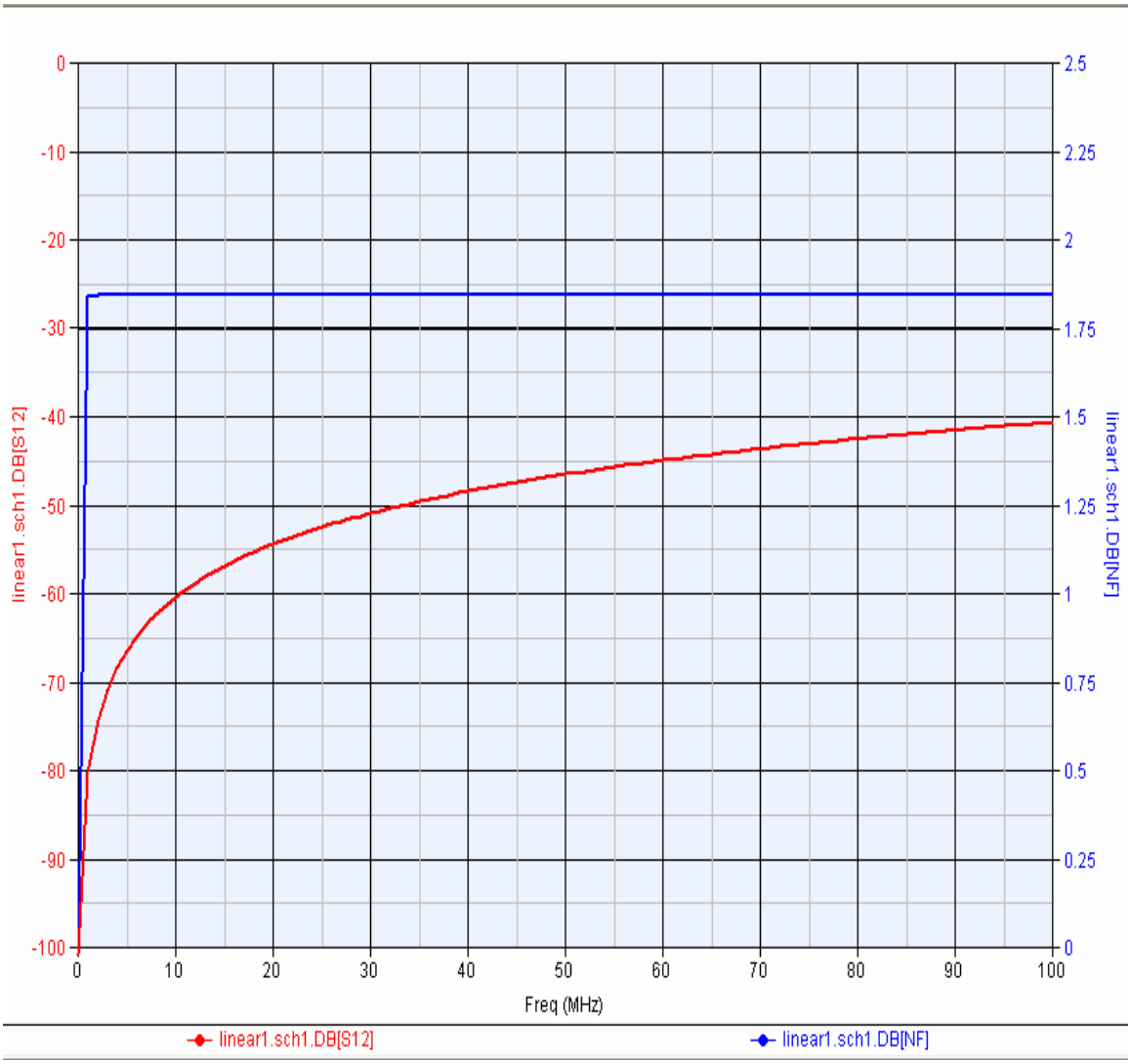

Figure 5.18 S12 & NF Graph for a GaAs Angelov-Calvo MESFET Charge Model

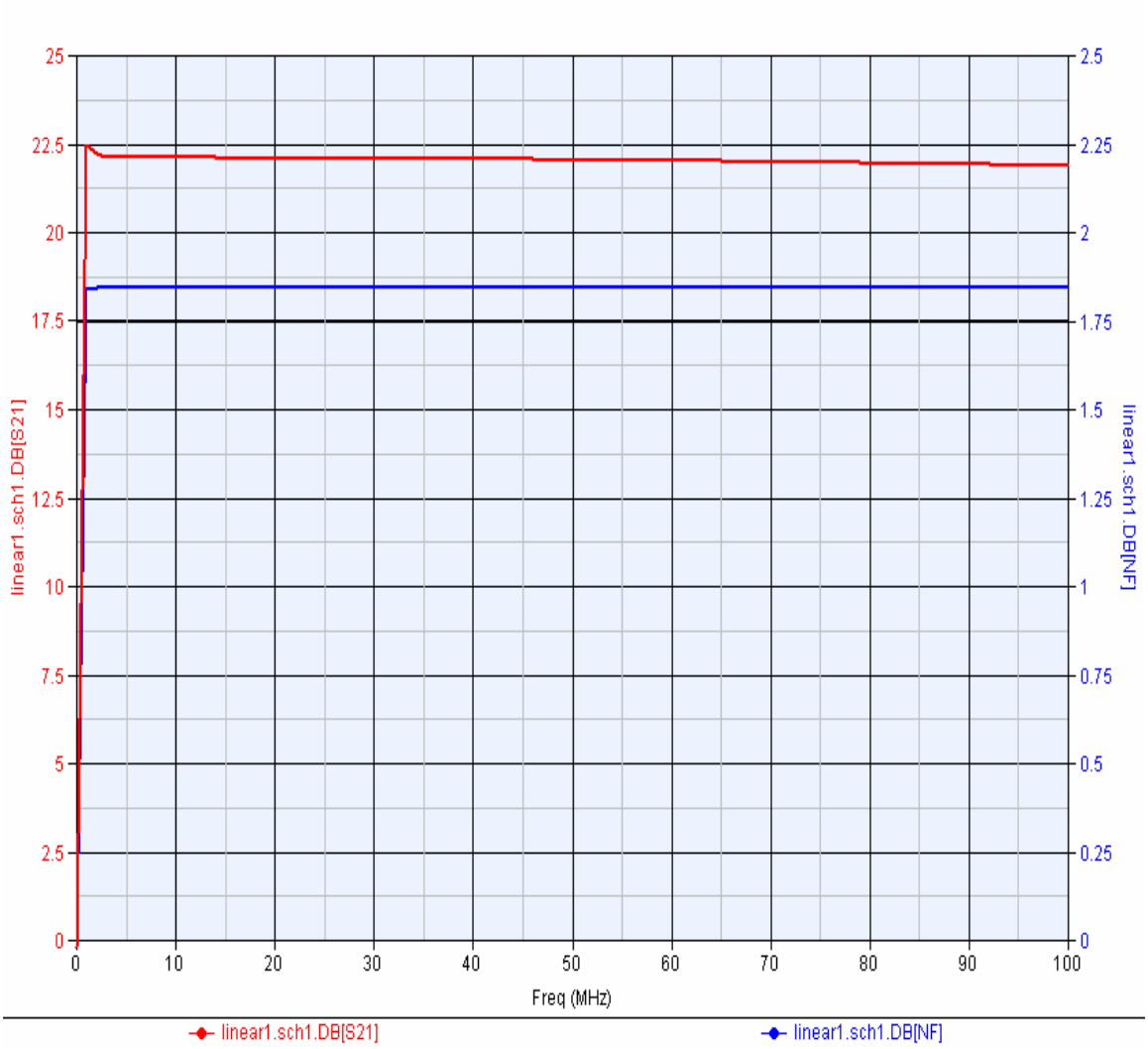

Figure 5.19 S21 & NF Graph for a GaAs Angelov-Calvo MESFET Charge Model

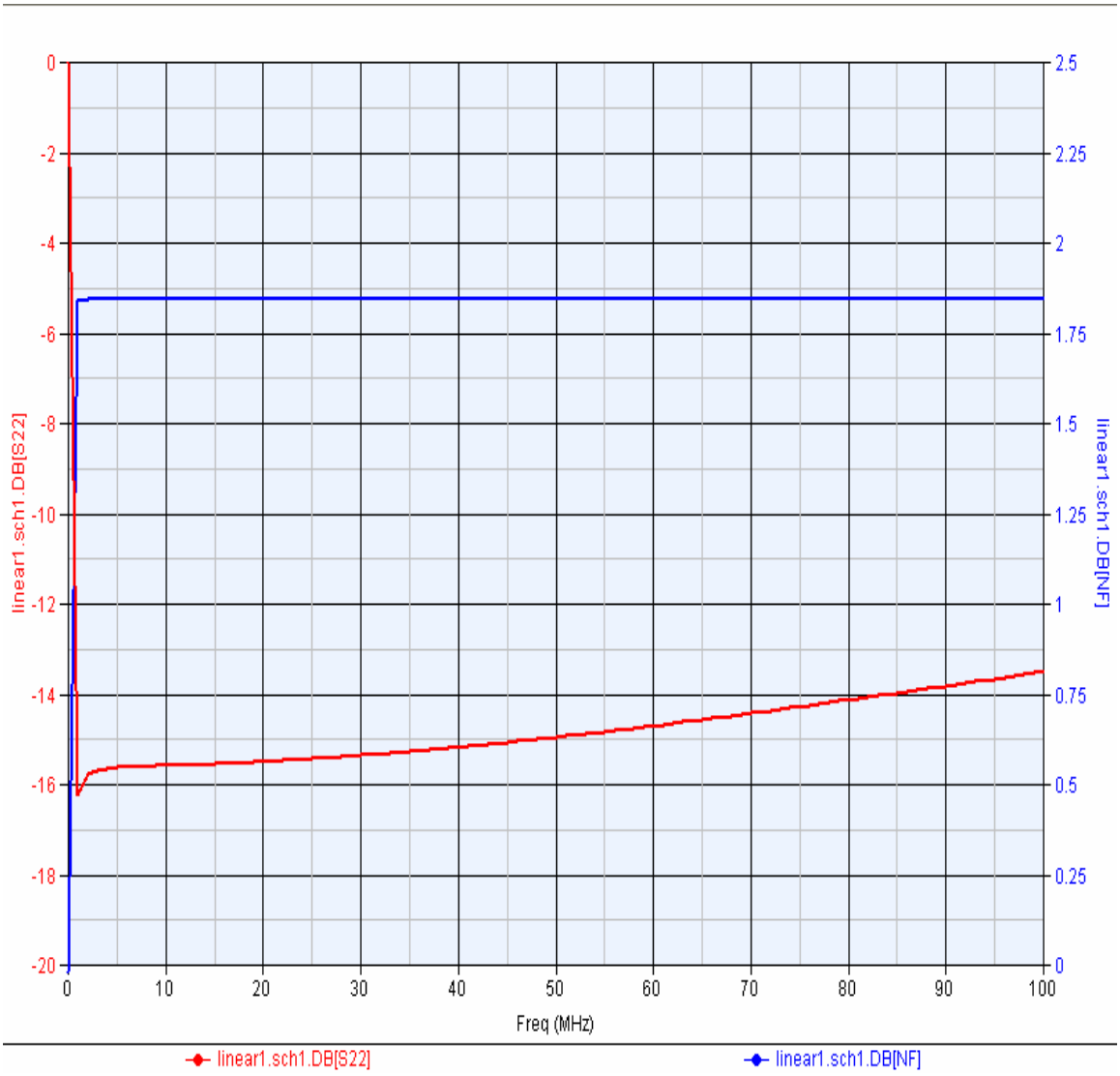

Figure 5.20 S22 & NF Graph for a GaAs Angelov-Calvo MESFET Charge Model

CHAPTER 6

RECOMMENDATIONS AND CONCLUSION

We have made use of Calvo's mathematical formulation applying it to Angelov's charge model to reduce the ill-effects of the (inevitable) presence of transcapacitance when modeling a nonlinear capacitor for a large-signal model essentially rendering the value of the transcapacitance equal to zero at a prescribed quiescent point. Calvo has pointed out that applying this scheme to a nonlinear bias dependent FET modeling applications has the following advantages:

1. All three capacitors can be modeled independently with any desired accuracy (as opposed to other procedures where capacitors are NOT modeled independently [1]).
2. The integrity of charge as a state variable (charge conservation) is maintained.
3. Simulations of small-signal excursions using large signal models are rendered consistent with their corresponding small signal models (up to negligible error).
4. This technique does not require any new parameter extraction (as would be the case if transcapacitance was inserted in the small signal model).
5. The convergence of harmonic balance simulations at very high power levels is improved in some models [1].

To summarize, a precise method of dealing with two-parameter bias dependent capacitors has been formulated such that the large signal model accurately tracks the small signal model performance. Furthermore, the method appears to improve the convergence range of harmonic balance simulations of large signal FET models.

The technique is general and is immediately adaptable for other applicable FET models such as Curtic, Statz and Parker Skellern models whose charge source formulas

have been obtained by integrating their corresponding capacitance formulas as shown in the earlier chapters.

Also, an entirely dual construction can be worked out for inductances to account for the 'transinductances' as well, if the nonlinear inductance (L) depends on a local and remote current $L(I_1, I_2)$. Then the flux will be conserved over cycles if L is accompanied by a transinductance $L^T(I_1, I_2)$ derivable from a flux function $\psi(I_1, I_2)$ via equation (6.1) [2] :

$$V = \partial\psi/\partial t = \partial\psi/\partial I_1 \bullet dI_1/dt + \partial\psi/\partial I_2 \bullet dI_2/dt = L\, dI_1/dt + L^T\, dI_2/dt \qquad (6.1)$$

This can prove to be an effective stratagem and is recommended for future work to model nonlinear inductances.

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APPENDICES

Appendix A: CODE

Angelov's Code of a Gallium Arsenide Field Effect Transistor modified using Miriam Calvo's Technique. The Modifications and changes in the code are in **bold.**

```
/*

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 Verilog-A definition of Angelov GaAsFET

 $RCSfile: angelov.va,v $ $Revision: 1.14 $ $Date: 2003/12/15 19:21:45
$

*/


`include "disciplines.vams"
`include "constants.vams"
`include "compact.vams"

`define SCALE_T_LINEAR_REL(x, s) x * (1 + s * delta_T)

module angelovmiriamnew_va(d, g, s);

    // %%DEVICE_CLASS=FET(NFET,PFET)%%

    // Instance parameters
    parameter integer NFET = 1 from [1:1];
    parameter integer PFET = 0 from [0:0]; // Only NFET supported
    parameter real W = -`NOT_GIVEN from (0:inf]; // Unused: gate width
    parameter real Ng = -`NOT_GIVEN from (0:inf]; // Unused: gate
fingers
    parameter integer Mode = 1 from [0:1];      // Unused
    parameter integer Noise = 1 from [0:1];     // Unused
    parameter integer Noimod = 1 from [0:1];    // Unused
    parameter integer Selft = 0 from [0:1];    // Flag for self-heating
    parameter real Trise = 0.0 from [-inf:inf]; // Difference sim. temp
and device temp, [C deg]
    parameter real Temp = `NOT_GIVEN from (-`P_CELSIUS0:inf];
//Device temp (only used if Trise is zero) [C]

    parameter integer Idsmod = 0 from [0:1];// Ids Current Model (0 or
1)
```

Appendix A (Continued)

```
    parameter integer Igmod = 0 from [0:1]; // Select gate diode model
[0:1]
     parameter integer Capmod = 1 from [0:2];// Select cap model [0:2]

     parameter real Vgs0 = -0.25; // operating voltage Vgs0 [V]
     parameter real Vgd0 = -3.25; // operating voltage Vgd0 [V]


    parameter real Ipk0 = 0.5671; // Current for max. transconductance
Ipk [A]
    parameter real Vpks = -0.17223; // Gate voltage Vpk for max
transconductance [V]
    parameter real Dvpks = 0.5454; // Delta gate voltage at peak gm [V]
    parameter real P1 = 0.887161; // Polynomial coeff P1 for channel
current [1/V]
    parameter real P2 = -0.323231; // Polynomial coeff P2 for channel
current [1/V^2]
    parameter real P3 = 0.284378; // Polynomial coeff P3 for channel
current [1/V^3]
    parameter real Alphar = 0.096189; // Saturation parameter alpha_r
[1/V]
    parameter real Alphas = 0.4742; // Saturation parameter alpha [1/V]
    parameter real Vkn = 0.8; // Knee voltage [V]
    parameter real Lambda = 0.02398; // Channel length modulation
parameter
    parameter real Lambda1 = 0.0; // Channel length modulation
parameter
    parameter real Lvg = 0.0; // Coeff for channel length modulation
parameter
    parameter real B1 = 1.88662; // Unsaturated coeff B1 for P1
    parameter real B2 = 0.67592; // Saturated coeff B2 for P1 [1/V]
    parameter real Lsb0 = 0.5; // Soft breakdown model parameter
    parameter real Vtr = 17.6; // Soft breakdown model parameter [V]
    parameter real Vsb2 = 0.0; // Surface breakdown model parameter [V]
    parameter real Cds = 707.752643e-15 from [0:inf]; // Zero-bias D-S
junction capacitance [F]
    parameter real Cgspi = 2249.92e-15; // Gate-source pinch-off
capacitance [F]
    parameter real Cgs0 = 3.39891e-12; // Gate-source capacitance
parameter [F]
    parameter real Cgdpi = 180.428772e-15; // Gate-drain pinch-off
capacitance [F]
    parameter real Cgdpe = 270.002e-15 from [0:inf]; // External G-D
Capacitor [F]
    parameter real Cgd0 = 0.0; // Gate-drain capacitance parameter Cgdo
[F]

    parameter real P10 = 0.00015731; // Polynomial coeff P10 for
capacitance
    parameter real P11 = 1.086932; // Polynomial coeff P11 for
capacitance
    parameter real P20 = 1.3259488; // Polynomial coeff P20 for
capacitance
```

Appendix A (Continued)

```
    parameter real P21 = 0.001938; // Polynomial coeff P21 for
capacitance
    parameter real P30 =9.1385e-005; // Polynomial coeff P30 for
capacitance
    parameter real P31 = 0.0666; // Polynomial coeff P31 for
capacitance
    parameter real P40 = 0.0001243; // Polynomial coeff P40 for
capacitance
    parameter real P41 = 1.04754; // Polynomial coeff P41 for
capacitance
    parameter real P111 = 1e-005; // Polynomial coeff P400 for
capacitance

    parameter real Ij = 0.02 from [0:inf]; // Gate fwd saturation
current [A]
    parameter real Pg = 15 from [0:inf]; // Gate current parameter
    parameter real Ne = 1.3 from [0:inf] exclude 0; // Gate p-n
emission coeff
    parameter real Vjg = 0.9 from [0:inf] exclude 0; // Gate current
parm [V]

    parameter real Rg = 0.35 from [0:inf]; // Gate ohmic resistance
[Ohm]
    parameter real Rd = 0.6336 from [0:inf]; // Drain ohmic resistance
[Ohm]
    parameter real Ri = 0.25 from [0:inf]; // Input resistance [Ohm]
    parameter real Rs = 0.561 from [0:inf]; // Source ohmic resistance
[Ohm]
    parameter real Rgd = 0 from [0:inf]; // Gate resistance [Ohm]

    parameter real Ld = 0 from [0:inf]; // Unused: Drain ohmic
inductance [H]
    parameter real Ls = 0 from [0:inf]; // Unused: Source ohmic
inductance [H]
    parameter real Lg = 0 from [0:inf]; // Unused: Gate ohmic
inductance [H]

    parameter real Tau = 4.2787e-12 from [0:inf]; // Device delay [s]
    parameter real Rcmin = 10 from [0:inf]; // Min value of Rc [Ohm]
    parameter real Rc = 54 from [0:inf]; // R for freq dep output cond
[Ohm]
    parameter real Crf = 10000e-12; // C for freq dep output cond [F]
    parameter real Rcin = 100.0e3 from [0:inf]; // R for freq dep input
cond [Ohm]
    parameter real Crfin = 0.0 from [0:inf]; // C for freq dep input
cond[F]

    parameter real Rth = 15 from [0:inf]; // Thermal resistance [Ohm]
    parameter real Cth = 10e-6 from [0:inf]; // Thermal capacitance [F]
    parameter real Tcipk0 = -0.00181; // Linear temp coef TIpk for Ipk
[A/K]
    parameter real Tcp1 = -0.00031; // Linear temp coef TIpk for Ipk
[A/K]
```

Appendix A (Continued)

```
    parameter real Tccgs0 = 0.0; // Linear temp coef Cgs0 parm
    parameter real Tccgd0 = 0.0; // Linear temp coef Cgd0 parm
    parameter real Tclsb0 = 0.0; // Linear temp coef Lsb0 parm
    parameter real Tcrc = 0.0; // Linear temp coef Rc parm
    parameter real Tccrf = 0.0; // Linear temp coef Crf parm

    parameter real NoiseR = 0.5 from [0:inf); // Gate noise coeff
    parameter real NoiseP = 1.0 from [0:inf); // Gate noise coeff
    parameter real NoiseC = 0.9 from [0:inf); // Gate-drain noise coeff
    parameter real Fnc = 0.0 from [0:inf); // Noise corner freq [Hz]
    parameter real Kf = 0.0 from [0:inf]; // Flicker noise coeff
    parameter real Af = 1.0 from (0:inf]; // Flicker noise exponent
    parameter real Ffe = 1.0 from (0:inf]; // Flicker noise parameter
    parameter real Tg = 25.0 from (-`P_CELSIUS0:inf]; // Equiv temp [C]
    parameter real Td = 25.0 from (-`P_CELSIUS0:inf]; // Equiv temp [C]
    parameter real Tdl = 0.1 from [-inf:inf]; // Equiv temp [C]
    parameter real Tmn = 1.0 from [-inf:inf]; // noise fitting coeff
    parameter real Klf = 1.0e14 from [-inf:inf]; // Flicker noise
exponent
    parameter real Fgr = 60.0e3 from [-inf:inf]; // G-R freq corner [Hz]
    parameter real Np = 0.3 from [-inf:inf]; // flicker noise freq exp
    parameter real Lw = 0.1 from [-inf:inf]; // effective gate noise
width [mm]

    parameter real Tnom = `NOT_GIVEN from (-`P_CELSIUS0:inf); // param
meas T [C]

    electrical d, g, s, di, gi, si, gdi, gsi, bi, rf, p_avg_i, t;

    real alpha, alpha_s, x, x_2, x_3, x_4, x_5, y;
    real Vgs, Vgd, Vds, Vdg;
    real Igs, Igd;
    real Vth, T_nom, T, delta_T;
    real V_pk, P_1, psi, L_sd1, L_sb, V_dgt;
    real Ids, P_avg, pg_param, tanh_gs, tanh_gd;
    real Q_gd, Q_gs;
    real psi_1, psi_2, psi_3, psi_4, psi_11, psi_44;
    real Ipk0_T, Lambda_T, Psat_T, B1_T;
    real Rc1, Lsb0_T, Cgs0_T, Cgd0_T, Rc_T, Crf_T;
    real P1m, P1_T, Vpkm;
    real T0, T1, T2;
    real lambda_n, lambda_n1;
    real lambda_p, lambda_p1;
    real psi_n, alpha_n, Idsp, Idsn;
    real tanh_psi, tanh_psi_n, tanh_alpha_vds, tanh_alpha_n_vds;
    real tanh1, tanh2, tanh3, tanh4, cosh0, cosh1, cosh11, lc1, lc11,
lc10, lc4, lc44, lc40;
    real Qgs0, Qgd0, Vgsc, Vgdc;

    analog begin

        Vgs = V(gi,si);
```

Appendix A (Continued)

```
Vgd = V(gi,di);
Vdg = -Vgd;
Vds = V(di,si);
Vgsc = V(gsi,si);
Vgdc = V(gdi, di);

// Temperature effects
if (Temp == `NOT_GIVEN)
    T = $temperature + Trise;
else
    T = Temp + `P_CELSIUS0;


if (Tnom == `NOT_GIVEN)
    T_nom = `DEFAULT_TNOM + `P_CELSIUS0;
else
    T_nom = Tnom + `P_CELSIUS0;

if (Selft)
    T = T + V(t);

Vth = $vt(T);
delta_T = T - T_nom;
if (delta_T || Rth > 0) begin
    Ipk0_T = `SCALE_T_LINEAR_REL(Ipk0, Tcipk0);
    P1_T   = `SCALE_T_LINEAR_REL(P1, Tcp1);
    Lsb0_T = `SCALE_T_LINEAR_REL(Lsb0, Tclsb0);
    Cgs0_T = `SCALE_T_LINEAR_REL(Cgs0, Tccgs0);

    Cgd0_T = `SCALE_T_LINEAR_REL(Cgd0, Tccgd0);
    Rc_T   = `SCALE_T_LINEAR_REL(Rc, Tcrc);
    Crf_T  = `SCALE_T_LINEAR_REL(Crf, Tccrf);
end
else begin
    Ipk0_T = Ipk0;
    P1_T = P1;
    Lsb0_T = Lsb0;
    Cgs0_T = Cgs0;
    Cgd0_T = Cgs0;
    Rc_T = Rc;
    Crf_T = Crf;
end

// If Pg is not given but Ne is given, Pg = 1/(2*Ne*Vt)
if (Pg == -`NOT_GIVEN) begin
    if (Ne == -`NOT_GIVEN)
        pg_param = 15.0; // Default value
    else
        pg_param = 0.5 / Ne / Vth;
end
else
    pg_param = Pg; // Take the given value
```

Appendix A (Continued)

```
        T0 = cosh(B2 * Vds);
        P1m = P1_T * (1 + B1 / (T0 * T0));
        Vpkm = Vpks - Dvpks + Dvpks * tanh(Alphas * Vds) - Vsb2 *
            (Vdg - Vtr) * (Vdg - Vtr);


        T1 = Vgs - Vpkm;
        T2 = T1 * T1;
        psi = P1m * (Vgs - Vpkm) + P2 * T2 + P3 * T1 * T2;
        tanh_psi = 1 + tanh(psi);
        alpha = Alphar + Alphas * tanh_psi;
        tanh_alpha_vds = tanh(alpha * Vds);

        if (Idsmod == 0) begin
            Ids = Ipk0_T * tanh_psi * tanh_alpha_vds *
                (1 + Lambda * Vds + Lsb0_T * limexp(Vdg - Vtr));
        end
        else begin
            T0 = Vgd - Vpkm;
            T1 = T0 * T0;
            T2 = T1 * T0;
            psi_n = P1m * (T0 + P2 * T1 + P3 * T2);

            tanh_psi_n = 1 + tanh(psi_n);
            alpha_n = Alphar + Alphas * tanh_psi_n;
            tanh_alpha_n_vds = tanh(alpha_n * Vds);
            lambda_n = Lambda + Lvg * tanh_psi_n;
            lambda_p = Lambda + Lvg * tanh_psi;
            lambda_n1 = Lambda1 + Lvg * tanh_psi_n;
            lambda_p1 = Lambda1 + Lvg * tanh_psi;
            Idsp = Ipk0_T * tanh_psi * (1 + tanh_alpha_vds) *
                 (1 + lambda_p * Vds + lambda_p1 * limexp(Vds / Vkn -
1));
            Idsn = Ipk0_T * tanh_psi_n * (1 - tanh_alpha_n_vds) *
                 (1 - lambda_n * Vds - lambda_n1 * limexp(Vds / Vkn -
1));
            Ids = 0.5 * (Idsp - Idsn);
        end


        // Leakage diodes
        if (Igmod == 0) begin
            T0 = exp(pg_param * tanh(-2 * Vjg));
            tanh_gs = tanh(2 * (Vgsc - Vjg));
            tanh_gd = tanh(2 * (Vgdc - Vjg));
        end
        else begin
            T0 = exp(-pg_param * Vjg);
            tanh_gs = tanh(Vgsc - Vjg);
            tanh_gd = tanh(Vgdc - Vjg);
        end
        Igs = Ij * (exp(pg_param * tanh_gs) - T0);
        Igd = Ij * (exp(pg_param * tanh_gd) - T0);
```

Appendix A (Continued)

```
        // Charge model
        psi_1 = P10 + P11 * Vgsc + P111 * Vds;
        psi_11 = P10 + P11 * Vgs0 + P111 * Vds;
        tanh1 = 1 + tanh(psi_1);
        psi_2 = P20 + P21 * Vds;
        tanh2 = 1 + tanh(psi_2);
        psi_3 = P30 - P31 * Vds;
        tanh3 = 1 + tanh(psi_3) - P111;
        psi_4 = P40 + P41 * Vgdc - P111 * Vds;
        psi_44 = P40 + P41 * Vgd0-P111 * Vds;
        tanh4 = 1 + tanh(psi_4);

        Rc1 = Rcmin + Rc_T / (1 + tanh1);

        case(Capmod)
        0: begin  // Linear capacitance
            Q_gs= Cgspi * Vgsc;
            Q_gd= Cgdpi * Vgdc;
        end
        1: begin  // Bias dependent capacitance
            Q_gs = (Cgspi + Cgs0_T * tanh1 * tanh2) * Vgsc;
            Q_gd = (Cgdpi + Cgd0_T * (tanh3 * tanh4 + 2 * P111)) * Vgdc;
        end
        2:begin  // Charge-based (best convergence)
            tanh2 = tanh2 - P111;
            cosh0 = cosh(P10 + P111 * Vds);
            lc10 = ln(cosh0);
            cosh1 = cosh(psi_1);
            cosh11 = cosh(psi_11);
            lc1 = ln(cosh1);
            lc11 = ln(cosh11);
            Qgs0 = P10 + P111 * Vds + lc10;
            Q_gs = Cgs0_T * ((psi_1 + lc1 - Qgs0) * tanh2/P11 + 2 *
P111 * Vgsc) + Cgspi * Vgsc - (Cgs0_T * ((psi_11 + lc11 - Qgs0) *
tanh2/P11 + 2 * P111 * Vgs0) + Cgspi * Vgs0);

            cosh0 = cosh(P40 - P111 * Vds);
            lc40 = ln(cosh0);
            cosh1 = cosh(psi_4);
            cosh11 = cosh(psi_44);
            lc4 = ln(cosh1);
            lc44 = ln(cosh11);
            Qgd0 = P40 - P111 * Vds + lc40;
            Q_gd = Cgd0_T * ((psi_4 + lc4 - Qgd0) * tanh3 / P41 + 2 *
P111 * Vgdc) + Cgdpi * Vgdc - (Cgd0_T * ((psi_44 + lc44 - Qgd0) * tanh3
/ P41 + 2 * P111 * Vgd0) + Cgdpi * Vgd0);
        end
        endcase

        I(di,si)  <+ Ids;
        I(gsi,si) <+ Igs;
```

Appendix A (Continued)

```
        I(gdi,di) <+ Igd;

        I(gdi,di) <+ ddt(Q_gd);
        I(gsi,si) <+ ddt(Q_gs);

        I(g,di)   <+ Cgdpe * ddt(V(g,di));
        I(di,si)  <+ Cds   * ddt(Vds);
        I(di,rf)  <+ Crf_T * ddt(V(di,rf));
        I(bi,gi)  <+ Crfin * ddt(V(bi,gi));
        V(rf,si)  <+ I(rf,si) * Rc1;
        V(bi,si)  <+ I(bi,si) * Rcin;
        V(gi,gdi) <+ I(gi,gdi) * Rgd;
        V(gi,gsi) <+ I(gi,gsi) * Ri;

        V(si,s)  <+ I(si,s) * Rs;
        V(di,d)  <+ I(di,d) * Rd;
        V(g,gi)  <+ I(g,gi) * Rg;

        V(p_avg_i) <+ Vds * Ids - Tau * ddt(P_avg);

        // Add noise
        I(di,si) <+ flicker_noise(Kf * pow(Ids, Af), 1.0, "flicker");
        V(si,s) <+ white_noise(4.0 * `P_K * T * (Rs), "Rs");
        V(di,d) <+ white_noise(4.0 * `P_K * T * (Rd), "Rd");

        if (Selft) begin
            I(t) <+ Cth * ddt(V(t));
            I(t) <+ -Ids * Vds + Igs * Vgsc;
            I(t) <+ V(t) / Rth;
        end
        end

endmodule
```