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Low Loss Rf/Millimeter-Wave Mems Phase Shifters

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by

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of the requirements for the degree of
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DEDICATION

This dissertation is dedicated to my parents, grand-parents and to my sister for their immense love and support in all my endeavors.

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ABSTRACT

A true time delay multi-bit MEMS phase shifter topology based on impedance-matched slow-wave CPW sections on a 500μm thick quartz substrate is presented. Design equations based on the approximate model for a distributed line is derived and used in optimization of the unit cell parameters. A semi-lumped model for the unit cell is derived and its equivalent circuit parameters are extracted from measurement and EM simulation data. This unit cell model can be cascaded to accurately predict N-section phase shifter performance. Experimental data for a 4.6mm long 4-bit device shows a maximum phase error of 5.5° and S_{11} less than -21dB from 1-50GHz. A reconfigurable MEMS transmission line based on cascaded capacitors and slow-wave sections has been developed to provide independent Z_o - and β-tuning. In the Z_o-mode of operation, a 7.4mm long line provides Z_o-tuning from 52 to 40Ω (+/-2Ω) with constant phase between the states through 50GHz. The same transmission line is reconfigured by addressing the MEM elements differently and experimental data for a 1-bit version shows 358°/dB (or 58°/mm) with S_{11} less than -25dB at 50GHz. The combined effect of Z_o- and β-tuning is also realized using a 5-bit version.

An electronically tunable TRL calibration set that utilizes a 4-bit true time delay MEMS phase shifter topology, is demonstrated. The accuracy of the tunable TRL is close to a conventional multi-line TRL calibration and shows a maximum error bound of 0.12 at 40GHz. The Tunable TRL method provides for an efficient usage of wafer area while retaining the accuracy associated with the TRL technique, and reduces the number of probe placements.

PREFACE

I sincerely thank my advisor, Dr. Tom Weller, for allowing me to continue with this thesis topic. When this project started there was little or no progress during the first year and his patience and support was of great help. His technical insight complimented with his understanding and patience make him one of the remarkable persons I have ever met. I sincerely thank him for his contributions to my personal and professional growth.

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CHAPTER 1

Introduction

The field of RF-microelectromechanical systems (RF-MEMS) has seen enormous growth in the past decade due to its potential for high performance in defense and commercial applications. The program objectives of federal agencies DARPA[1]'s SPO[2] and MTO[3] is to develop innovative ideas that offer significant improvement in technology and to pursue these ideas from the demonstration of technical feasibility through the development of prototype systems. Other federal research organizations such as NASA, NSF, Airforce Research Labs, Navy and several commercial organizations are actively pursuing the incorporation of MEMS devices for future applications [1]. The strong advantages of RF MEMS are found in terms of low loss, virtually no DC power consumption, light weight and can be manufactured on low-cost silicon or glass substrates.

At first this interest was driven by the success of low-frequency MEMS devices and their advantage of low-power operation and easy integration with CMOS circuitry. However, most low frequency devices are based on polysilicon structures. The high resistivity of polysilicon at microwave frequencies causes excessive loss and therefore not a suitable material for RF-MEMS. Because of this, most researchers in the field of microwave MEMS devices have used metal structures driven by electrostatic actuation [2]. Most of the research in the microwave MEMS devices has focused on the development of low-loss circuits such as single-pole single-throw (SPST) switches and switched-line phase shifters [30, 18, 60]. The advantage of using MEMS devices over FETs or PIN diodes is their extremely low series resistance, on the order of 0.1 to 0.3Ω as compared to 2 to 6Ω, and

[1] DARPA: Defense Advanced Research Project Agency

[2] SPO: Special Projects Office

[3] MTO: Microsystems Technology Office

their extremely low drive power requirements, on the order of μW as compared with mW. Furthermore, due to the fact that MEMS devices do not contain a semiconductor junction, with the associated non-linearity, they lack any measurable intermodulation distortion [19].

1.1 RF-MEMS Switch

MEMS switches have been fabricated in suspended beam, cantilever, and diaphragm configurations with the bridge height typically 3 to 4 μm above the transmission line, resulting in an actuation voltage of 25 to 100 V. Pacheco et al. have shown that low voltage actuation of 9 to 16 V can be achieved with a gap height of 3 μm by using serpentine cantilever springs at the ends of the beam [38]. This height is necessary in order to reduce the parasitic capacitance of the bridge in the OFF-state (bridge up), and results in a capacitance ratio of 50 to 100 for capacitive switches. MEMS switches have been demonstrated reliably up to 40 GHz with low insertion loss (0.2 to 0.5 dB) and high linearity [30, 19]. The achievable isolation with these switches is typically 20 to 40 dB, depending on the size of the MEMS bridge, with an associated reflection coefficient from -15 to -20 dB.

Current microwave MEMS switches have been designed in both series and shunt configurations with both cantilever and fixed-fixed beams. In the series configuration, shown in Figure 1.1 with a cantilever beam, the isolation is limited by the parasitic capacitance which allows coupling at high frequencies. This can be seen with a simulation in which the MEMS bridge is represented by a series capacitor-inductor-resistor combination as shown in Figure 1.2. Figure 1.3 shows the circuit simulation for the isolation when the switch is up and the return loss when the switch is down. As can be seen, for the capacitance values used, the performance at low frequencies is limited by the return loss rising to -10 dB around 2 GHz and at high frequencies by the isolation rising above -20 dB around 8 GHz. One of the main problems of series capacitive switches is the high return loss, with the switch down, in the frequency range where the isolation is greatest, with the switch up. In Figure 1.3, this occurs at 0.1-2 GHz. It is for this reason that metal-to-metal series MEMS switches are used. Yao et al. presented a series metal-to-metal MEMS switch for use in systems up to 6 GHz with better than 50 dB isolation up to 4 GHz [60].

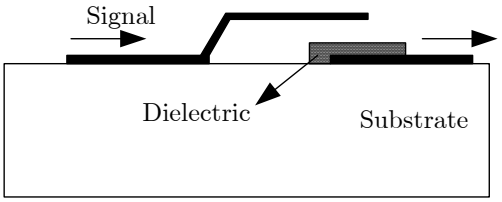


Figure 1.1: Cantilever MEMS bridge in series configuration along a transmission line.

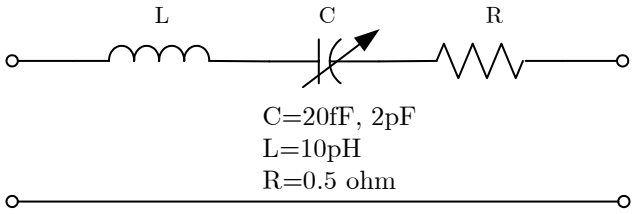


Figure 1.2: Circuit model for a series capacitive MEMS switch with the capacitance varying from 20fF to 2pF.

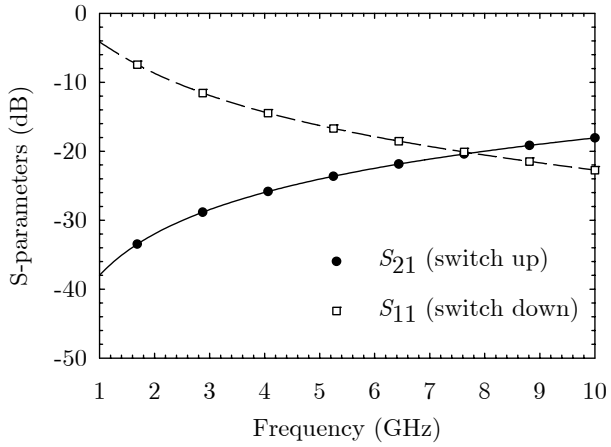


Figure 1.3: Circuit simulation of the series capacitive switch using the model in Figure 1.2.

The shunt switch configuration is shown in Figure 1.4 with a fixed-fixed beam over a CPW line. In this case, the parasitic capacitance limits the high frequency response when the switch is up by producing unwanted reflections. Again, the MEMS bridge can be modeled by a series capacitor-inductor-resistor combination as shown in Figure 1.5. The circuit simulation of this model is shown in Figure 1.6 where the return loss, when the switch is up, and the isolation, when the switch is down, is shown. As can be seen, the low frequency limit is set by low isolation while the high frequency limit is set by high return loss. Because of the high frequency of operation of the shunt configuration, the inductance in the MEMS bridge resonates with the capacitance as seen in the isolation curve in Figure 1.6 Goldsmith et al. [19], have developed a shunt capacitive MEMS switch

with 40 dB isolation, with the switch down, and -15 dB return loss, with the switch up, at 40 GHz. Muldavin et al. have demonstrated that by using several shunt capacitive MEMS switches, the reflections can be tuned out and higher isolation can be achieved as compared to a single switch. The measured results demonstrate a return loss below -15 dB from DC-40 GHz with an isolation of better than 40 dB from 16-40 GHz [33].

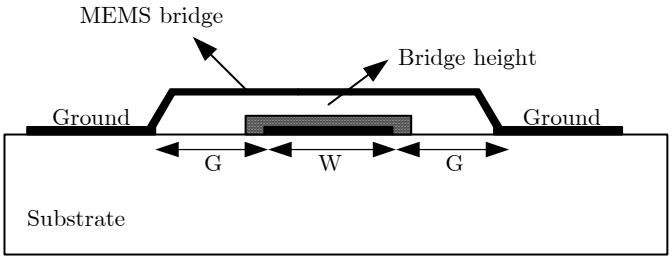


Figure 1.4: Suspended MEMS bridge in shunt configuration over a CPW transmission line.

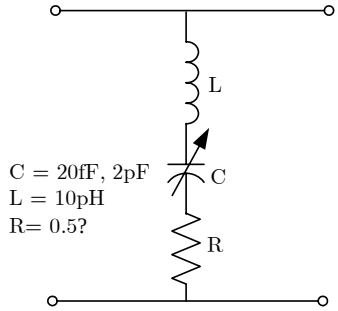


Figure 1.5: Circuit model for a shunt capacitive MEMS switch with the capacitance varying from 20fF to 2pF.

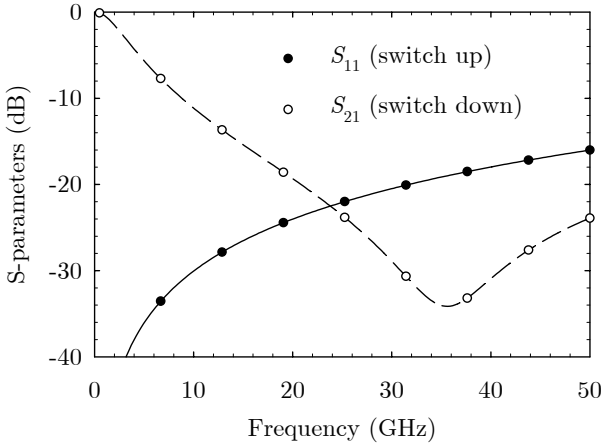


Figure 1.6: Circuit simulation of the shunt capacitive switch using the model in Figure 1.5.

The concept of periodically loaded lines has been researched for use as nonlinear transmission lines since about 1960 [29]. In this case, a transmission line is loaded with millimeter-wave Schottky diodes and is used in voltage-level pulse shaping, picosecond-level sampling, and harmonic multipliers [44, 45]. More recently, the periodically loaded line concept has been used in developing microwave phase shifters using varactor diodes as the capacitive loading [35, 36]. However, diode-based periodically loaded lines are quite lossy at millimeter wave frequencies, due to the series resistance of the Schottky diodes, and cannot be used in low-loss phase shifters and wideband switches above 26 GHz. For these frequencies, MEMS based designs offer excellent performance.

MEMS switch designs have been very similar to standard PIN diode or FET switch networks, with the active device replaced by the MEMS switch. This departure from the traditional approach by incorporating the MEMS switches/varactors was first introduced by Barker et al. In this approach, a CPW transmission line is loaded periodically with MEMS bridges, as shown in Figure 1.7, which act as shunt capacitors/varactors. A microstrip version of the phase shifter was implemented by Hayden et al. The impedance and propagation velocity of the resulting slow-wave transmission line are determined by the size of the MEMS bridges and their periodic spacing. The shunt capacitance associated with the MEMS bridges is in parallel with the distributed capacitance of the transmission line and is included as a design parameter of the loaded line. Thus, the height of the MEMS bridge can be lowered from 3-4μm to 1-1.5μm. An advantage of the lowered height is that the pull-down voltage of the MEMS bridge is reduced to 10 to 20 V. By using a single analog control voltage to vary the height of the MEMS bridges, the distributed capacitive loading on the transmission line, and therefore its propagation characteristics, can be varied. This results in analog control of the transmission line phase velocity and therefore in a true-time delay phase shifter.

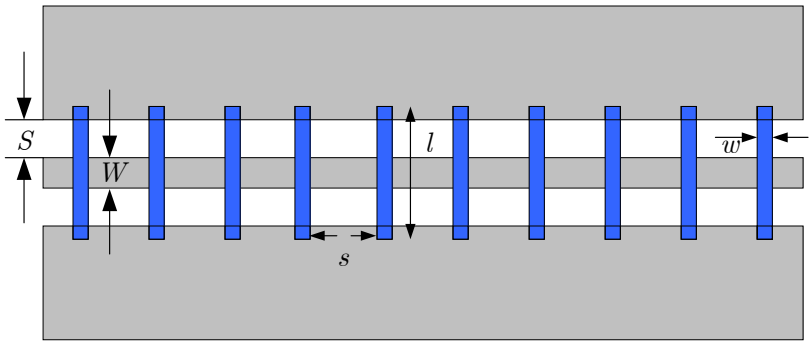


Figure 1.7: Top view of a CPW line periodically loaded by shunt MEMS bridges.

1.2 Thesis Organization

This thesis consists of 5 chapters. Chapter 2 starts with the theory of periodically loaded lines with extensions for the case of using MEMS bridges as the varactors. Both analytic and circuit models are found which provide for both the design and accurate simulation of the distributed lines. Both analog as well as digital true-time-delay (TTD) phase shifter were measured and it is shown that the results agree favorably with published report. Chapter 3 discusses the design, optimization, fabrication and modeling of a impedance matched phase shifter designed to operate through 50GHz. The concept of slow-wave transmission line has been applied to the design of filters and feeding network. Using the measured results a semi-distributed model for the phase shifter is also presented. Furthermore, design considerations for scaling the 50GHz design to *X*-band and *W*-band frequency is suggested. In Chapter 4, the slow-wave unit cell is used in a broad-band tunable transmission line that can provide independent impedance as well as phase tuning. Furthermore, a multi-bit version of the phase shifter is used to realize a on-wafer electronic multi-line TRL calibration set. These circuits are made possible due to the quasi-constant impedance, low loss performance of the slow-wave unit cell. Chapter 5 concludes the thesis with a discussion of the future directions of research for microwave MEMS devices and the distributed MEMS transmission line. Several appendices are included for completeness.

1.3 Contribution

In this work, 1-bit and multi-bit impedance-matched phase shifters are designed on low loss quartz substrate using slow-wave unit cells. Experimental results for a 4.6mm long MEM device indicate 310°/dB for the 1st generation design and 355°/dB for the 2nd generation design. The results represent state-of-the-art performance for TTD phase shifters through 50GHz. There are many applications that utilize phase shifter; however, the slow-wave unit cell is applied herein to the design of tunable transmission line and an electronic multi-line TRL calibration set. To the best of author's knowledge the application demonstrated using tunable slow-wave unit cells is one of the first reported results.

The results for the phase shifter indicate 200% improvement in the figure-of-merit and 40% reduction in size when compared with current state-of-the art designs such as DMTL. However, the number of MEM devices per mm is three times more when compared with the designs based on the DMTL topology. The long term reliability, power handling, packaging, temperature, and switching speed issues need to be addressed. Some of these issues are addressed briefly in final chapter but a thorough analysis is required before making this design more viable for commercial applications.

CHAPTER 2

Theory of Distributed MEMS Transmission Line

Distributed circuits are used in many devices including filters [41], traveling-wave amplifiers [44], phase shifters [36], and non-linear transmission lines [44]. The concept is very useful because the parasitics of the discrete components, such as the gate-to-source capacitance of transistors in traveling-wave amplifiers, or the capacitance of Schottky diodes in non-linear transmission lines, are included as part of the periodic transmission line, thereby resulting in very wideband operation. The transmission-line dimensions can also be designed such that the resulting periodic transmission line will have a 50Ω characteristic impedance.

The distributed MEMS transmission line (DMTL) consists of a high impedance line (> 50Ω) capacitively loaded by the periodic placement of MEMS bridges. This could be done with many different types of transmission lines, however it is most easily implemented using coplanar waveguide (CPW) transmission lines. Figure 3.1 shows the top view of a typical DMTL used in this work. The MEMS bridges have a width w, a length l = W + 2S, and a thickness t. The periodic spacing between the bridges, s, and the number of bridges vary depending upon the application. The DMTL is connected to probe pads via 50Ω CPW feed lines for the purpose of testing.

A result of creating a periodic structure is the existence of a cut-off frequency or Bragg frequency, f_B, near the point where the guided wavelength approaches the periodic spacing of the discrete components [47]. In many of the distributed circuits mentioned, this cutoff frequency can be designed such that it will not limit the device performance since the discrete components will have a comparable maximum frequency [44]. In the case of the distributed MEMS transmission lines used in this work, the self-resonant frequency of the MEMS bridges is not approached and thus the operation is limited by the Bragg frequency of the line.

2.1 Analytical Model of Periodically Loaded Transmission Lines

The general model of a periodically loaded transmission line is shown in Figure 2.1. Assuming complex propagation constant $\gamma = \alpha + j\beta$, where α is the attenuation per section and β is the phase shift per section, a forward wave is represented by:

$$V_{n+1} = V_n e^{-\gamma} \tag{2.1}$$

Using Figure 2.1 the voltages and currents are found to be:

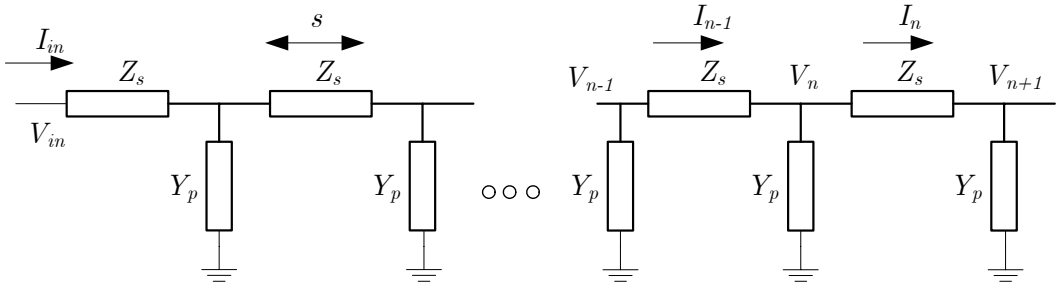


Figure 2.1: General model for a periodic loaded transmission line with series impedance Z_s and shunt admittance Y_p.

$$\begin{aligned} V_n &= \frac{I_{n-1} - I_n}{Y_p} \\ I_{n-1} &= \frac{V_{n-1} - V_n}{Z_s} \quad and \quad I_n = \frac{V_n - V_{n+1}}{Z_s} \end{aligned} \tag{2.2}$$

Substituting the current equations for I_{n-1} and I_n into the voltage equation for V_n, the following equation is found [8]

$$\frac{V_{n-1} + V_{n+1}}{2V_n} = 1 + \frac{Z_s Y_p}{2} = \frac{e^{\gamma} + e^{-\gamma}}{2} = cosh(\gamma) \tag{2.3}$$

Equation 2.3 relates the propagation constant γ to the series impedance of the transmission line (Z_s) and the shunt admittance Y_p. Using these equations the characteristic impedance of the line is found from $Z=V_{in}/I_{in}$. (assuming the line is matched). The half-angle formula for the hyperbolic sine is used in (2.3), the characteristic impedance of the loaded line is found to be [44]: and given by:

$$Z = \frac{V_{n+1/2}}{I_n} = \frac{V_{n-1} - 2V_n + V_{n+1}}{V_n - V_{n+1}} \frac{1}{Y_p} - \frac{Z_s}{2}$$

$$= \frac{Z_s e^{\gamma/2}}{2\,sinh(\gamma/2)} - \frac{Z_s}{2} \tag{2.4}$$

$$Z = \sqrt{\frac{Z_s}{Y_p}} \sqrt{1 + \frac{Z_s Y_p}{4}}$$

If a section of length s of unloaded line is used with characteristic impedance Z_o and effective dielectric constant ε_{eff} then;

$$Z_s = j\omega s L_t; \quad Y_p = j\omega s C_t \tag{2.5}$$

where, $C_t = \sqrt{\varepsilon_{eff}} \left(c\, Z_o\right)^{-1}$ *and* $L_t = C_t {Z_o}^2$ are the per unit length capacitance and inductance respectively, of the unloaded transmission line. Substituting these values in (2.4) gives

$$Z = \sqrt{\frac{L_t}{C_t}} \sqrt{1 - \frac{\omega^2 s^2 L_t C_t}{4}} = \sqrt{\frac{L_t}{C_t}} \sqrt{1 - \left(\frac{\omega}{\omega_B}\right)^2} \tag{2.6}$$

where, $\omega_B = 2 \Big/ s\left(\sqrt{L_t C_t}\right)$ is the Bragg's frequency or the frequency at which the characteristic impedance goes to zero, indicating no power transfer can occur. It can be seen that when $s \to 0$, $\omega_B \to \infty$ and $Z \to \sqrt{L_t / C_t} = Z_o$.

For a DMTL transmission line, the MEMS bridge can be modeled as a shunt capacitor, resulting in a loaded line model as shown in Figure 2.2 where C_b is the shunt capacitance due to the MEMS bridge, and s is periodic spacing of the bridges. Using this model the series impedance is $j\omega s L_t$ and the shunt admittance is $j\omega\left(sC_t + C_b\right)$. The characteristic impedance found using (4) is given by:

$$Z = \sqrt{\frac{sL_t}{sC_t + C_b}} \sqrt{1 - \frac{\omega^2 s L_t \left(sC_t + C_b\right)}{4}} = \sqrt{\frac{L_t}{C_t}} \sqrt{1 - \left(\frac{\omega}{\omega_B}\right)^2} \tag{2.7}$$

The Bragg's frequency for a DMTL transmission line is given by:

$$\omega_B = \frac{2}{\sqrt{sL_t\left(sC_t + C_b\right)}} \tag{2.8}$$

The time delay per section of the loaded-line is determined from (2.3) by assuming a lossless line and using the model in Figure 2.2 [2, 3].

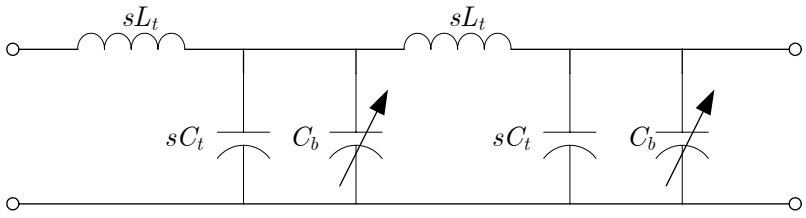


Figure 2.2: Lumped element model of a distributed MEMS transmission line. The MEMS bridges are represented by a variable capacitor C_b. L_t and C_t represent the per unit length inductance and capacitance of the unloaded transmission line, while s is the periodic spacing between bridges.

$$\begin{aligned} \upsilon &= \frac{s}{\tau} = \frac{\omega s}{\beta} \\ &= \frac{\omega s}{cos^{-1}\left(1 - \frac{2\omega^2}{{\omega_B}^2}\right)} \\ &= \frac{\omega s}{\sqrt{sL_t\left(sC_t + C_b\right)}\left(1 + \frac{\omega^2}{6{\omega_B}^2} + \ldots\right)} \end{aligned} \tag{2.9}$$

Where, τ is the time delay per section. From (2.9), it is seen that by varying the MEMS bridge capacitance, C_b, the phase velocity of the transmission line (υ) can be varied resulting in a varying delay line or true-time delay (TTD) phase shifter.

Since the characteristic impedance (Z) of the DMTL affects S_{11}, the lower and upper bound for Z using (2.7) is calculated to be 36Ω and 69Ω respectively, for S_{11} < -10dB. When the line is loaded (or Z=36Ω), the maximum value of C_b is typically less than 0.1pF, for s=200μm, and an unloaded impedance of 100Ω. To obtain this value of C_b, the width of the bridge (w) is typically 20-70μm and the length (l) is typically less than 300μm. Using a quasi-static approximation, the inductance of the bridge (L_b) can be calculated by assuming the bridge as a microstrip line suspended on a 2-3μm thick substrate with air (ε_r=1) as the dielectric. For the footprints of the bridge aforementioned, L_b is typically within 10-30pH.

Table 2.1 shows the calculated Bragg frequencies versus several values of bridge inductance for a line with an unloaded impedance of 100Ω, a periodic spacing of 200 μm, and a bridge capacitance of 40 fF on silicon (ε_r=11.7), quartz (ε_r=3.8), and air dielectric (ε_r=1). It is seen from the table that including the series inductance of the bridge has a significant effect on the position of the Bragg frequency.

Table 2.1: Effect of series inductance (L_b) on the Bragg's frequency.

	f_B (GHz)		
L_b (pH)	Air (ε_r=1)	Quartz (ε_r=3.8)	Silicon (ε_r=11.7)
0	224GHz	145 GHz	89 GHz
10	189 GHz	129 GHz	83 GHz
20	164 GHz	116 GHz	77 GHz
30	147 GHz	106 GHz	73 GHz

2.2 Distributed Transmission Line Loss

When the impedance is changed, the loss of the line is also changed due to a change in the amount of current on the line for the same amount of power. For example, if a high impedance line is capacitively loaded to a lower impedance, the current on the lower impedance line will be higher, thus increasing the I^2R losses. This can be seen directly by considering the complex propagation constant for a lossy transmission line. If the transmission line is represented by series inductance and resistance per unit length, L_t and R_t, and by a shunt capacitance and admittance per unit length, C_t and G_t, respectively, then the propagation constant is given by [10]:

$$\gamma = \sqrt{(R_t + j\omega L_t)(G_t + j\omega C_t)} \tag{2.10}$$

For a low loss line where $R_t \ll j\omega L_t$ and $G_t \ll j\omega C_t$, the propagation constant can be approximated as:

$$\gamma \approx j\omega\sqrt{L_t C_t} + \frac{1}{2}\sqrt{L_t C_t}\left(\frac{R_t}{L_t} + \frac{G_t}{C_t}\right) = \alpha + j\beta \tag{2.11}$$

Assuming the characteristic impedance can be approximated by $Z = \sqrt{L_t / C_t}$, the attenuation constant α is:

$$\alpha = \frac{R_t}{2Z} + \frac{G_t Z}{2} \tag{2.12}$$

In a planar transmission line such as microstrip or CPW, R_t represents conductor loss while G_t represents dielectric loss. For the lines considered in this work (on low-loss substrates at mm-wave frequencies), the conductor loss dominates and the attenuation constant can be approximated as $\alpha = R_t / 2Z$. Thus, a change in the characteristic impedance from a high impedance to a low impedance will increase the loss by a factor of the ratio of the impedances.

The transmission loss can also be included in the model of the distributed MEMS transmission line (Figure 2.2) by including a resistance R_s in series with the line inductance, sL_t. In this case the series impedance becomes $Z_s = R_s + j\omega sL_t$. To find the attenuation constant, (2.3) is expanded to give:

$$\begin{aligned} \cosh(\gamma) &= \cosh(\alpha)\cos(\beta) + j\sinh(\alpha)\sin(\beta) \\ &= 1 - \frac{\omega^2 LC}{2} + j\frac{\omega R_s C}{2} \\ &= 1 - 2\left(\frac{\omega}{\omega_B}\right)^2 + j\left(\frac{\omega}{\omega_B}\right)\frac{R_s}{Z} \end{aligned} \tag{2.13}$$

where $L = sL_t$, $C = sC_t + C_b$, and the low frequency approximations have been used for ω_B and Z. By equating the real parts and assuming α is small ($\cosh(\alpha) \approx 1$), the equation for the phase delay per section is found to be $\beta = cos^{-1}\left(1 - 2\omega^2 / {\omega_B}^2\right) \approx 2\omega / \omega_B$ .To find the attenuation per section, the imaginary parts are equated to give:

$$sinh(\alpha) \approx \alpha = \frac{(\omega / \omega_B) R_s / Z}{sin(2\omega / \omega_B)} \approx \frac{R_s}{2Z} \tag{2.14}$$

Where Z is now the impedance of the loaded line. This result matches what was derived earlier in the unloaded case. The only difference is that in the unloaded case, α is the

attenuation per unit length (Np/m), while in the distributed case, α is the attenuation per section (Np).

The effect of a series resistance in the bridge can be taken into account by placing a resistor R_b in series with the bridge capacitance in Figure 2.2. In this case, (2.3) becomes:

$$\begin{aligned} cosh(\alpha + j\beta) &= 1 + \frac{j\omega s L_t}{2}\left(j\omega s C_t + \frac{j\omega s C_b + \omega^2 R_b {C_b}^2}{1 + \omega^2 {R_b}^2 {C_b}^2}\right) \\ &= 1 - 2\left(\frac{\omega}{\omega_B}\right)^2 + j\left(\frac{\omega}{\omega_B}\right)^3 \frac{4R_b}{Z}\left(\frac{C_b}{sC_t + C_b}\right)^2 \end{aligned} \tag{2.15}$$

where $\omega_B = 2/\sqrt{sL_t\left(sC_t + C_b\right)}$, $Z = \sqrt{sL_t/\left(sC_t + C_b\right)}$ and a low frequency approximation has been used for $1 + \omega^2 {R_b}^2 {C_b}^2 \approx 1$. Using $\omega < \omega_B$, the propagation constant is found to be:

$$\begin{aligned} \alpha + j\beta &= cosh^{-1}\left(1 - 2\left(\frac{\omega}{\omega_B}\right)^2 + j\left(\frac{\omega}{\omega_B}\right)^3 \frac{4R_b}{Z}\left(\frac{C_b}{sC_t + C_b}\right)^2\right) \\ &\approx j2\frac{\omega}{\omega_B} + \frac{R_b Z {C_b}^2 \omega^2}{2} \end{aligned} \tag{2.16}$$

Combining this loss with the transmission line loss, the total loss per section for a distributed MEMS transmission line is [44]:

$$\alpha = \frac{R_s}{2Z} + \frac{R_b Z {C_b}^2 \omega^2}{2} \tag{2.17}$$

For a line with an unloaded impedance of 100Ω, an unloaded effective dielectric constant of 2.4, a periodic spacing of 200 μm, a bridge capacitance of 34fF, a loss of 0.6dB/cm (R_t=15Ω/cm) at 40 GHz for the unloaded line, and a bridge resistance of 0.1Ω at 40 GHz the loss from the transmission line is 1.6 dB/cm at 40 GHz respectively. While the loss due to the bridge resistance is only 0.07 dB/cm ($< 4\%$) at 40 GHz. Thus, for these typical parameters, the loss is dominated by the transmission line loss.

Radiation loss is also present in an unloaded CPW line on a thick dielectric substrate because the wave velocity of the transmission line is greater than the phase velocity of the waves in the dielectric [46]. This loss is given by:

$$\alpha_{\text{rad}}=\left(\frac{\pi}{2}\right)^5 \frac{1}{\sqrt{2}} \frac{\left(1-\varepsilon_r\right)^2}{\sqrt{1+\varepsilon_r}} \frac{f^3(W+2S)^2}{c^3 K(k)K(k')}$$
$$k=\frac{W}{W+2S} \tag{2.18}$$
$$k'=\sqrt{1-k^2}$$

where W+2S is the ground-to-ground spacing of the CPW line and K(k) is the complete elliptic integral of the first kind. The radiation into the substrate primarily occurs around the angle:

$$cos\,\psi=\frac{k_z}{k_d} \tag{2.19}$$

Where k_z is the propagation constant of the line and k_d is the propagation constant in the dielectric. To avoid radiation and radiation loss, the wave velocity of the transmission line should be slower than the phase velocity of the dielectric. The angle necessary to phase match the wave on the transmission line to the wave in the dielectric becomes imaginary indicating that radiation, and therefore radiation loss, cannot occur. Alternatively, a slow-wave mode propagation (or no radiation) results if the effective dielectric constant of the DMTL is greater than the relative dielectric constant of the substrate. Figure 2.3 shows the extracted effective dielectric constant ($\varepsilon_{extract}$) of a DMTL versus the center conductor width for three dielectric constant with Z=100Ω, s=200μm and C_b= 40fF (assuming maximum loading). As seen in Figure 2.3, $\varepsilon_{extract} > \varepsilon_r$ for center conductor widths less than 80μm (Z=64Ω) on silicon, while $\varepsilon_{extract} > \varepsilon_r$ for W≈ 370μm (Z=60Ω) on quartz and no radiation is possible for the entire range of conductor widths on an air substrate. The decrease in $\varepsilon_{extract}$ is because for a given CPW pitch, the phase shift per unit length decreases as impedance decreases.

2.3 Circuit Model of DMTL

While the analytic model presented in section 2.2 provides a good general understanding of the operation of periodically-loaded distributed lines, it is desirable to have a circuit model that can be used in a linear circuit simulator. The simulator used for the modeling of the DMTL is Agilent's Advanced Design System (ADS). Using the circuit elements available in

ADS, the model for a single section of the DMTL is shown in Figure 2.4. The model consists of a section of physical transmission line to represent the unloaded CPW line and a capacitor-inductor series combination shunted across the transmission line to represent the MEMS bridge. The entire DMTL is modeled in the simulator by cascading the necessary number of sections. In this approach, the unloaded line impedance, Z_o, the spacing of the MEMS bridges, s, the number of sections, n, and the effective dielectric constant of the unloaded line, ε_{eff} are determined from the physical dimensions of the DMTL being modeled. The unloaded line attenuation, A, bridge capacitance, C_b, and bridge inductance, L_b, are all varied to fit the model to the measured data. The attenuation in the physical transmission line model is specified at a particular frequency and then follows a $\sqrt{f}$ variation.

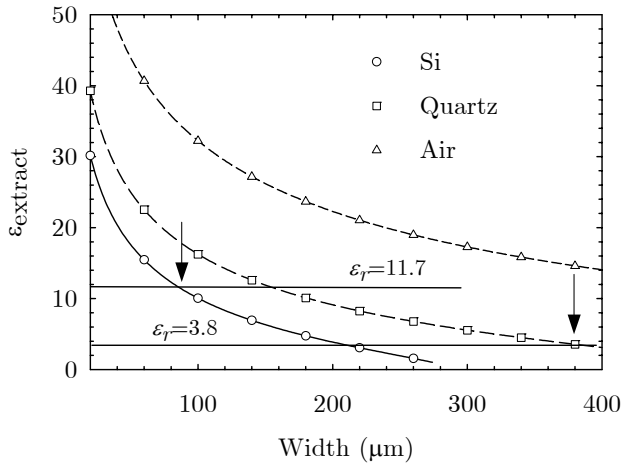


Figure 2.3: Extracted effective dielectric constant ($\varepsilon_{extract}$) for the DMTL versus center conductor width at 40GHz. The relative dielectric constant of silicon (ε_r=11.7) and quartz (ε_r =3.8) are shown for reference.

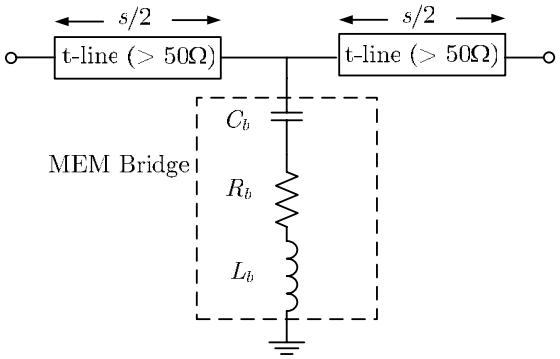


Figure 2.4: Circuit model used for a section in the DMTL simulation. Z_0 of the transmission line (t-line) is the unloaded line impedance, s is the periodic spacing of the MEMS bridges, C_b is the MEMS bridge capacitance.

2.4 DMTL Phase Shifter and Results

As mentioned in Section 2.2, the DMTL can be used as a true-time delay (TTD) phase shifter since a change in the MEMS bridge capacitance changes the phase velocity of the line (equation 2.9). The change in the bridge capacitance is achieved by applying a single bias voltage to the center conductor of the DMTL with the CPW ground planes acting as a DC ground as well. This application is demonstrated in Figure 2.5 (a)–(c). A DMTL phase shifter with 11 bridges (40μm wide) spaced at 700μm is simulated using the model shown in Figure 2.4. The unloaded line impedance is 65Ω (W = 60μm and S = 180μm) with an effective dielectric constant of 6.1. Figure 2.5 (b) and (c) shows the measured and modeled data for S_{11} and S_{21} in the high capacitance state (down state) and the low capacitance state (up state) respectively. It is seen from these figures that the S_{11} of the DMTL in the down state has more closely spaced nulls, indicating that the line is electrically longer than it is in the up state. Since the physical length of the DMTL has not changed, the phase velocity of the line has decreased, as expected. The relative phase between the two states or the net phase shift ($\Delta\phi$) is found from the change in the phase constant given by:

$$\begin{aligned}\Delta\phi &= \beta_1 - \beta_2 \\ &= \omega\left(\frac{1}{\upsilon_1} - \frac{1}{\upsilon_2}\right)\end{aligned} \tag{2.20}$$

Using (2.9) for the phase velocity and a capacitance ratio C_r ($= C_{dn} / C_{up}$)$\Delta\phi$ per unit length is given by:

$$\begin{aligned}\Delta\phi &= \omega\sqrt{L_t C_t}\left(\sqrt{1+\frac{C_{bo}}{sC_t}} - \sqrt{1+\frac{C_r C_{bo}}{sC_t}}\right) \\ &= \frac{\omega Z_o\sqrt{\varepsilon_{eff}}}{c}\left(\frac{1}{Z_{lu}} - \frac{1}{Z_{ld}}\right)\end{aligned} \tag{2.21}$$

$\Delta\phi$ for three different values of C_r and measured $\Delta\phi$ versus frequency is shown in Figure 2.5 (a). The SEM picture of the fabricated device is also shown in this figure. As seen from this figure, $\Delta\phi$ increases linearly with frequency as expected for a TTD type phase shifter and is within 5% of the predicted $\Delta\phi$ with C_r=1.15. There is some deviation from this linear increase at approximately 30GHz which is a result of approaching the Bragg

frequency (calculated to be 67 GHz). The maximum $\Delta\phi$ is 170° at 40 GHz with an associated insertion loss of 1.75 dB.

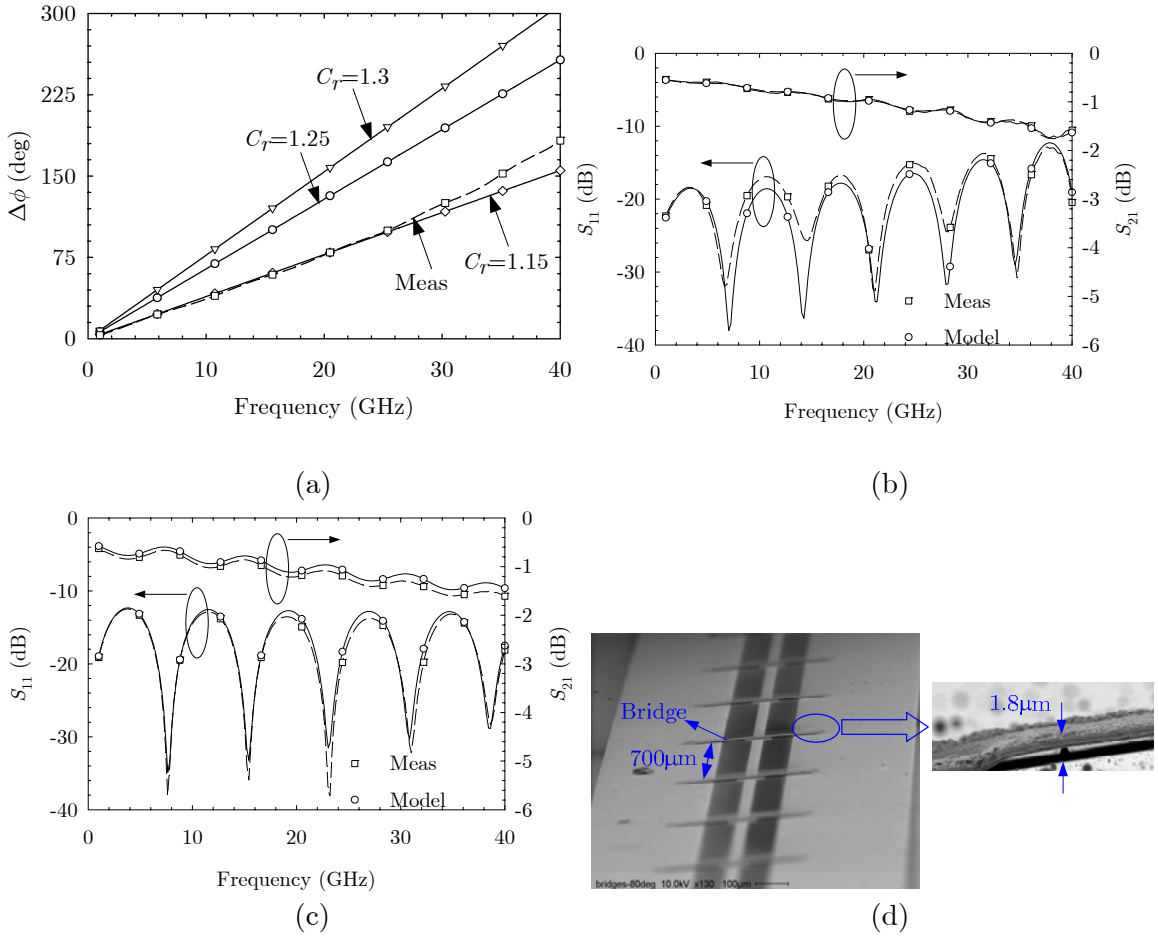


Figure 2.5: Measured (a) phase shift ($\Delta\phi$); (b) S_{11} and S_{21} in the down-state; (c) S_{11} and S_{21} in the up-state, d) SEM picture of the fabricated device on silicon. The DMTL comprises of 11 bridges (40µm wide) spaced at 700µm (total length = 7.84mm).

The figure of merit for the phase shifter is the phase shift per dB ($\Delta\phi$/dB); this figure is achieved by dividing (2.21) by (2.17). Figure 2.6 (a) shows a measured $\Delta\phi$/dB of 97°/dB and indicates good agreement with the modeled data from 1-30GHz. However, for frequencies greater than 30GHz, the model data is 10-15°/dB higher than the measured value. This is because the closed-form equations for the conductor loss of the uniform CPW lines sections (α) used in the ADS circuit simulator under estimates the measured data. Usually, this is adjusted by multiplying α with a constant (F_c) determined by fitting the model to the measured data. No compensation was used in the modeled data shown in

Figure 2.6 (F_c=1). A detailed analysis of CPW conductor loss and its effect on phase shifter performance is discussed in Chapter 3.

The change in bridge capacitance also changes the characteristic impedance, as indicated in (2.7). This effect can be seen in Figure 2.5 (b) in which the peak in the low-frequency reflection coefficient is seen to change from -18.4 to -12.7 dB. This peak in reflection coefficient occurs at a frequency where the DMTL is a quarter-wave length long and the input impedance, seen from the 50Ω feed line, is at a maximum given by:

$$Z_{in} = \frac{Z^2}{50} \tag{2.22}$$

Where Z is the characteristic impedance of the DMTL. Thus, the characteristic impedance of the DMTL changes from 56Ω to 48Ω. The measured DMTL in Figure 2.5 has a capacitance ratio (C_{dn}=C_{up}) of approximately 1.15-1.2, so the impedance change is relatively small. However, if this capacitance ratio could be made much larger (C_r >5), the characteristic impedance of the DMTL would change by significant amounts causing undesirably large reflection coefficients.

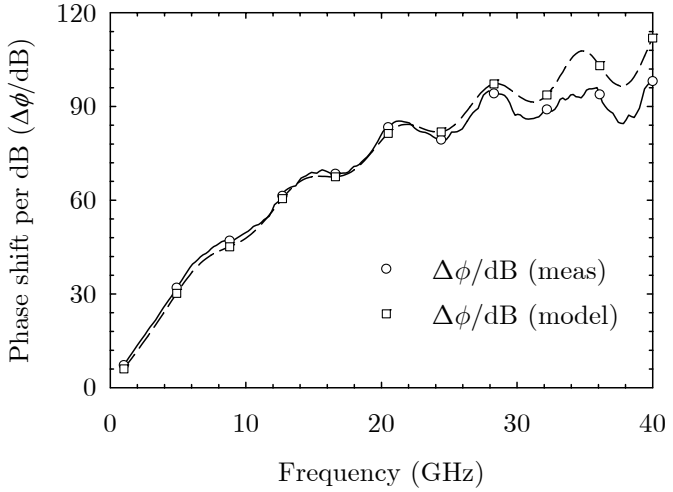


Figure 2.6: Comparison of phase shift per dB between measured and modeled DMTL phase shifter.

In this case, the DMTL should be designed such that the variation in characteristic impedance results in the same maximum allowable reflection coefficient in the low and high bridge capacitance states. For example, if it is desired to have the maximum

reflection coefficient below -15 dB, then the characteristic impedance should be 60Ω in the low capacitance state and 42Ω in the high capacitance state. In general, the upper and lower bounds of the characteristic impedance, for a given reflection coefficient, are given by:

$$Z_{lu} = Z_0 \left(\frac{1+S_{11}}{1-S_{11}} \right)^{1/2} \qquad and \qquad Z_{ld} = Z_0 \left(\frac{1-S_{11}}{1+S_{11}} \right)^{1/2} \tag{2.23}$$

Where Z_{ld} and Z_{lu} are the DMTL impedance in the high and low capacitance states, respectively.

Using (2.7) and (2.23), the minimum and maximum bridge capacitances are found to be:

$$C_{min} = \frac{sL_t}{50^2}\left(\frac{1-S_{11}}{1+S_{11}} \right) - sC_t \quad and \quad C_{max} = \frac{sL_t}{50^2}\left(\frac{1+S_{11}}{1-S_{11}} \right) - sC_t \tag{2.24}$$

Using (2.24), the capacitance ratio C_r is found to be:

$$C_r = \frac{C_{max}}{C_{min}} = \frac{{Z_o}^2\left(\frac{1+S_{11}}{1-S_{11}} \right) - 50^2}{{Z_o}^2\left(\frac{1-S_{11}}{1+S_{11}} \right) - 50^2} \tag{2.25}$$

Where $Z_o = \sqrt{L_t / C_t}$ is the characteristic impedance of the unloaded transmission line. Figure 2.7 shows this capacitance ratio versus the maximum allowable reflection coefficient for different unloaded-line impedances. It is noted that the capacitance ratio is independent of the substrate dielectric constant. Furthermore, this calculation is based on the low-frequency impedance and does not account for the effects of approaching the Bragg frequency. It is seen that the usable capacitance ratio for a maximum reflection of -13 dB is around 3 for a 100 Ω unloaded impedance.

The Bragg frequency is an important design parameter and introduces non-linearity in $\Delta\phi$ if f_B is close to the maximum frequency of operation, thereby reducing the bandwidth of a DMTL as a TTD phase shifter. For the design parameters used in Figure 2.5 and using (2.21) and (2.7) the non-linear effects due to f_B are shown in Figure 2.8. As seen from this figure, for f_B=1.5f_{max} the linear range of operation is limited to less than 20GHz, while the

bandwidth is improved up to 25GHz if f_B=1.8f_{max}. Furthermore, the loaded and the unloaded impedance fall off quickly when f_B is closer to f_{max} as noticed in Figure 2.9. Therefore, to increase the linear range of operation, f_B should be increased ($f_B \geq 2f_{max}$). This is achieved by decreasing the spacing between the bridges. The spacing (s) is obtained by solving (2.7) and (2.8), with the assumption that f_B is defined at the lowest impedance state (Z_{ld} or high capacitance state).

$$s = \frac{Z_{ld}c}{\pi f_B Z_o \sqrt{\varepsilon_{eff}}} \tag{2.26}$$

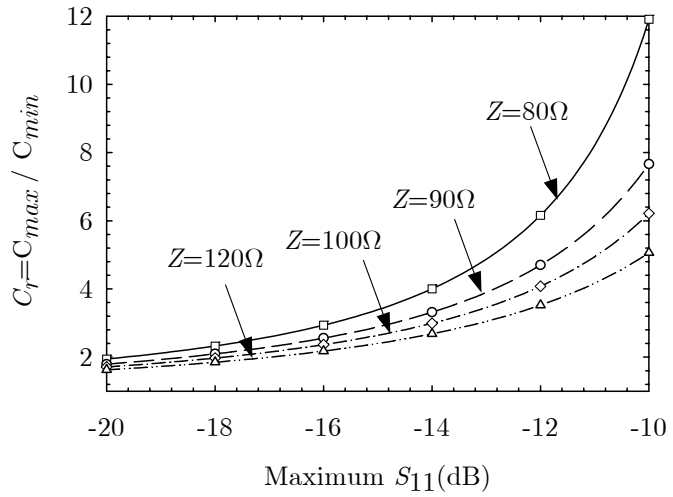


Figure 2.7: Capacitance ration versus maximum allowable S_{11} (dB) for unloaded impedances of 80, 90, 100, and 120Ω.

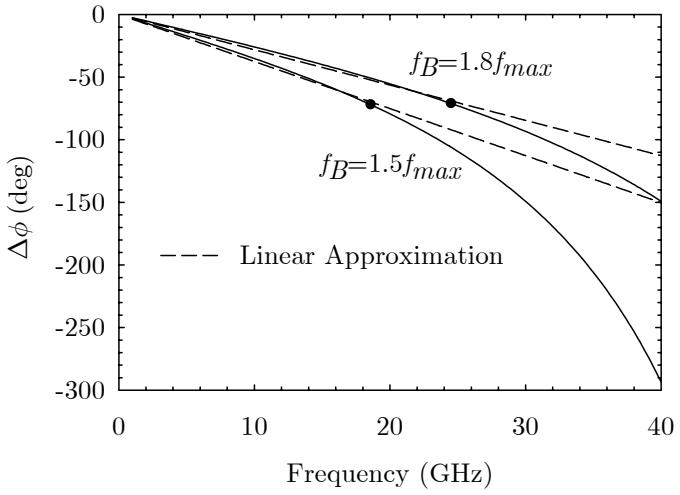


Figure 2.8: Effect of Bragg frequency on the linear range of $\Delta\phi$. f_{max}= 40GHz, Z_{lu}=61Ω, s=700μm.

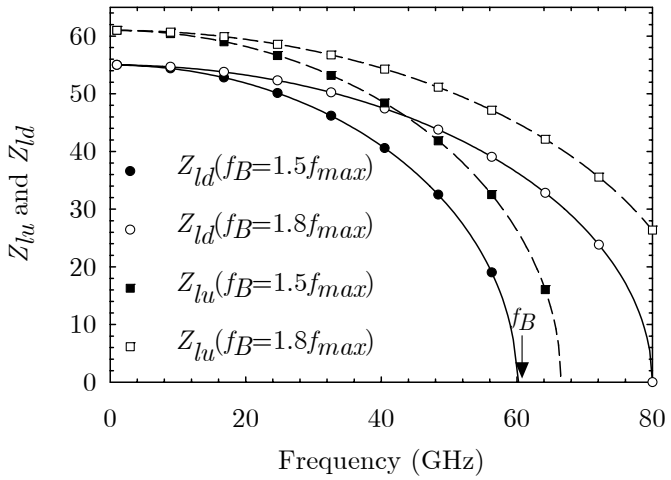


Figure 2.9: Effect of Bragg frequency on the loaded (solid lines) and unloaded impedance (dashed lines) for f_B=1.5 and $1.8f_{max}$. The model parameters used in Figure 2.5 is used herein.

2.5 MEM Capacitor Design

The actuator system used to move the MEMS switches in this work is the electrostatic force. The electrostatic force between the MEMS switch and the signal conductor of the transmission line is the result of a simple voltage potential between them, as exists between the plates of a capacitor under voltage [26]. This force is found by evaluating the power delivered to the time dependent capacitance of the MEMS switch [56]. The capacitance of the MEMS switch is given by:

$$C_b = \frac{\varepsilon_o W w}{h} + C_f \tag{2.27}$$

where W is the width of the signal conductor, w is the width of the MEM bridge, and h is the suspended height as shown in Figure 2.6 (b). The total capacitance of the bridge to the signal conductor is a combination of the parallel plate approximation and the component (C_f), which accounts for the fringing fields. Typically, the value for C_f is found by fitting the two port [S]-parameters of the model (Figure 2.4 with s=0) with a full wave electromagnetic simulation. In this work, C_f values were found to vary within 20% to 25% of C_b.

The applied force to the MEMS switch is shown below and can be written in terms of the switch's physical dimensions using the capacitance equation above:

$$F = \frac{1}{2} V^2 \frac{dC(h)}{dh} = -\frac{1}{2} V^2 \frac{\varepsilon_o W w}{h^2} \tag{2.28}$$

By equating electrostatic force in (2.28) to the mechanical restoring force of the capacitor at height h, and solving for the voltage, a closed form solution versus the applied voltage up to an instability point is found to be:

$$\begin{aligned} &\frac{1}{2} V^2 \frac{\varepsilon_o W w}{h^2} = k\left(h_o - h\right) \\ &V = \sqrt{\frac{2kh^2\left(h_o - h\right)}{\varepsilon_o W w}} \end{aligned} \tag{2.29}$$

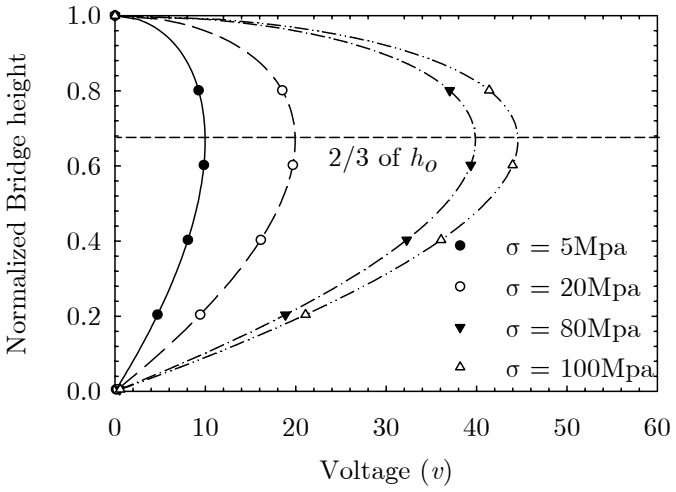
Where, h_o is the original height, k is the spring constant of the MEMS bridge. The general expression for a suspended beam is [33]:

$$k = \frac{32Ewt^3}{L^3}\left(\frac{1}{2-(2-x)x^2}\right) + \frac{8\sigma(1-\nu)wt}{L}\left(\frac{1}{2-x}\right) \tag{2.30}$$

Where, $x = W/L$, E is the Young's modulus of the bridge, σ is the biaxial residual stress on the bridge, t is the thickness of the bridge, ν is the Poison's ratio, L is the length of the bridge. The solution for the voltage versus bridge height is shown in Figure 2.10. In this figure, an instability at 2/3 h_o due to the positive feedback results from the constant voltage effect on charge in the bridge. This instability point may also be found by taking the derivative of (2.29) with respect to h. Because the switch membrane quickly snaps to the signal conductor at this instability point, it is called the pull-in voltage, V_p. The data in Figure 2.15 below the instability point represents the new pull down voltage if, after pulling the switch all the way to the signal conductor, a mechanical stop is placed at a height below the instability point.

By definition, the pull-in voltage V_p is found to be:

$$V_P = V\left(\frac{2}{3}h_o\right) = \sqrt{\frac{8kh_o^{\,3}}{27\varepsilon_o W w}} \tag{2.31}$$



Residual Stress, σ (Mpa)	k (N/m)
5	2.6
20	10.3
80	41.5
100	51.9

Figure 2.10: Normalized switch height versus applied voltage (normalization factor = original height=2μm) for L=500μm, W=100μm, w=80μm, E=80GPa, ν=0.4, t=1μm).

The pull-in voltage represents a limitation for "analog" type DMTL phase shifter design. Due to this instability, it is clear that a switching ratio, C_r, is limited to 1.5 because beyond that voltage, the bridge snaps down and a very high (20-80) capacitance ratio results. For phase shifter based on DMTL topology require typical switching ratios (Figure 2.7) of 2-3. The fringing capacitance typically does not change with height, therefore, practical capacitance ratio is around 1.3. An "analog" design consists of any DMTL phase shifter designed for a maximum capacitance ratio of C_r=1.3. Because the capacitance ratio can be adjusted to be anywhere from 0-1.3 based on the voltage applied, the phase shift which results can be considered analog due to the infinite number of states obtainable.

A more stable design is to use "digital" type tuning because the phase shift and the performance can be predicted with greater accuracy than for the "analog" alternatives. The DMTL phase shifter can be made "digital" in several ways; two are mentioned here. In the first method, a very thick dielectric is used to limit the travel of the MEMS switch. The capacitance of the MEMS switch in the up and down state is (ignoring the effect of fringing capacitance):

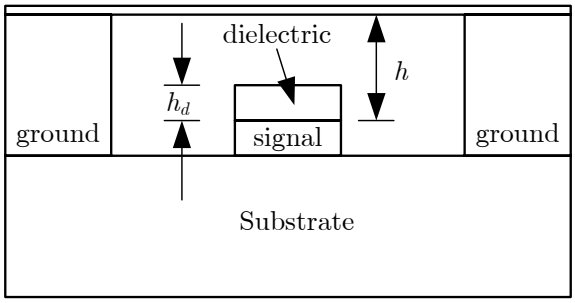


Figure 2.11: Schematic of a digital implementation using very thick dielectric (h_d) for digital operation.

$$C_{up}{}^{-1} = \left(\frac{\varepsilon_o W w}{h - h_d}\right)^{-1} + \left(\frac{\varepsilon_o \varepsilon_r W w}{h_d}\right)^{-1}$$
$$C_{up} = \frac{\varepsilon_o \varepsilon_r W w}{(h - h_d)\varepsilon_r + h_d}; \qquad C_{dn} = \frac{\varepsilon_o \varepsilon_r W w}{h_d} \tag{2.32}$$

Using (2.32) the capacitance ratio C_r ($= C_{dn} / C_{up}$) is plotted for nitride (ε_r=7.6) and SiO_2 (ε_r=4). This method presents a couple of challenges, the first of which is the required dielectric thickness. A typical design with capacitance ratio of $C_r = 2.5$ and a suspended switch height, h, of 1.5 to 2μm is required for low-voltage electrostatic actuation. Using the equation above, oxide dielectric must be 1.3-1.5μm and the nitride dielectric must be 1.2-1.6μm, which are unrealistically thick. Furthermore, thick layers underneath the MEMS switch present additional challenge in MEMS bridge fabrication. Since the sacrificial layer follows the contours of the materials below it, a large step height change will result in additional stress in the bridge and one of the reliability concerns from a fabrication standpoint.

One of the biggest challenges in using thick dielectrics is the switching ratio instability introduced. If the switch membrane and dielectric layer below it are not perfectly smooth, the capacitance measured will be quite lower than the capacitance expected from the parallel plate approximation. Charge buildup in the dielectric can worsen this condition because moving charges in the dielectric cause the membrane to move on top of the dielectric, causing the capacitance to change with time. Since a stable down-state capacitance is required for a "digital" design, it may be argued that the thick dielectric method is not the best solution.

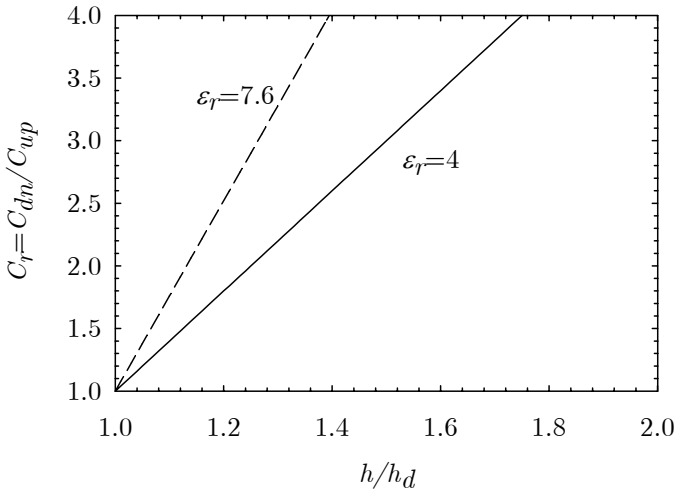


Figure 2.12: Capacitance ratio versus normalized height of the dielectric.

The second "digital" implementation method uses a static capacitor, C_s, in series between the MEMS switch and the ground conductor. The total load capacitance, C_L, on the transmission line is the series combination of the two capacitors:

$$C_L = \frac{C_b C_s}{C_b + C_s} \tag{2.33}$$

There are two states for the MEMS bridge: up and down (pulled down completely by the electrostatic force). When the switch is pulled down, the capacitance is on the order of 1 3 pF whereas in the up state it is on the order of 10-100 fF. Therefore, when the MEMS switch is in the down-state position, the loaded capacitance, C_L, experienced by the line is dominated by the static capacitor, C_s, and $C_L\, C_{bd} \sim C_s$. When the MEMS switch is in the up-state position, the capacitance seen by the line is C_{bu} in series with C_s. The distributed capacitance can therefore be "discretely" controlled by the independent choice of the MEMS switch upstate capacitance, C_{bu} and the static capacitance, C_s and tends towards C_{bu}. Since the desirable switching ratio is on the order of 2-3, the bridge capacitance is designed to be equal to 1-0.5 times that of the static capacitor. As a result of adding the static capacitor, the required MEMS switch loading capacitance becomes larger and thus easier to fabricate. Furthermore, in comparison to the thick dielectric method, the stability of down state capacitance is greatly improved. The switching ratio could be anywhere between 20-80. The stabilization capacitor makes this factor relatively insignificant because

the static capacitance, C_s, dominates in the down-state position and this capacitance can be consistently fabricated.

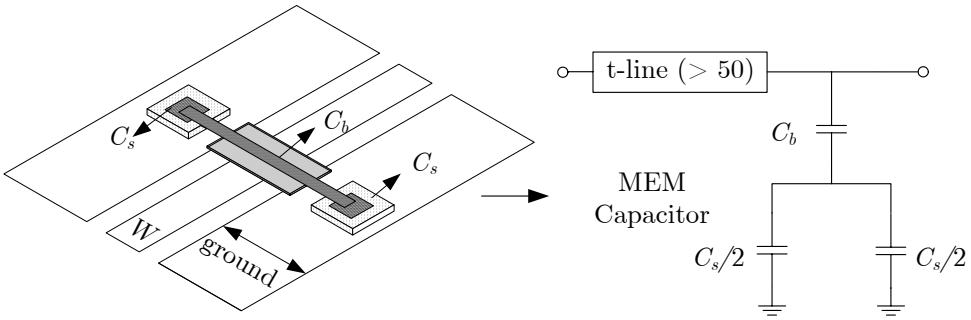


Figure 2.13 : Unit cell representation of a DMTL that utilize static capacitor in series with the bridge. This type of configuration is used in a "digital" type tuning.

When discrete static capacitors are required, their loss is of importance, as will be described in the following section. The capacitors can be implemented using standard metal-insulator-metal (MIM) capacitors, or for higher Q, the MIM capacitors can be replaced with metal-air-metal (MAM) capacitors. The use of MAM capacitors for improving the Q is discussed in Chapter 3, where these high Q capacitors are used in the design of slow-wave phase shifters.

2.6 Non-Uniform Transmission Line Loaded Phase Shifter Modeling and Results

NTL's have been used widely in many applications that include impedance matching [66], pulse shaping [67], and analog signal processing [68]. NTL's also exist in many VLSI interconnection structures to provide smooth connections between high-density IC chips and the chip carriers [70], [71].

This section provides experimental results of distributed MEMS transmission line phase shifters that utilize non-uniform transmission line (NTL) connecting sections between MEM capacitors. The NTL based phase shifter use digital type varactor tuning as aforementioned and was designed on a 400μm thick high resistive silicon substrate ($\rho > 2000\Omega$-cm).

One of the advantages of using silicon as the substrate is that the net phase shift ($\Delta\phi$) from equation (2.21) is directly dependent on $\sqrt{\varepsilon_{eff}}$. Therefore, a phase shifter on a silicon

substrate results in more phase shift per unit length than a DMTL on a quartz substrate. Table 2.2 shows the design parameters for a DMTL phase shifter with S_{11} <-15dB and $f_B \approx 1.8 f_{max}$ on three substrates. The optimum choices for unloaded impedance are approximately 107, 95, 71Ω for air, quartz, and silicon substrates. The optimization procedure is described in Chapter 3.

Table 2.2: DMTL phase shifter with 360° phase shift for design parameters on air, quartz and silicon substrates.

f_{max}=35 GHz

Substrate	Air (ε_r =1)	Quartz (ε_r =3.8)	Silicon (ε_r =11.7)
W (μm)	300	100	30
S (μm)	100	100	60
Z_o (Ω)	107	95	71
C_{bo} (fF)	100	86	27
C_r	2.15	2.35	4.2
Length per 360° (mm)	12.8	9.3	7.4

Improvement in $\Delta\phi$ is achieved by using NTL sections between the MEM bridges. The schematic (unit cell) of two designs is shown in Figure 2.14 (a) and the fabricated phase shifter (comprised of 10 cascaded sections) is shown in Figure 2.14(b). In order to use the transmission line model, the impedance variation between two discrete points is required and described by the following polynomial:

$$Z_c(x) = Z_c(0)(1+kx), \qquad 0 \le x \le l$$
$$\beta_o = \frac{\omega}{c} \tag{2.34}$$

Where, l is the length of the non-uniform transmission line section. $Z_c(0)$ is the characteristic impedance at the input to the NTL. The characteristic impedance at any given point is related to the line parameters by:

$$
\begin{aligned}
&Z_c(x) = \sqrt{\frac{L_t\,(x)}{C_t\,(x)}} \\
&\textit{where} \\
&L_t(x) = \sqrt{L_t\,(0)\,C_t\,(0)}\Big[Z_c\,(0)(1+kx)\Big] \\
&C_t(x) = \frac{\sqrt{L_t\,(0)\,C_t\,(0)}}{\Big[Z_c\,(0)(1+kx)\Big]}
\end{aligned}
\tag{2.35}
$$

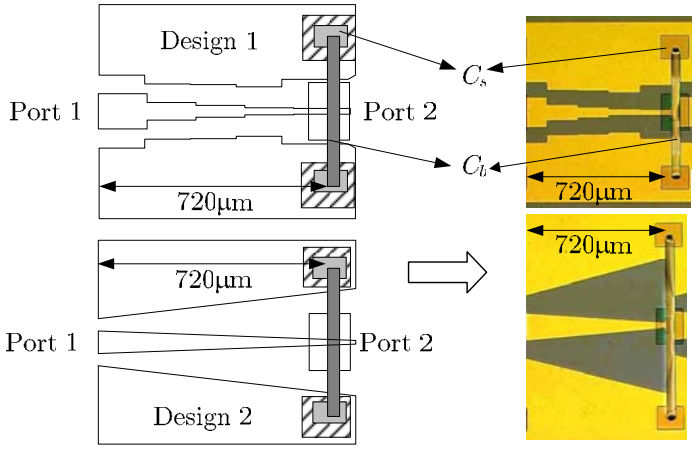
In design 1, the impedance of a distributed line between two adjacent MEMS capacitor is increased in steps of 10Ω from 50Ω to 90Ω making it a 5–section stepped impedance transformer. Each impedance section is 145μm long and the overall length of connecting sections is maintained at 725μm. In design 2, a linear taper from 50Ω to 105Ω is used. For the two designs presented herein, k=1.15 and k=1.52 for design 1 and design 2 respectively. These values of k were chosen such that the impedance at the mid-point is close to the optimal impedance value for silicon (=70Ω).

In order to derive the two port S-parameter for the unit cell $[S]_{UNIT}$, the S-matrix for the NTL ($[S]_{NTL}$) is required. One approach in solving for $[S]_{NTL}$ is based on a lossless TEM transmission line model. Using the transmission line parameters, equation (2.35), and adopting phasor notation for voltage and the current the modified Telegrapher's equation can be written as:

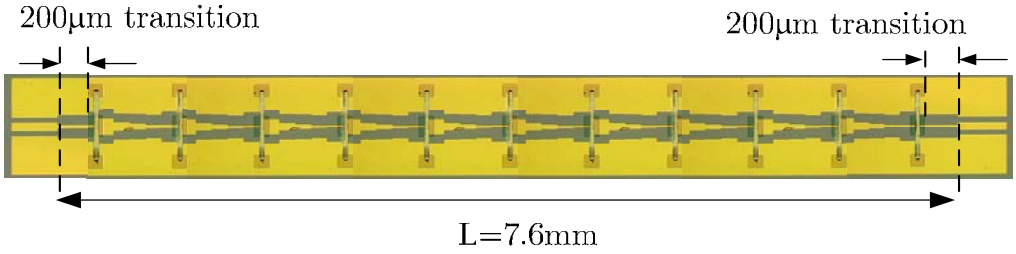
$$
\begin{aligned}
&\frac{\partial^2 V}{\partial x^2} - \frac{1}{Z_c(x)}\frac{\partial Z_c(x)}{\partial x}\frac{\partial V}{\partial x} + L_t(0)\,C_t(0)\,\omega^2\,V = 0 \\
&\frac{\partial^2 I}{\partial x^2} + \frac{1}{Z_c(x)}\frac{\partial Z_c(x)}{\partial x}\frac{\partial I}{\partial x} + L_t(0)\,C_t(0)\,\omega^2\,I = 0
\end{aligned}
\tag{2.36}
$$

The solution to (2.36) exists but requires complex algebraic operations with the involvement of Bessel functions. From (2.36), the [ABCD] parameters for the NTL ($[ABCD]_{NTL}$) can be solved. The overall [ABCD] parameter ($[ABCD]_{UNIT}$) is obtained by multiplying $[ABCD]_{NTL}$ and $[ABCD]_{MEM}$. Using matrix conversion, $[ABCD]_{UNIT}$ can be transformed to obtain S-parameters of the two port network. A simpler alternative to the matrix conversion approach is to use a commercial full wave electromagnetic (EM) solver. Agilent's planar EM solver which is based on Method of Moments (MoM) approach is used

for extracting the S-parameter of the unit cell. The S-parameters obtained from EM simulation for a unit cell are then cascaded in a circuit simulator (ADS) to predict the performance of the phase shifter.



(a)



(b)

Figure 2.14: (a) Schematic and fabricated unit cell of two NTL capacitively loaded phase shifter designs; (b) Photograph of the fabricated device (design 1), a 200µm long high impedance (Z_o=66Ω) line is used to transition from a 50Ω feed to the DMTL sections.

The NTL phase shifter was fabricated on high resistivity silicon. The fabrication procedure is illustrated in Appendix C. Measurements were performed from 5–40GHz using a Wiltron 360B vector network analyzer and 150µm GGB microwave probes. A Thru–Reflect–Line (TRL) calibration was performed using calibration standards fabricated on the wafer. A high voltage bias tee was used to supply voltage through the RF probe to avoid damaging the VNA test port.

Figure 2.15 (a) shows the comparison between measured and simulated $\Delta\phi$ for the two NTL designs (design 1 and design 2). The measured and simulated $\Delta\phi$ for the DMTL (or uniform Z_o =70Ω) on silicon is also shown for comparison. The agreement between measurement and simulation results is good (within 5%) through 40GHz. The worst-case S_{21} is typically observed when the line is loaded (high capacitance state) and found to be approximately -3dB for design 1 and -4dB for design 2 at 40GHz.

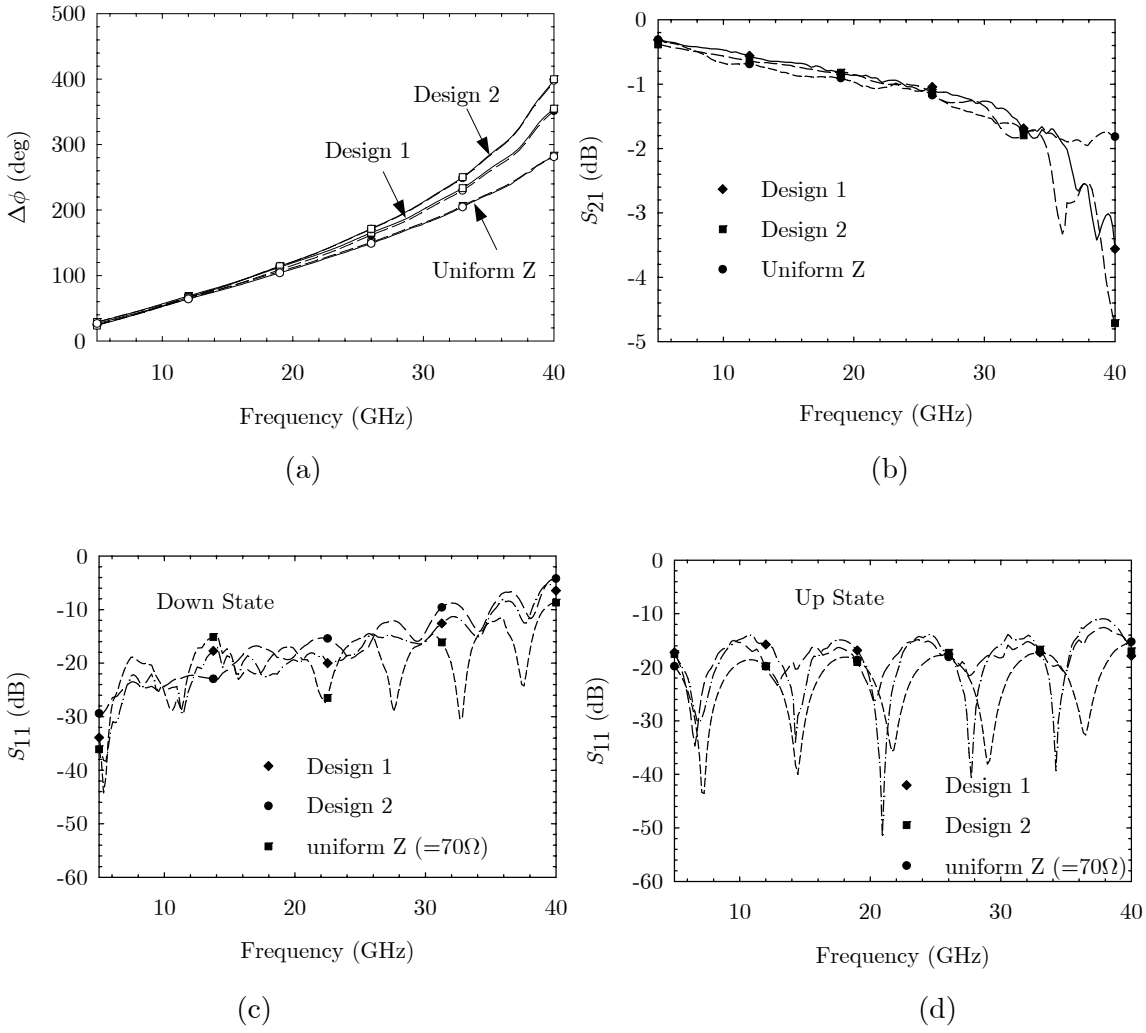


Figure 2.15: (a) Measured differential $\Delta\phi$ for the two NTL phase shifter (design 1, design 2 and DMTL with Z_o =70Ω) on 400μm thick high resistive silicon. The solid line for $\Delta\phi$ curve represents EM simulation data and the dashed lines represent measured data; (b) Worst-case S_{21} for the phase shifter; (c) Measured S_{11} in the down state; (d) Measured S_{11} in the up state.

The measured S_{11} plot in Figure 2.15 (c) and (d) indicate S_{11} < -10dB in both the states up to 35GHz for all the designs. Beyond this frequency, S_{11} for the NTL designs is higher than -10dB and it is also evident from the phase shift plot where the non-linearity in $\Delta\phi$ is more prominent (equation 2.21). Table 2.3 shows the comparison of the three designs at f_{max}=35GHz.

When compared with DMTL performance, design 1 and design 2 provide 15% and 21% improvement in $\Delta\phi$ at 35GHz, respectively. With respect to the uniform Z performance, the phase shift per dB figure of merit ($\Delta\phi$/dB) for design 1 is relatively unchanged, while there is 11% decrease in $\Delta\phi$/dB for design 2. This is because the NTL designs provide a non-constant rate of change in the loaded impedances. As a result, the Bragg frequency for the NTL designs is much lower than for the uniform Z design. This is evident from Figure 2.16 which shows the extracted effective characteristic impedance in both the states (Z_{eff}^{down} and Z_{eff}^{up}) for the NTL unit cell (Figure 2.14) and the uniform Z design under the loading conditions specified in Table 2.3. It is clear from this figure that the NTL designs show a non-linear increase in Z_{eff} for frequencies greater than 25GHz, while, Z_{eff} is almost constant through 40GHz for uniform Z unit cell. Substituting Z_{eff} for Z_o in equation (2.21), it is clear that for a given loading conditions, the phase shift increases as characteristic impedance Z_o increase. Therefore, more $\Delta\phi$ is seen for NTL designs when compared to uniform Z phase shifter.

Table 2.3: Comparison of the NTL phase shifter performance versus DMTL phase shifter with Z_o=70Ω.

f_{max} = 35GHz; C_r = 3.3 (=76fF/23fF)

	design 1	design 2	Uniform Z=70Ω
$\Delta\phi$ (deg)	274°	296°	233
Max S_{11}(dB)	-11.2	-10.3	-12.5
Worst-case S_{21}(dB)	-1.9	-2.3	-1.6
$\Delta\phi$/dB	144 °/dB	128 °/dB	145°/dB

Assuming the MEM bridge to be ideal, the conductor loss of the transmission line calculated using (2.12) with G_t =0 is approximately equal to 1.15dB at 35GHz (for the uniform Z phase shifter). When compared with the measured data in Table 2.3, it is seen

that the loss contributed by the static MIM capacitors is approximately 0.45dB. The increase in insertion loss for the NTL designs is due to the Bragg frequency effects as aforementioned.

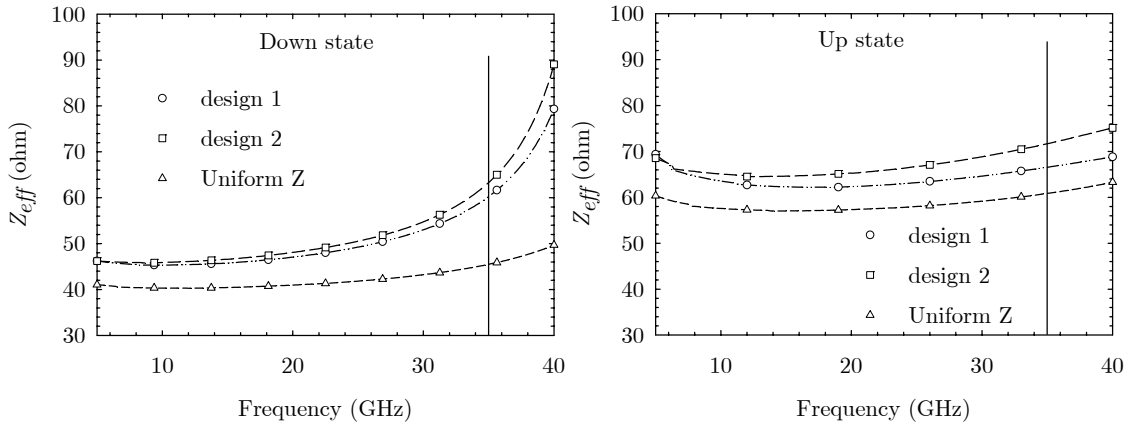


Figure 2.16: a) Extracted effective impedance (Z_{eff}^{down}) in the down state; b) extracted effective impedance in the up state (Z_{eff}^{up}) for the capacitively loaded NTL unit cell and uniform Z unit cell.

2.7 Chapter Summary

The theory of Distributed MEMS transmission line is presented and measured up to 40GHz. The DMTLs are fabricated using CPW lines on a 425μm thick silicon substrate with MEMS bridges periodically spaced across the line. An analytic model and a circuit model developed herein agrees well with the measured results. The circuit model consists of a physical length of transmission line for the CPW line and a capacitor-inductor series combination to model the MEMS bridge. The circuit model has also been used to quantify the accuracy of the measured data. Furthermore, for a reliable operation a digital type tuning is preferred and achieved by using a series-shunt capacitor arrangement. This capacitor design was used in the phase shifter constructed using non-linear transmission line. The measured results for the phase shifter show good agreement with the EM simulated results.

CHAPTER 3

Cascaded Slow-wave Phase Shifter Design and Results

This chapter presents the design and optimization of a TTD multi-bit MEMS phase shifter based on impedance-matched slow-wave CPW sections on a 500μm thick quartz substrate. The development of electronically variable phase shifters has been driven primarily by their use in phased array radars, although they are now used in a wide range of systems including communications and measurement instrumentation [27].

Most phase shifters currently used can be divided into either ferrite phase shifters or semiconductor device phase shifters. The ferrite based phase shifters typically work well from 3 GHz to 60 GHz with switching times on the order of a few microseconds to tens of microseconds [21, 22]. Most ferrite based phase shifters are not monolithic and require large switching energies but can handle kilowatts of RF power [9]. Recently, there has been research into the use of the ferroelectric material barium strontium titanate [$Ba_{1-x}Sr_x TiO_3$ (BSTO)] to produce planar phase shifters [12]. The designs demonstrate 44°/dB insertion loss at 14.3 GHz, however, they require very high bias voltages (250-400 V) [46]. In [61] authors have demonstrated a BSTO based phase shifter with 90°/dB with lower tuning voltage from 20-160V.

On the other hand, semiconductor device based phase shifters have been used up to 100 GHz with switching times well under 10μs [2, 7, 16, 27, 32, 39, 49, 52, 59]. These devices are either hybrid or monolithic with switching powers on the order of milliwatts. The hybrid devices (p-i-n or varactor diodes) can handle up to a kilowatt of RF power; however, the monolithic devices can only handle RF power on the order of milliwatts to one watt [27]. There are many different designs for the semiconductor device based phase shifters. Some of the more prominent designs are switched-line phase shifters [52], loaded-line phase shifters [22, 23], branch line or 3-dB coupler based phase shifters [39, 7, 59], and high-

pass/low-pass phase shifters [32]. The loaded-line and high-pass/low-pass type phase shifters are inherently limited to at most 67% bandwidth, where as the switched-line phase shifter is true-time delay with the bandwidth limited by the high-frequency operation of the switches. Typical figures of merit for the semiconductor device based phase shifters are 144°/dB at 1 GHz [32], 211°/dB at 12 GHz [16], 86°/dB from 16-18 GHz [7], 60°/dB at 60 GHz [39], and 41°/dB at 94 GHz [59].

Recently distributed true-time delay phase shifters were demonstrated in [31, 32]. These devices are very similar to the distributed MEMS transmission lines, but use varactor diodes rather than MEMS bridges for the variable capacitance. The phase shifters developed in [31] have shown good performance with 86°/dB insertion loss at 20 GHz, or 4.2 dB insertion loss for 360° phase shift. However, the millimeter wave performance of these devices is limited by the series resistance of the diodes.

For broad band and low loss operation, two commonly used true time delay (TTD) phase shifter designs are the switched network and the distributed MEMS transmission line (DMTL) [1]. The switched network consists of multiple delay networks that are typically switched using DC-contact series switches. The performance of the switched network is usually better than the DMTL up to 30GHz; however, for broad band operation beyond 30 GHz the DMTL type design is preferred [2].The DMTL design has been demonstrated from X-band to W-band [2-6]. Typical measured results for 2-bit X and Ka-band designs on quartz indicate 168°/dB at 13.6GHz and 128°/dB at 37.7GHz respectively [5]. Similar 2-bit and 4 bit designs demonstrate a phase shift of 130°/dB at V-band [2]. The W-band designs in [6] present a slightly lower phase shift (93-100°/dB) on a glass substrate. However, suggestions for improving the phase shift up to 200°/dB were also presented. In [2-6], metal-air-metal capacitors are used to minimize loss. Table 3.1 shows the measured DMTL performance of the current state of art DMTL phase shifter.

Table 3.1: Comparison of current state-of-the-art TTD phase shifter.

Substrate	Quartz (Barker/Rebeiz)	Glass (Nagra/York)	Quartz (Hayden/Rebeiz)
S_{11}	-13dB	-9.6dB	-12dB
S_{21}	-2dB	-1.7dB	-2.1dB
$\Delta\phi$ (°)	120	270	180
Length (L)	5.4mm	8.9mm	5.6mm
Spacing (s)	360um	780um	400um
Freq (GHz)	60	35	37.7

As seen in Chapter 2, the DMTL devices are often designed such that the S_{11} is less than -10dB in both phase states, up state (low capacitance state) and down-state (high capacitance state) positions. From equation (2.21), it is clear that for a given unloaded impedance Z_o, $\Delta\phi$ increases when the loaded impedances (in the high and low capacitance states) are symmetrically farther away from 50Ω. Using (2.21) and assuming no dispersion, the variation in $\Delta\phi$ versus maximum allowable S_{11} is shown in Figure 3.1(a) for three frequencies on a quartz substrate. It is seen from this figure that the amount of phase shift is proportional to the difference in the loaded and unloaded impedances. For example, if S_{11} less than -20dB is desired then the maximum $\Delta\phi$ is only 186°/cm at 50GHz and the loaded impedances should vary by a factor of 55/45.4Ω. Achieving this small variation in the impedance requires tight control over the value of the MEM capacitor. Assuming s=200μm and Z_o=95Ω, the capacitance values in the low and high impedance states is approximately $C_{max} / C_{min} = 29\text{fF} / 27\text{fF}$ from Figure 3.1 (b). Furthermore, from this figure it is seen that for the same operating condition, f_B decreases from 131/118GHz as the constraint on S_{11} decreases from -20 to -10dB, indicating that the usable range of the phase shifter is reduced by the same ratio.

This limitation in the capacitively-loaded design restricts the amount of achievable $\Delta\phi$ per unit length in light of impedance matching considerations. Therefore, a true time delay MEMS phase shifter topology that overcomes the limitations of the capacitor-only DMTL is presented herein. The topology uses cascaded, switchable slow-wave CPW sections to

achieve high return loss in both states, a large $\Delta\phi$ per unit length, and phase shift per dB that is better than previously reported performance.

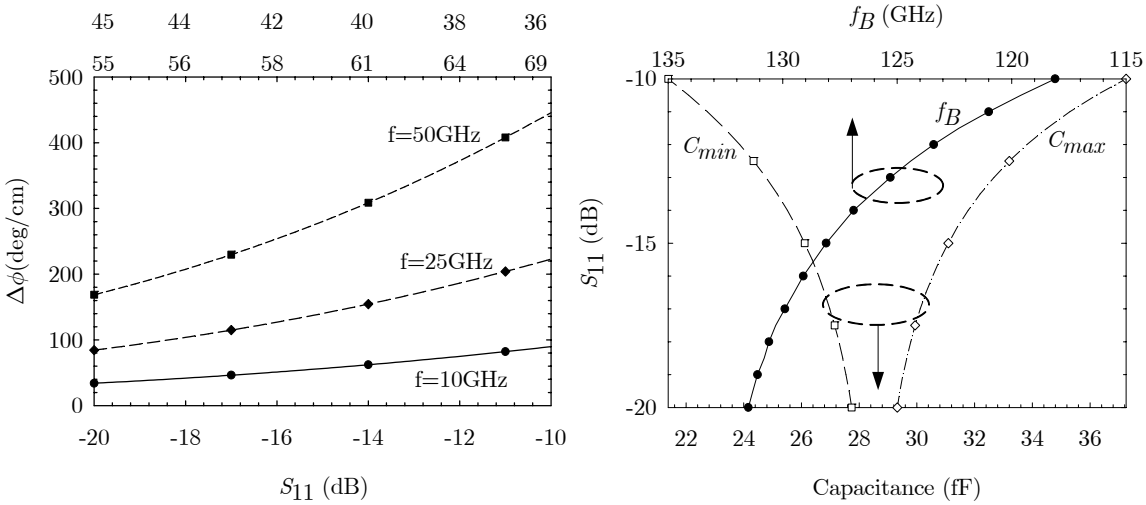


Figure 3.1: (a) Net phase shift ($\Delta\phi$) versus maximum allowable S_{11} (dB) assuming CPW on quartz. The impedance corresponding to S_{11} specifications is listed at the top of the plot; (b) S_{11} as a function of minimum and maximum capacitance values for the MEM bridge. The plots pertain to s =200μm and Z_o=95Ω.

3.1 Slow-wave Unit Cell Design and Fabrication

The MEM slow-wave unit-cell shown in Figure 3.2 is designed to provide small variations in the impedances around 50Ω, with a $\Delta\phi$ per unit length that is greater than a capacitively-loaded DMTL that has a worst-case S_{11} near -10 dB. The unit-cell is 460μm long and consists of two bridges on each ground plane and a shunt bridge that connects the ground planes and is suspended over the center conductor. In the normal state (Figure 3.2a), the bridges on each ground plane are actuated (solid lines) with electrostatic force applied through SiCr bias lines, while the shunt bridge is in the non-actuated state (dashed lines). In this normal state the signal travels directly from the input to the output. In the slow-wave state (Figure 3.2b), the bridges on the ground plane are not-actuated while the shunt bridge is actuated to contact the center conductor. The signal thus travels the longer path through the slot in the ground plane, thereby increasing the time delay. Furthermore, in the slow-wave state the increase in the per-unit length inductance is compensated by the

increase in the per-unit length capacitance (due to the wide center conductor) thereby maintaining the impedance close to 50Ω.

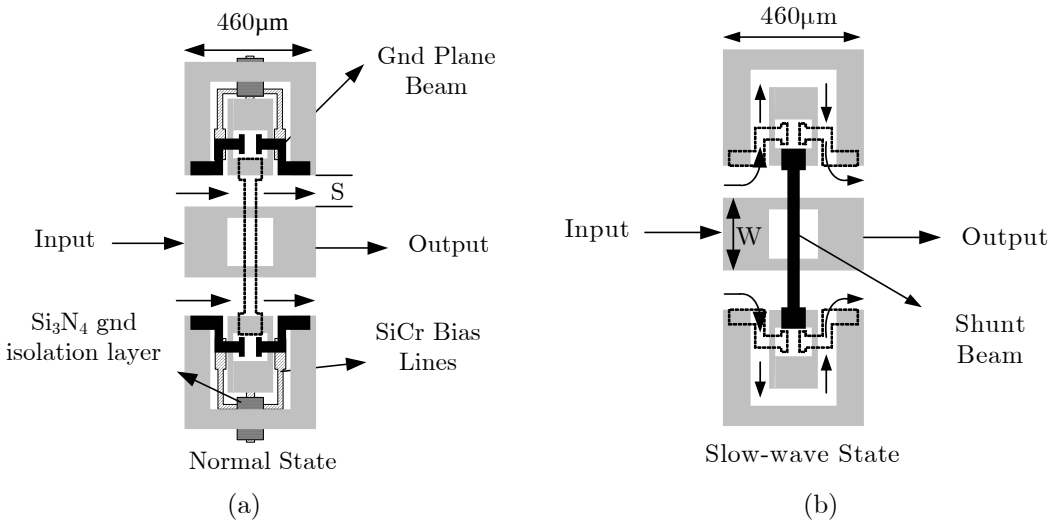


Figure 3.2: Schematic of the slow-wave structure - a) Normal state; b) Slow-wave state (the SiCr bias lines are not shown).

The slow-wave MEM devices used in this work are fabricated on a 500μm thick quartz (ε_r = 3.8, tanδ=0.0004). The outline of the fabrication process is shown in Figure 3.3. The SiCr bias lines are defined first using the liftoff technique by evaporating a 1000Å layer of SiCr using E-beam evaporation. The measured line resistivity is approximately 2000 Ω/sq. Next a 4000Å RF magnetron sputtered Si_xN_y layer is deposited and patterned to form the ground isolation layer. This layer is located where the SiCr bias lines enters the ground conductor (see Figure 3.3(c)). Next the CPW lines are defined by evaporating a Cr/Ag/Cr/Au to a thickness of 150/8000/150/1500Å using liftoff technique. Next the sacrificial layer (MICROCHEM PMMA)[1], is spin coated and etched in a reactive ion etcher (RIE) using a 1500Å Ti layer as the mask. The PMMA layer thickness can be varied from 1.5-2μm by varying the rotational speed of the spinner from 2500-1500 rpm. In this work, the thickness of PMMA is optimized to provide a height of 1.5-1.7μm (for low actuation voltage). The Ti layer is removed and a 100/2000Å Ti/Au seed layer is evaporated over the entire wafer and patterned with photoresist to define the width and the spacing of the MEM bridges. The bridges are then gold-electroplated to a thickness of 1μm, followed by removal of the top photoresist layer and seed layer. The sample is then annealed at 105° and 120° to flatten the bridges before removing the sacrificial PMMA

layer. The sacrificial PMMA layer is removed and critical point drying is used to release the MEMS structures.

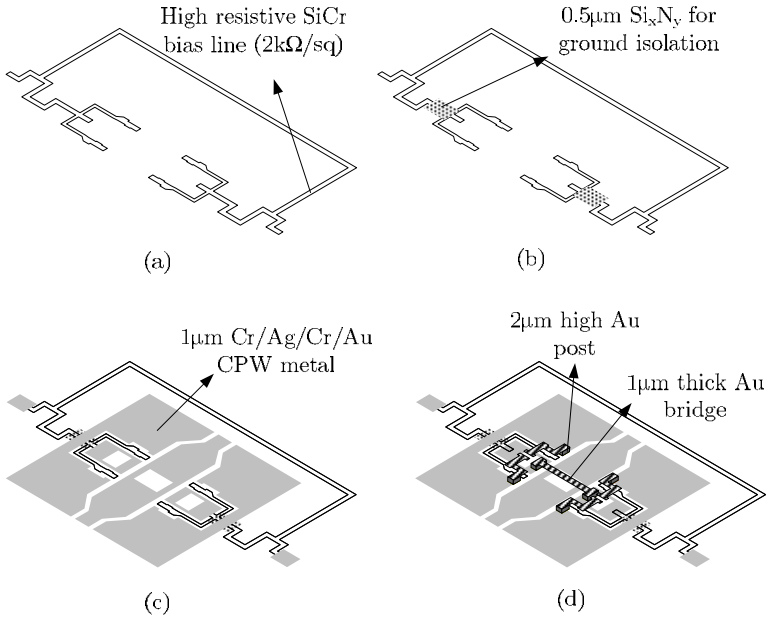


Figure 3.3: Details of the fabrication process for the MEM structures. The illustration shows a perspective view of a slow-wave unit cell.

3.2 Modeling of Slow-wave Unit Cell

The model for a slow-wave unit cell in both the states excluding the parasitics due to the bridge and the discontinuities is shown in Figure 3.4. In the normal state, the model comprises of transmission line of length s, with a capacitor to ground due to the shunt bridge (C_{bs}). In the slow-wave state, the model comprises of two shunt capacitors to ground due to the ground-plane bridges (C_{bg}) separated by the transmission line of length s_1 (which is equal to the total length through the slot).

Using the equations describing the DMTL, the impedance, propagation velocity, and the Bragg frequency for each states of the slow-wave unit cell is given by:

$$Z_n = \sqrt{\frac{sL_{tn}}{sC_{tn} + C_{bs}}} \qquad Z_s = \sqrt{\frac{s_1 L_{ts}}{s_1 C_{ts} + C_{bg}}} \tag{3.1}$$

$$v_{pn} = \frac{s}{\sqrt{sL_{tn}\left(sC_{tn} + C_{bs}\right)}} \qquad v_{ps} = \frac{s_1}{\sqrt{s_1 L_{ts}\left(s_1 C_{ts} + C_{bg}\right)}} \tag{3.2}$$

$$\omega_{Bn} = \frac{2}{\sqrt{sL_{tn}\left(sC_{tn} + C_{bs}\right)}} \qquad \omega_{Bs} = \frac{2}{\sqrt{s_1 L_{ts}\left(s_1 C_{ts} + C_{bg}\right)}} \tag{3.3}$$

where, L_{tn}, C_{tn} is the per unit length inductance and capacitance in the normal state. While, L_{ts}, C_{ts} are the per unit length inductance and capacitance in the slow-wave state. C_{bs} and s is the bridge capacitance and spacing between the shunt bridges. C_{bg} and s_1 is the bridge capacitance and spacing between the ground plane bridges.

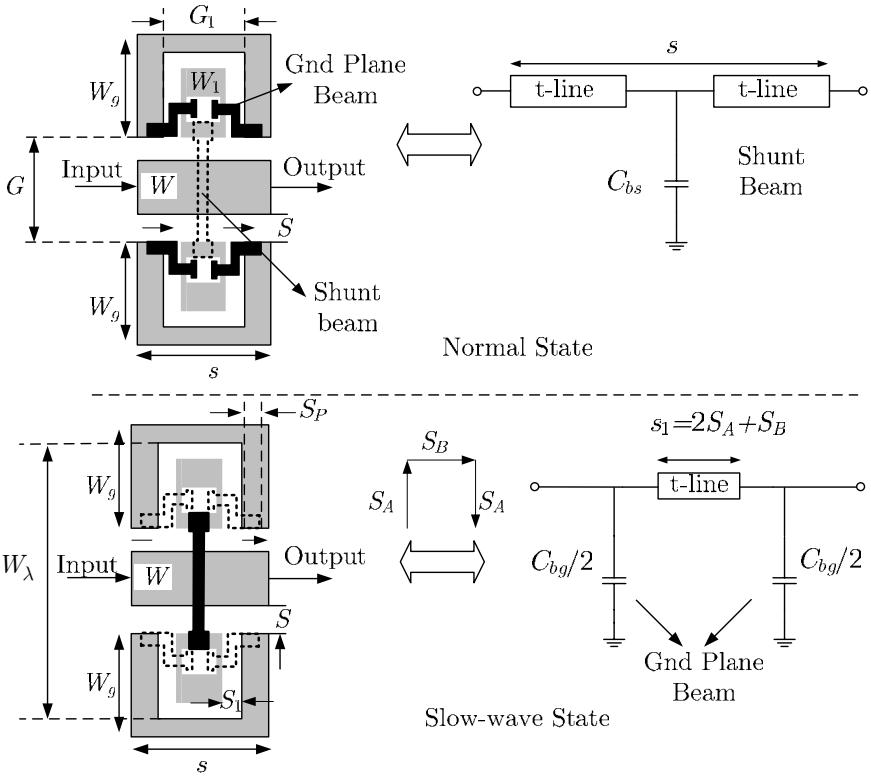


Figure 3.4: Ideal model for the slow-wave unit cell in both the states. This model does not take into account the parasitics due to the bridge and the discontinuities.

The per unit length capacitance and the inductance in both the states, has the form given by [42].

$$\begin{aligned} C_{tn} &= \sqrt{\varepsilon_{eff}} \,/\, cZ_{on} \qquad & C_{ts} &= \sqrt{\varepsilon_{eff}} \,/\, cZ_{os} \\ L_{tn} &= C_{tn} {Z_{on}}^2 & L_{ts} &= C_{ts} {Z_{os}}^2 \end{aligned} \tag{3.4}$$

in which ε_{eff} is the effective dielectric constant of the transmission line and c is the free space velocity. Since the slow-wave is constructed using a CPW line, Z_o and ε_{eff} can be related to the physical line parameters using conformal mapping [21]:

$$Z_o = \frac{30\pi}{\sqrt{\varepsilon eff}} \frac{K(k_1)}{K'(k_1)}$$

$$\varepsilon_{eff} = 1 + \frac{\varepsilon_r - 1}{2} \frac{K(k_2)}{K'(k_2)} \frac{K'(k_1)}{K(k_1)} \tag{3.5}$$

$$k_1 = \frac{W}{G}; k_2 = \frac{sinh\left(\frac{\pi W}{4h}\right)}{sinh\left(\frac{\pi G}{4h}\right)}$$

where, W is the width of the center conductor, G is the ground-to-ground spacing in the normal state, and h is the substrate thickness. The variables W and G are replaced with W_1 and G_1 for calculating the impedance in the slow-wave state.

The design of a slow-wave phase shifter requires the specification of the maximum frequency of operation (f_{max}) or Bragg frequency (f_B), dielectric constant (ε_r) and the normal state impedance (>50Ω). From these specifications, the maximum ground-to-ground spacing (W) in the slow-wave state is calculated using (3.6). A ground-to-ground spacing (W) of $\lambda/8$ is typical of CPW designs in order to limit radiation loss, however, as mentioned in Chapter 2, the periodic structures has negligible radiation loss. Therefore a larger W less than $\lambda/5$ is usable; in this work W is set to $\approx 65°$ which translates to $\lambda/$ (5.5) at f_{max}. The total length along the mid-point through the slot is equal to $2S_A + S_B$ (3.7), where S_A is the length of the slot in the north-south direction and S_B is the length of the slot in the east-west direction (Figure 3.4). Since the overall length of the unit cell cannot exceed "s" set by the Bragg frequency, the maximum value for $S_B = s$. However, this spacing is further reduced by a factor of $(2 \times S_P)$ required to accommodate the two ground plane pedestals. In this work, S_P is set to 80μm. The approximate signal path through the mid-point in the slot is calculated using (3.8). Therefore, the maximum value for G_1 is $2 \times S_P$.

$$W_\lambda = \frac{\lambda}{5.5} = \frac{c}{(5.5) f_{max} \sqrt{\varepsilon_{eff}}} \tag{3.6}$$

$$s_1 = 2S_A + S_B$$
$$= 2\left(\frac{W_\lambda}{2} - \frac{(W+S)}{2}\right) + S_B \tag{3.7}$$

$$s_1 = 2\left(\frac{W_\lambda}{2} - \frac{(W+S)}{2}\right) + \left(s - 2\times S_P\right) - \left(\frac{G_1 - W_1}{2}\right) \tag{3.8}$$

In equation (3.8), the separation (s) is dependent on simultaneous equations (3.1) and (3.3). The Bragg frequency, f_B, is selected as per guidelines provided in Chapter 2. Using (3.1) through (3.3), the separation between the shunt bridges and the bridge capacitance is given by:

$$s = \frac{c}{\pi f_B \sqrt{\varepsilon_{eff}}} \qquad\qquad C_{bs} = s\left[\frac{L_{tn}}{Z_n^{\,2}} - C_{tn}\right] \tag{3.9}$$

It is seen from (3.9) that s is inversely proportional to the Bragg frequency (f_B) and the effective dielectric constant of the substrate. For a given ground-to-ground spacing (G), and f_B=2.6f_{max}=130GHz, s=734μm on air, 474μm on quartz and 291μm on silicon substrate at f_{max}. Using (3.9), and for an impedance matched condition (Z_n=50Ω), Figure 3.5 (a) shows C_{bs} (fF) as a function of W (and assuming G=300μm) for three different substrates (ε_r=1, ε_r=3.8, ε_r=11.7). Figure 3.5 (b) shows C_{bs} versus W for two different values of G on a quartz substrate.

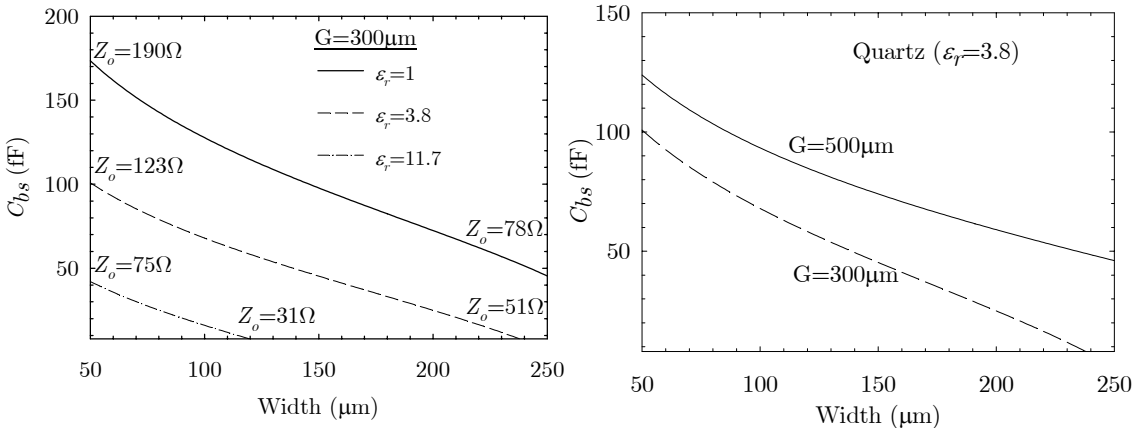


Figure 3.5: a) C_{bs} versus center conductor width, W (and G=300μm) for air, quartz, and silicon substrates; b) C_{bs} versus W for two ground-to-ground spacing on quartz substrate. f_B is set to 2.6f_{max}=130GHz.

The impedance matched condition is also applied to the slow-wave state and the ground plane bridge capacitance (C_{bg}) is given by (3.10):

$$C_{bg} = s_1 \left[\frac{L_{ts}}{Z_s^{\,2}} - C_{ts} \right] \tag{3.10}$$

Using (3.2), the phase constants in both the states and the net phase shift ($\Delta\phi$) is derived in (3.11) and (3.12) respectively:

$$\begin{aligned} \beta_n &= \frac{\omega}{v_{pn}} = \frac{360}{2\pi}\, s\, \omega \left(\sqrt{L_{tn} C_{tn} \left(1 + \frac{C_{bs}}{C_{tn}} \right)} \right) \qquad \text{deg/section} \\ \beta_s &= \frac{\omega}{v_{ps}} = \frac{360}{2\pi}\, s_1\, \omega \left(\sqrt{L_{ts} C_{ts} \left(1 + \frac{C_{bg}}{C_{ts}} \right)} \right) \qquad \text{deg/section} \end{aligned} \tag{3.11}$$

$$\begin{aligned} \Delta\phi &= \beta_n - \beta_s \\ &= \frac{360\,\omega}{2\pi} \left[s \left(\sqrt{L_{tn} C_{tn} \left(1 + \frac{C_{bs}}{C_{tn}} \right)} \right) - s_1 \left(\sqrt{L_{ts} C_{ts} \left(1 + \frac{C_{bg}}{C_{ts}} \right)} \right) \right] \qquad \text{deg/section} \end{aligned} \tag{3.12}$$

From (3.8), it is seen that maximum value of G_1 is related to s, and varies as $1/\sqrt{\varepsilon_{eff}}$ (Figure 3.6). It is seen from this figure that the maximum value for G_1 with f_B=2.6f_{ma} (130GHz) on silicon is equal to 200μm. Using this equation and (3.5)-(3.10), the phase shift per millimeter versus the conductor width (W_1) for the slow-wave unit cell is calculated on silicon, quartz, and air at 50GHz for the specifications listed in Table 3.2.

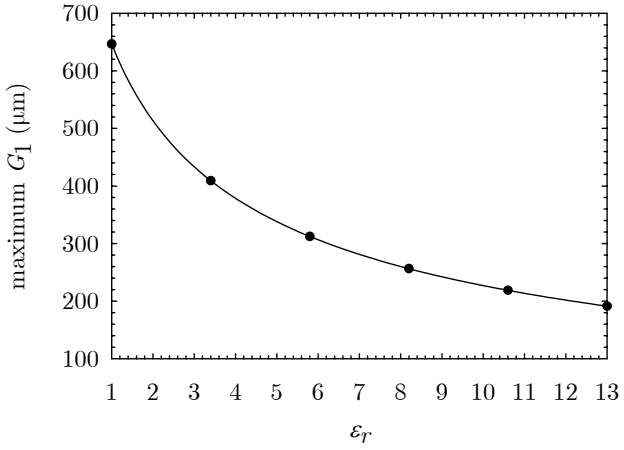


Figure 3.6: Maximum value of G_1 versus substrate dielectric constant assuming f_B =2.6f_{max}=130GHz.

In this calculation, two different total CPW widths G (300μm and 500μm) are plotted (Figure 3.7) keeping the spacing G_1=300μm and the width W=100μm constant. As can be seen from Figure 3.7, for a given G, the phase shift is much larger for a narrow center conductor width (high impedance). This is due to larger loading capacitance C_{bg}/s_1 needed to load the line to 50Ω and therefore the bridge capacitance has a larger effect on the phase velocity. It is observed for the same substrate, at two different impedance values with different total CPW widths G results in same phase shift. For instance, on quartz, for W/G_1=100/300μm, W_1/G=109/300μm (91Ω), $\Delta\phi$ = 150°/mm. The same $\Delta\phi$ is obtained for W_1/G=84/500μm (123Ω). Furthermore, for a given W_1, W and G_1, it is seen that $\Delta\phi$ increases as G decreases. For example, for the same W/G_1 ratio on quartz and with W=100μm, $\Delta\phi$/mm increases from -124° (G=500μm) to -160° (G=300μm). Therefore, reducing the spacing G results in larger $\Delta\phi$. However, one of the limitations in reducing the spacing G is that the pull-in voltage (V_p) required to actuate the shunt bridge increases as G decreases. For a 1μm thick Au platted bridge suspended 2μm above the CPW line with residual stress σ=30Mpa, ν=0.42, width=100μm, and a Young's modulus E=90GPa; V_p=20V for a 300μm long bridge while, V_p= 33V for 200μm long bridge. Therefore, for reasonable pull-in voltages V_p ($\leq$ 30V), the total CPW width G is designed to be $\geq$ 300μm.

Figure 3.8 shows $\Delta\phi$/mm versus the conductor width (W) for the slow-wave unit cell on silicon, quartz, and air at 50GHz for the specifications listed in Table 3.2. In this calculation, two different total CPW widths G (300μm and 500μm) are plotted keeping the spacing G_1=300μm and the width W_1=100μm constant. As can be seen from Figure 3.8, for a given G, the phase shift is much larger for a wide center conductor width (low impedance). This is due to smaller loading capacitance C_{bs}/s needed to load the line to 50Ω and the bridge capacitance has smaller effect on the phase velocity in the normal state (β_n). Therefore, the difference in phase constants between the two states increases (see (3.12)). Furthermore, for a given W_1, W and G_1, it is seen that $\Delta\phi$ increases as G decreases. For example, assuming W_1/G_1= 100/300μm on air, $\Delta\phi$/mm= -193° for W/G =100/300μm (147Ω) and $\Delta\phi$/mm=-160° for W/G =100/500μm (179Ω).

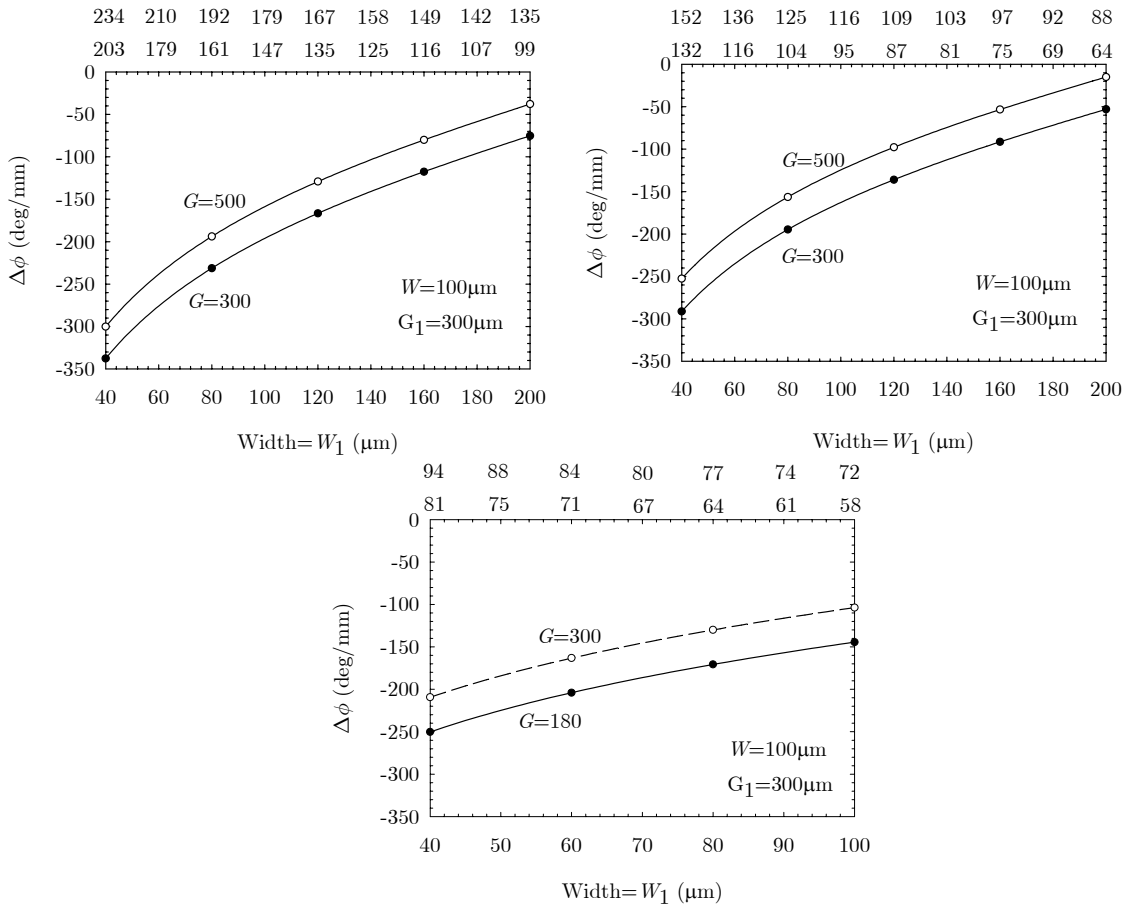


Figure 3.7: Calculated phase shift per mm versus the conductor width (W_1) at 50GHz for (a) Air, (b) Quartz, and (c) silicon with G_1=300μm and W=100μm. The maximum width W is equal to λ/5.5 in each case. The impedance corresponding to the center conductor width is given at the top of each plot.

From these figures it can be seen that phase shift ($\Delta\phi$/mm) increases as W decreases, while $\Delta\phi$ increases as W_1 decreases for a given spacing G and G_1. The following section presents optimum widths for W_1 and W such that the figure of merit $\Delta\phi$/dB is maximized.

Table 3.2: Specifications used in Figure 3.6.

$Z_n = Z_s$	50Ω
$f_B = 2.6 f_{max}$	130GHz

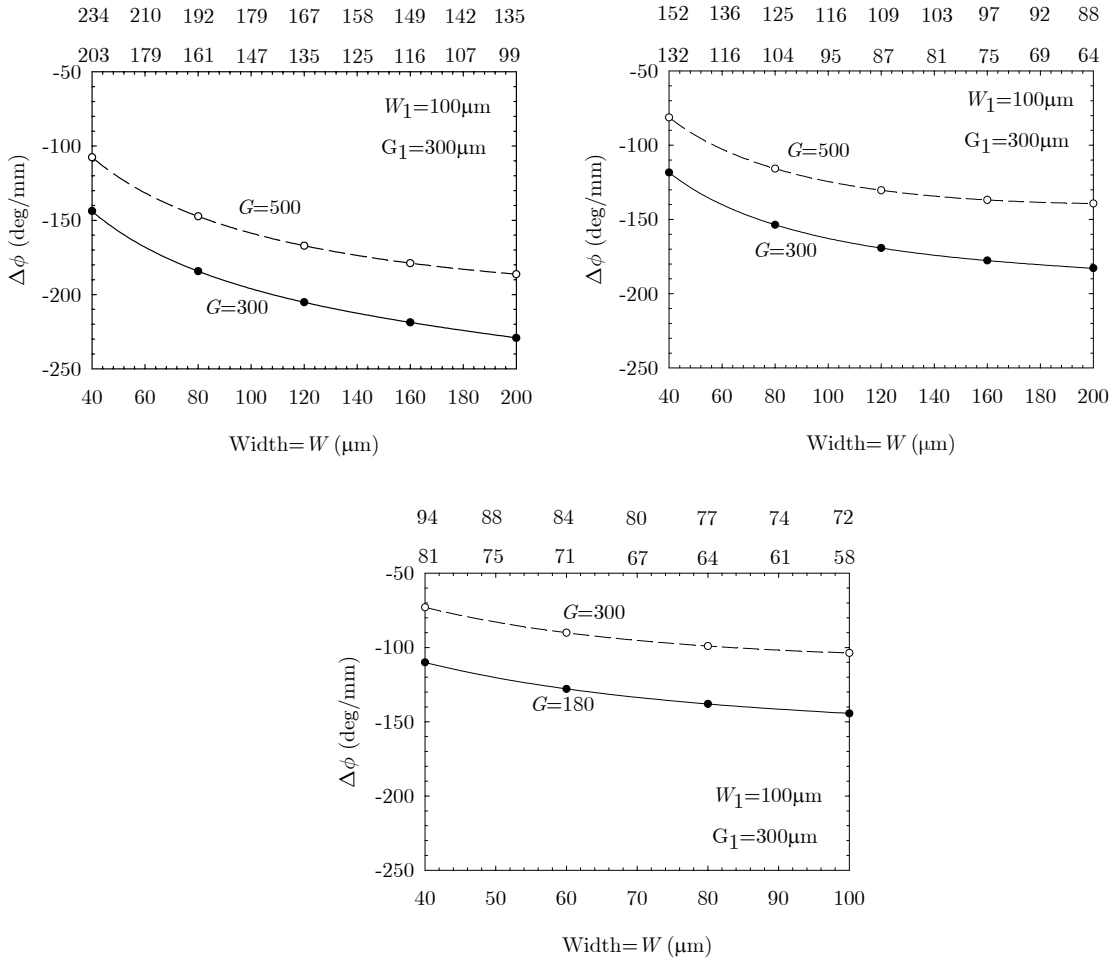


Figure 3.8: Calculated phase shift per mm versus the center conductor width at 50GHz for (a) Air, (b) Quartz, and (c) silicon with G_1=300μm. The maximum width W is equal to λ/5.5. The impedance corresponding to the center conductor width is given at the top of each plot. For example, for G=300μm on silicon, Z_o varies from 203Ω to 99Ω.

3.3 Optimization

One of the first reported optimization methods based on the work of Rodwell et al. was to minimize the loss in distributed non-linear CPW lines [20]. The distributed line analysis was significantly extended to optimize for the best phase shift by Nagra et al. [21]. Barker et al. [22, 23] applied a different method to a DMTL in which the MEM device was optimized to provide maximum amount of phase shift for the minimum amount of insertion loss. In this thesis, a method similar to [22] is applied to the slow-wave unit cell so that maximum $\Delta\phi$/dB is obtained. In order to carry out this optimization, analytic expressions for both the phase shift per unit length and the insertion loss per unit length are required. $\Delta\phi$ per

unit length is calculated using (3.12) and the conductor loss (α) per unit length is calculated using conformal mapping [21] and reproduced in (3.13).

$$\alpha(W,S) = \frac{8.686R_s\sqrt{\varepsilon_{eff}}}{4\eta_o SK(k)K\left(k'\right)\left(1-k^2\right)}\left[2\left(\pi+\ln\left(\frac{4\pi W(1-k)}{t(1+k)}\right)\right)\right] + \frac{8.686R_s\sqrt{\varepsilon_{eff}}}{4\eta_o SK(k)K\left(k'\right)\left(1-k^2\right)}\left(\frac{2S}{W}\left(\pi+\ln\left(\frac{4\pi W(1-k)}{t(1+k)}\right)\right)\right) \quad dB/length \tag{3.13}$$

where $K(k)$ is the complete elliptic integral of the first kind, $k = W/(W+2S)$, $k' = \sqrt{1-k^2}$, t is the metal thickness, R_s is the surface resistance given by $R_s = \left(\pi f\mu/\sigma\right)^{-1/2}$, and σ is the conductivity of the metal.

To verify the accuracy of (3.13), measured S_{21} data for uniform CPW line on 500μm thick quartz and on 425μm thick high resistive silicon (ρ > 2500Ω-cm) is compared with the loss obtained from (3.13). Figure 3.9 shows the measured and calculated loss versus frequency for a 300μm total width CPW line with a 100μm wide center conductor on quartz (Z_o = 95Ω) and on silicon (Z_o = 58Ω). The reference impedance for the measured data is set to the Z_o of the line.

It is seen from this figure that (3.13) underestimates the measured loss on quartz and on silicon substrate as evidenced by the correction factor required to match the measured data. The 1μm thick metal line is comprised of evaporated Cr/Au layer and the skin depth ($\delta = \sqrt{1/\pi f\mu\sigma}$) at 50GHz is approximately 2.8, while the 3μm thick lines are Au electroplated $\left(\sigma = 4.1\times10^{-7}\ S/m\right)$ [22]. According to (3.13) if the metal thickness is increased from 1μm to 3μm the loss would decrease by a factor of 1.12. However, this is not seen in measured data for quartz (Figure 3.9). This is because (3.13) assumes the metal thickness t to be greater than 4δ [27]. For the metallization used herein this condition is violated for freq > 30GHz.

It was experimentally found that the correction factor is not constant versus CPW pitch (Appendix B), therefore, (3.13) is used without any modification and therefore will predict

higher $\Delta\phi$/dB than measured data. However, for calculating the optimal CPW center conductor width (W and W_1) the trend is sufficient.

Apart from the conductor loss, the unit cell also has loss due to contact resistance of the bridge, conductor roughness, and leakage via the SiCr bias lines. These effects are difficult to calculate, and as will be seen in the next section, even with full wave EM simulation data a perfect match is not possible. Therefore, (3.13) is used to predict the trend of loss versus center conductor width.

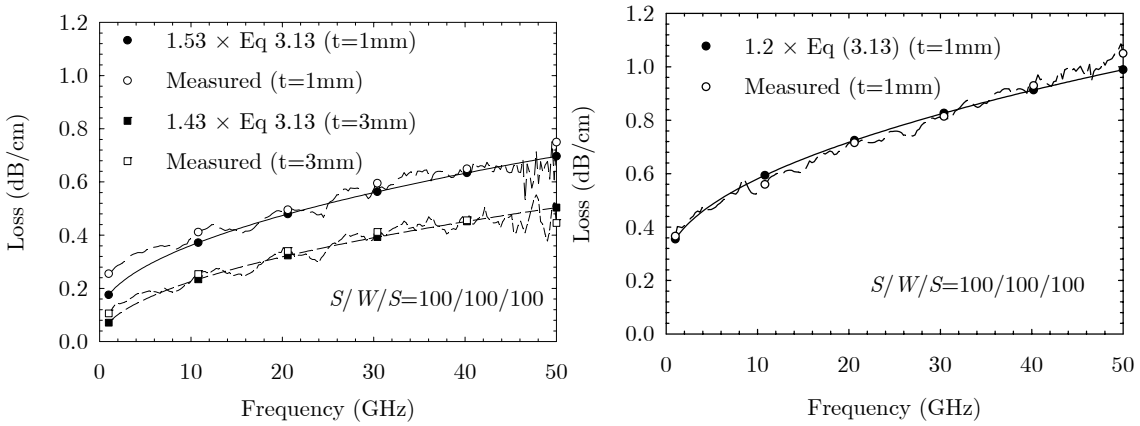


Figure 3.9: Measured and calculated uniform CPW line loss versus frequency for a 300μm total width for, a) quartz (Z_o=95Ω), b) silicon (58Ω). The reference impedance for the measurement is set to the Z_o of the line.

The bridge resistance is calculated using (3.14) and included in the analysis:

$$\alpha_{bs} = \frac{8.68 R_{bs} Z_n {C_{bs}}^2 \omega^2}{2}$$
$$\alpha_{bg} = \frac{8.68 R_{bg} Z_s 2{C_{bg}}^2 \omega^2}{2} \qquad (3.14)$$

Where, R_{bs} and R_{bg} are the shunt and ground plane bridge resistance. The loss due to the bridge resistance versus frequency is shown in Figure 3.10 for two values of bridge resistance of 0.1 and 0.2Ω. These values for R_{bs} and R_{bg} are typical of a MEM bridge with similar footprint [40]. The calculation is for a 300μm total width (G=G_1=300μm) with a 100μm width center conductor (W=W_1=100μm) (Z_o = 95Ω). Also shown in this figure is the variation of loaded line loss and the loss due to bridge resistance versus center

conductor width (assuming G=G_1=300μm) at 50GHz on quartz. Furthermore, this calculation is for the slow-wave state, since maximum loss is typically seen when compared with the normal state due to longer signal path. From this figure the loss due to bridge resistance (R_{bs}) at 50GHz is only 0.05dB or $<$ 10% of the CPW conductor loss. This percentage reduces for W=$W_1 > 150$μm.

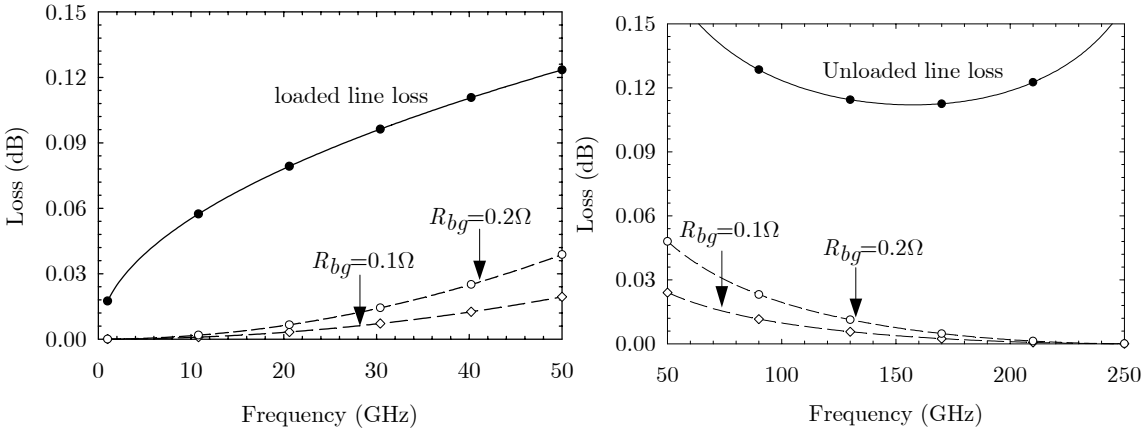


Figure 3.10: Loaded transmission line loss and loss due to bridge resistance versus a) frequency, b) W=W_1=100μm and G=G_1=300μm on quartz at 50GHz (f_B = 2.6f_{max} = 130GHz). The bridge is comprised of 1μm thick plated Au.

The optimal center conductor width (W and W_1) is found by dividing the phase shift per section by the loss per section to find the phase shift per dB loss for the unit cell. The total CPW width G is set to 300μm in light of pull-in voltage calculation. G_1 depends on f_B and ε_r and listed in Table 3.3.

Table 3.3: Maximum CPW width G_1 versus dielectric constant.

ε_r	G_1 (μm)
1	500
3.8	300
11.7	200

Figure 3.11 shows the calculation of $\Delta\phi$/dB at 50 GHz for air, quartz, and silicon substrates for f_B = 130GHz, G=300μm. It is seen from this figure that maximum phase shift per dB increases as the dielectric constant decreases and is 1219°/dB for air, 717°/dB for quartz, and 300°/dB for silicon. The maximum $\Delta\phi$/dB for the assumed CPW dimensions is

listed in Table 3.4. Furthermore, the 0° contour for $\Delta\phi$/dB is due to high C_{bs}/s required to load the line to 50Ω in the normal state offsets low C_{bg}/s_1 in the slow-wave state.

Although such high $\Delta\phi$/dB is theoretically possible, fabrication related limitations restrict achieving this value. For example, on quartz substrate maximum $\Delta\phi$/dB is obtained for $S/W/G/ = 25/250/25$ and $S_1/W_1/S_1$=125/50/125. For $S/W/G/ = 25/250/25$, C_{bs} is calculated to be 1.4fF (using 3.9). Achieving such small capacitance is not possible (due to fringing effects). Assuming a minimum achievable C_{bs}=8fF (for a 2μm gap), W is limited to approximately 220μm (Figure 3.5). For this value of W, maximum achievable $\Delta\phi$/dB is 640°/dB with W_1=50μm. Furthermore, the ground-plane bridge capacitance (C_{bg}) for this $\Delta\phi$/dB value is calculated to be 71fF (see equation 3.10). Assuming the parallel plate approximation and that the ground-plane bridge is also 2μm above the line, the required area is 1.58×10^4 μm^2. Designing this capacitance requires unrealistic bridge dimensions considering that the available bottom electrode width (W_1) for two bridges is only 50μm. Therefore, for practical design consideration, $W < 200$μm and $W_1 \geq 100$μm is more practical. These constraints further reduce the maximum achievable $\Delta\phi$/dB to $\sim$ 600°/dB on quartz. It is worth mentioning that the design equations do not use the correction factor for conductor loss and do not account for parasitics, therefore, measurable values will be considerably lower than the 600°/dB value as will be seen in the next section.

From a design standpoint, an air substrate can potentially provide more $\Delta\phi$/dB, however, air substrates are not practical for MEM circuits. Figure 3.12 shows C_{bg} values as a function of center conductor widths (W and W_1) at 50GHz for air, quartz, and silicon substrates (f_B = 130GHz, G=300μm). Figure 3.11 and Figure 3.12 and can be used as a guideline for designing a slow-wave unit cell.

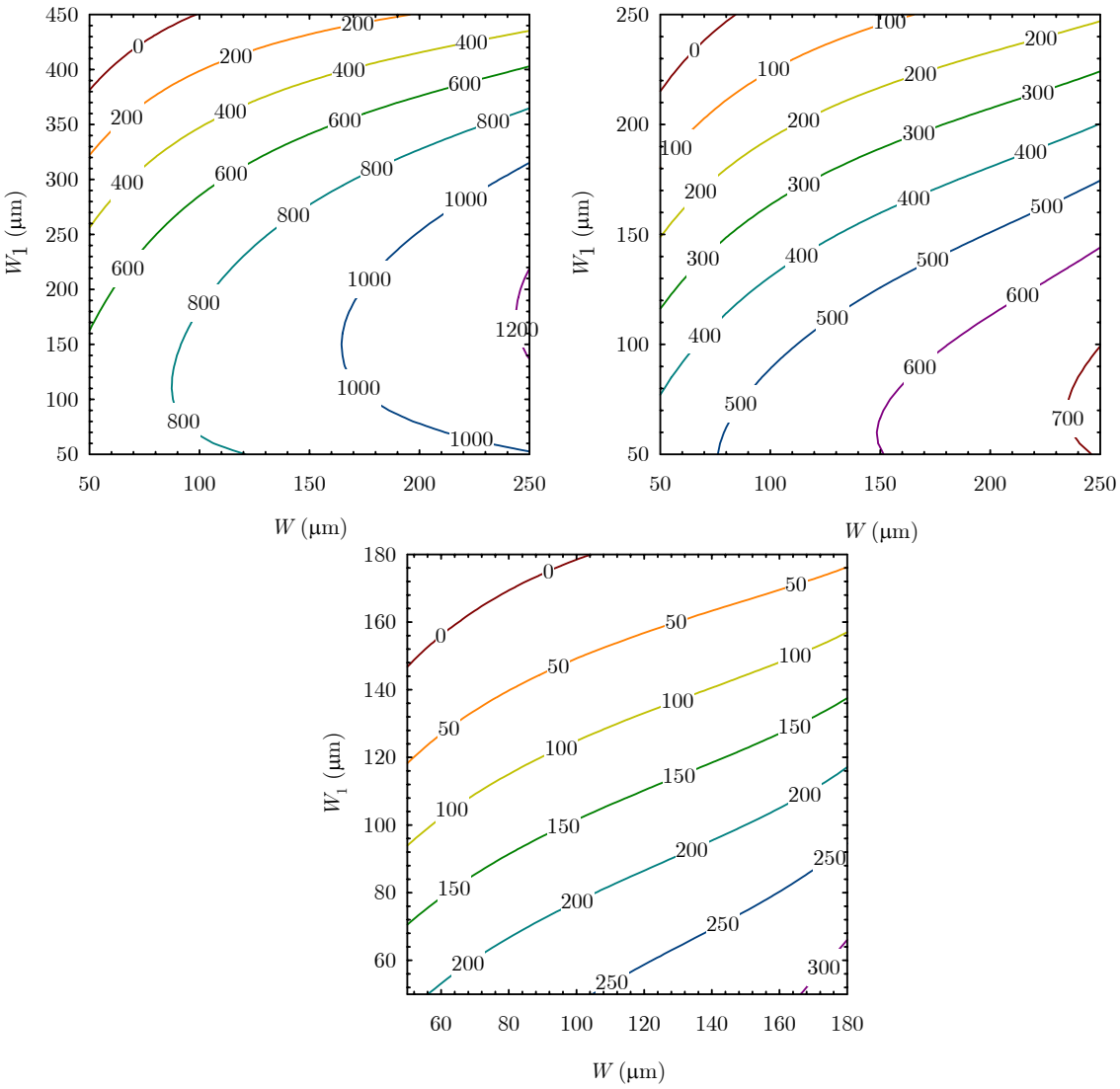


Figure 3.11: Calculated phase shift per dB (°/dB) at 50 GHz versus CPW center conductor width (W and W_1) for (a) air, (b) quartz, and (c) silicon substrates. In this calculation the total CPW width G=300μm, f_B=130GHz, and G_1 value in Table 3.3 is used.

Table 3.4: Calculated center conductor width (W and W_1) for maximum $\Delta\phi$/dB.

f_B=130GHz, $G=G_1$=300μm

ε_r	$\Delta\phi$ /dB	W (μm)	W_1 (μm)
1	1219	250	150-200
3.8	711	250	55-90
11.7	311	180	50-63

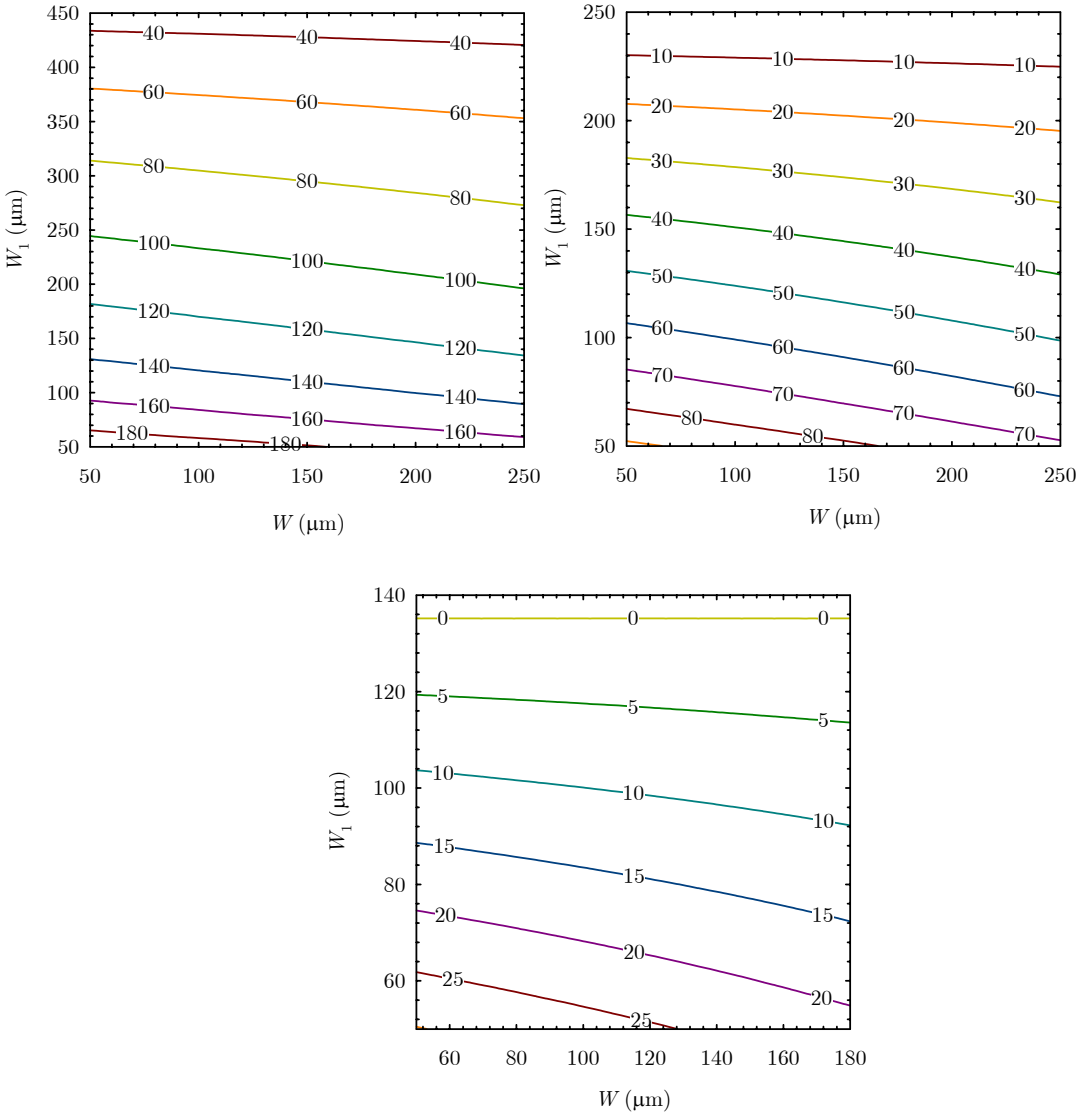


Figure 3.12: Calculated ground plane bridge capacitance ($2\times C_{bg}$) at 50 GHz versus CPW center conductor width (W and W_1) for (a) air, (b) quartz, and (c) silicon substrates. In this calculation the total CPW width G=300μm, f_B=130GHz, and G_1 value in Table 3.3 is used.

In order to verify the optimal center conductor width, a slow-wave unit cell was fabricated on a 500μm thick quartz substrate with $S/W/S$=100/100/100 and $S_1/W_1/S_1$=100/100/100 for the specifications listed in Table 3.2. Using the design equations (3.5)-(3.10), the bridge capacitances (C_{bs} and C_{bg}) and spacing (s and s_1) are calculated and listed in Table 3.5. The comparison between measured and calculated $\Delta\phi$ (using 3.10) is shown in Figure 3.13. From this figure it is clear that the agreement between the measured $\Delta\phi$ (=40.4°) data and calculated $\Delta\phi$ (35.5°) is within 12% through 50GHz. The discrepancy between the data sets is the calculation does not account for additional inductance due to current bending at the junction. An accurate value for f_B can be calculated by taking bridge inductance (L_b) into account, as presented in section 3.4. This calculation is not made here and could be one of the reasons for the differences. From the measured S_{11} data (Figure 3.13), it is seen that effective impedance in both the states (Z_n, Z_s) is close to 50Ω since S_{11} < -23dB. Furthermore, worst-case measured S_{21} is less than -0.13dB translating to ∼ 300°/dB. This value is lower than predicted value of 420°/dB, however, the contact resistance, conductor roughness, and signal leakage via SiCr bias lines contribute additional loss and reduce the $\Delta\phi$/dB.

It is proven via measurement that the design equation outlined in this section can serve as a design tool with limited accuracy. A semi-lumped model for the unit cell is presented in the next section to accurately model the measured S-parameters.

Table 3.5: Calculated parameters for the slow-wave unit cell.

	Calculated values
C_{bs}	62fF
C_{bg}	32fF
s	474μm
s_1	923μm

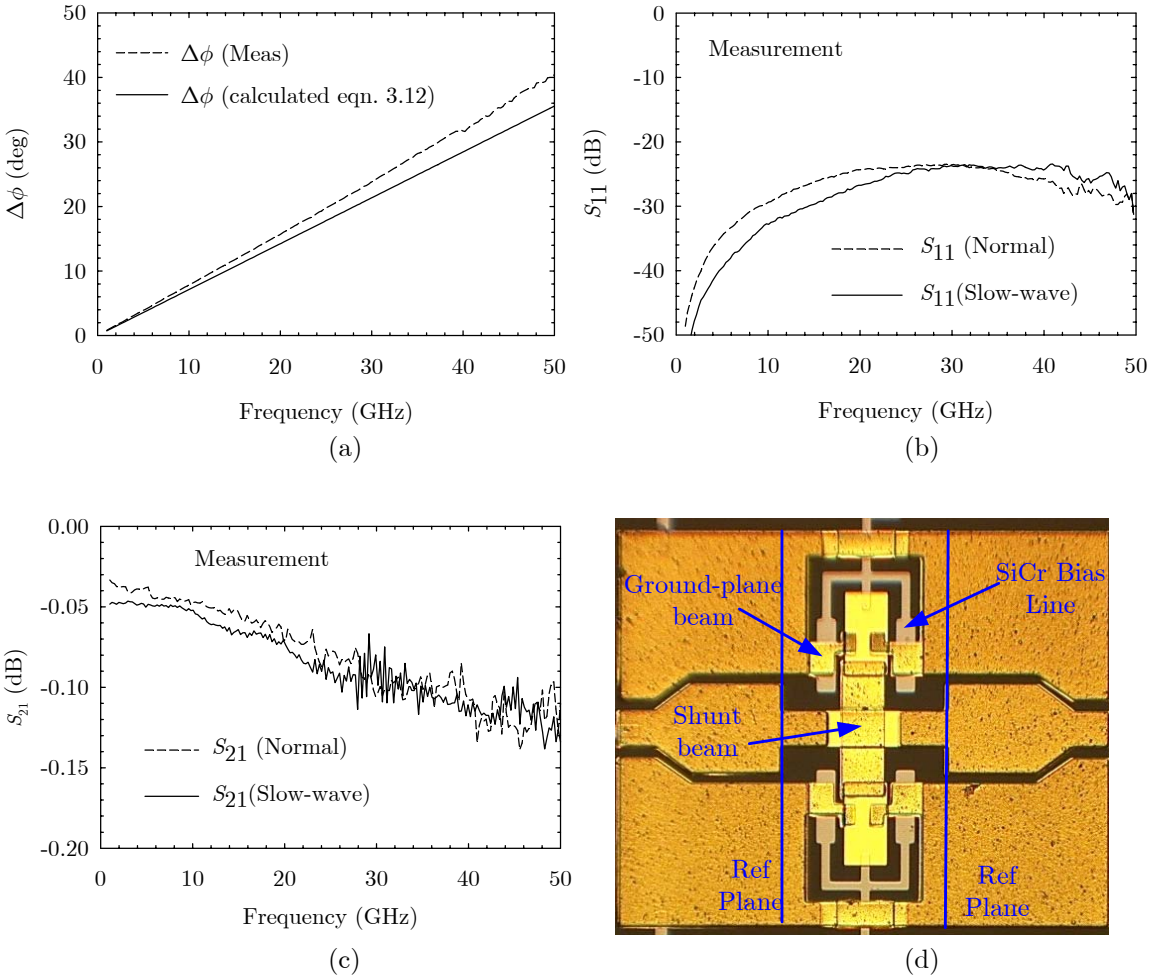


Figure 3.13: a) Comparison between measured and calculated $\Delta\phi$ (using 3.10) for a 460µm long unit cell, b) Measured S_{21} in both the states, c) Measured S_{11} in both the states, d) Photograph of the fabricated device.

3.4 Accurate Slow-wave Unit Cell Model

The model for a 460µm long slow wave unit cell in the normal state is shown in Figure 3.14 a. In the normal state (Figure 3.14 a), the model consists of uniform section of 55Ω transmission line (S/W/S=35/250/35µm) that is 210µm long on each side of the shunt bridge. The shunt bridge, which is 40µm wide and suspended 1.8-2µm above the center conductor provides a capacitance (C_{bs}) of approximately 8fF (using the parallel plate approximation). Using the per unit length value for line parameters (Capacitance=C_{tn}, Inductance=L_{tn}) and a spacing s=460µm for a 55Ω transmission line, the effective normal state impedance (Z_n) is found to be approximately 50.5Ω using (3.1) [22]. The effect of bridge inductance is excluded in (3.1), since the impedance due to L_{bs} is typically 50x (or

more) lower than the bridge capacitance (C_{bs}). The bridge inductance (L_b) and the bridge resistance (R_{bs}) are found via circuit optimization using measurement data. The resistance (R_p) and inductance (L_p) indicate the signal to ground path via ground plane bridges; their values are also found via optimization.

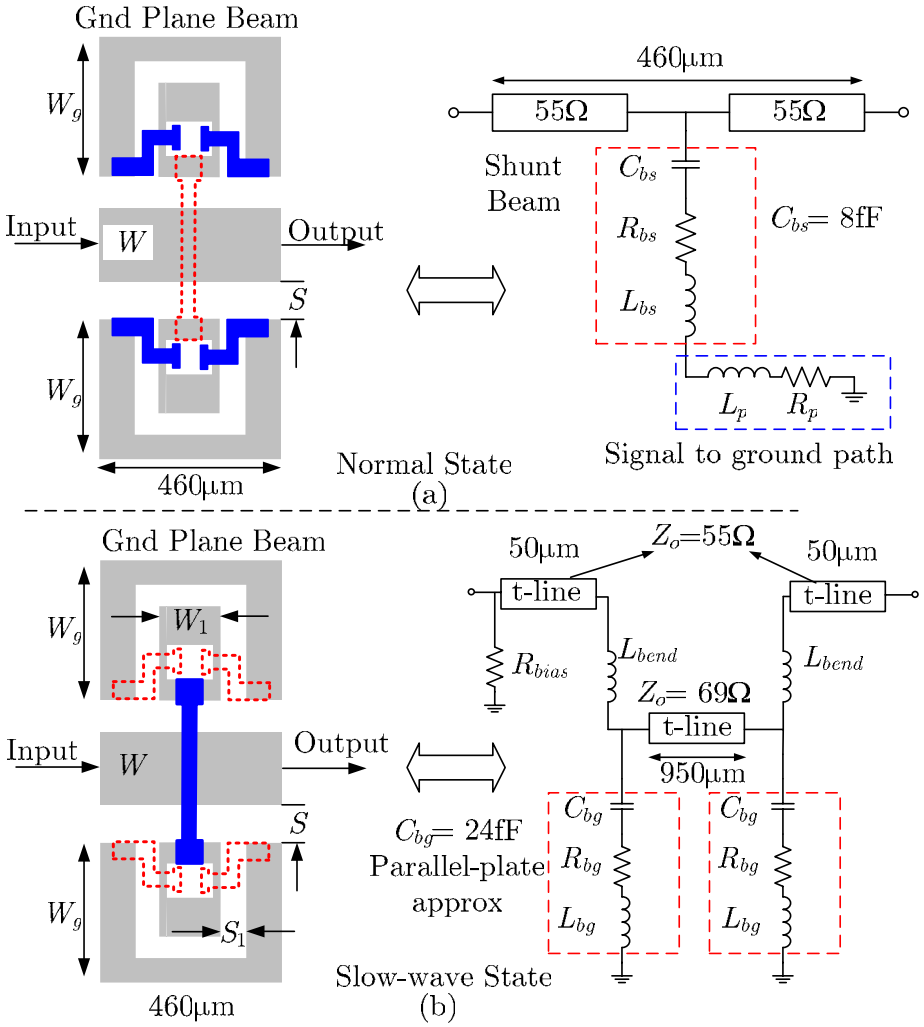


Figure 3.14: (a) Equivalent circuit model for the unit cell in the normal state, (b) Equivalent circuit model for the unit cell in the slow-wave state.

The model for the slow-wave state (Figure 3.14 b) also includes a 55Ω transmission line (50µm long) to model the feed section. Since the signal is routed through the long slot section, the current bending at the junction is modeled using an inductor L_{bend} and the value is found via circuit optimization. The total length of the CPW line that is routed through the slot is approximately 950µm ($=s_1$). The non-actuated ground-plane bridges provide a total capacitance (C_{bg}) of 2×24fF. A good impedance match in the slow-wave state is made

possible by designing the unloaded impedance of the slow-wave section to emulate a 69Ω uniform CPW line ($S_1/W_1/S_1$=60/160/60). The effective impedance (Z_s) for the slow-wave unit cell is calculated from (3.1) and found to be approximately 49.54Ω. The electrostatic voltage to pull the shunt bridge is provided via SiCr bias line at the input port which makes direct contact with the center conductor. The signal leakage (when shunt bridge is in DC-contact) through SiCr is modeled as R_{bias}, and the value for R_{bias} is typically obtained via circuit optimization. The maximum ground-to-ground spacing (W) is chosen to be less than λg/5 at 50GHz.

Measurements were performed from 1–50GHz using a Wiltron 360B vector network analyzer and 150μm pitch GGB microwave probes. A Thru–Reflect–Line (TRL) calibration was performed using calibration standards fabricated on the wafer. A high voltage bias tee was used to supply voltage through the RF probe to avoid damaging the VNA test ports. Typical actuation voltages are shown in Table 3.6.

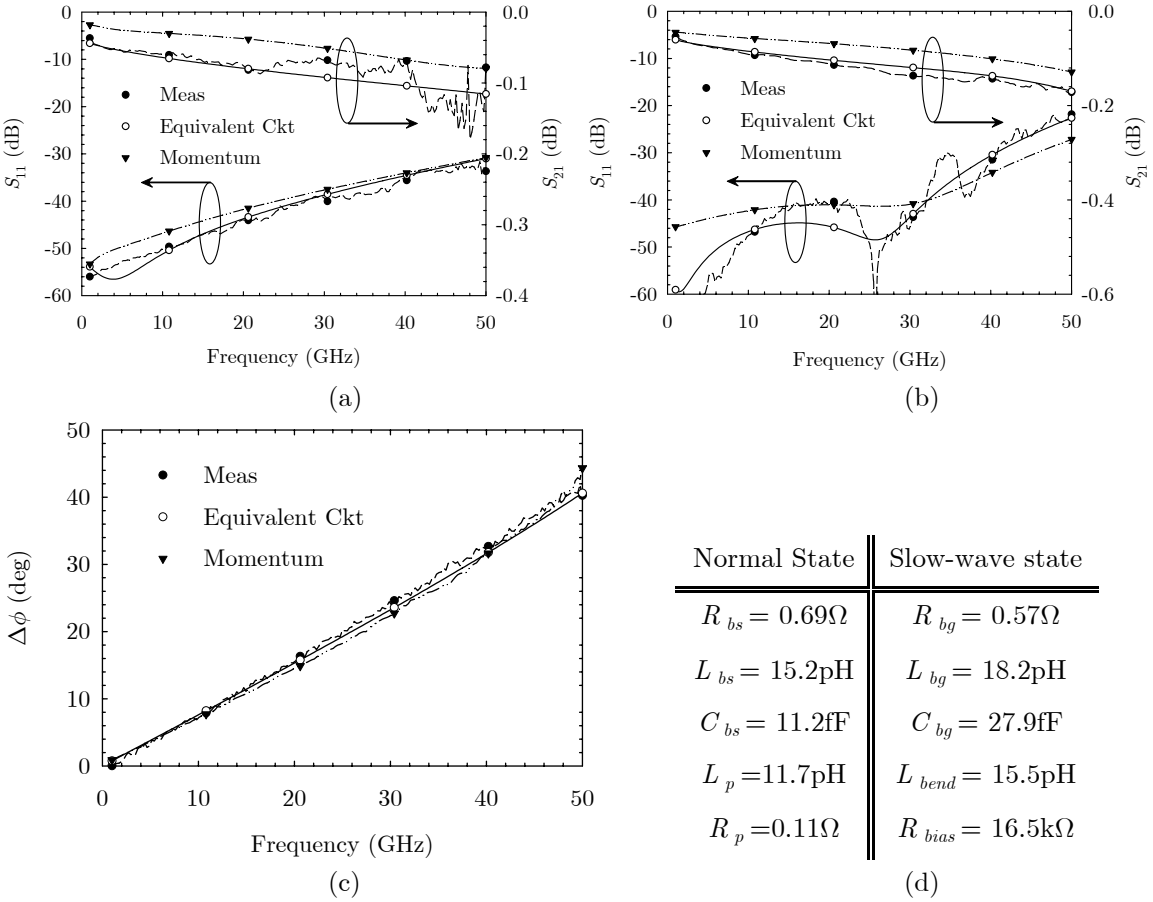
Table 3.6: Physical dimensions of CPW and MEM bridge

MEM bridge	Ground-plane Bridge	Shunt Bridge
Width	70	40
Length	285	440
V_p (volts)	35	28
CPW	Normal State	Slow-wave State
Center conductor	W= 250	W_1= 160
Slot	S = 35	S_1= 60

The unit cell model in Figure 3.14 was optimized to the measured data using ADS[1] circuit simulator. A full-wave electromagnetic (EM) simulation (Momentum) of the unit cell in both the states is performed to extract the parasitics and used as the starting value in the optimization routine. The comparison between equivalent circuit model, EM simulation and measured data (S_{11}, S_{21}, and $\Delta\phi$) for the unit cell in both the states is shown in Figure 3.15. From this figure it is clear that the agreement between the measured data and model

[1] ADS, Agilent Technol. Inc, Palo Alto, CA, 2003.

(equivalent circuit and Momentum) is good through 50GHz with a slight discrepancy in the slow-wave state. This discrepancy may be due to the coupling of signal (via the SiCr) underneath the ground plane and/or due to the conductor roughness.



Normal State	Slow-wave state
$R_{bs} = 0.69\Omega$	$R_{bg} = 0.57\Omega$
$L_{bs} = 15.2$pH	$L_{bg} = 18.2$pH
$C_{bs} = 11.2$fF	$C_{bg} = 27.9$fF
$L_{p} = 11.7$pH	$L_{bend} = 15.5$pH
$R_{p} = 0.11\Omega$	$R_{bias} = 16.5\text{k}\Omega$

(d)

Figure 3.15: Comparison between measurement data and model (equivalent circuit and full wave EM simulation), (a) S_{11} and S_{21} in the normal state, (b) S_{11} and S_{21} in the slow wave state, (c) Phase shift ($\Delta\phi$), (d) model parameters.

The Bragg frequency (f_B) is calculated using (3.15) [22]. For the unit cell as described herein, f_B is calculated for the parameters in the slow-wave state due to higher loading capacitance. Assuming a bridge inductance (L_{bg}) of 19pH (found from full wave EM simulation); f_B using (3.15) is calculated to be 126GHz.

$$
\begin{aligned}
f_B &= \frac{1}{2\pi}\sqrt{\frac{b-\sqrt{b^2-4ac}}{2a}} \\
a &= {s_1}^2 L_{ts} C_{ts} L_{bg} C_{bg} \\
b &= {s_1}^2 L_{ts} C_{ts} + s L_{ts} C_{bg} + 4 L_{bg} C_{bg} \\
c &= 4
\end{aligned}
\tag{3.15}
$$

It is seen that $\Delta\phi$ is approximately 44° at 50GHz and S_{11} is below -22dB from 1-50GHz. The worst-case S_{21} is -0.17dB for both states. The measured effective relative dielectric for the uniform CPW feed line was found to be 2.43. Using this value the effective length of the unit cell in the normal state is 580μm and in the slow-wave state it is approximately 1050μm, resulting in a slowing factor of 1.81 [7].

3.5 Phase Shifter Performance (1-bit and 4-bit version)

A 1-bit phase shifter is constructed by cascading 10 slow-wave unit cells (as shown in Figure 3.16). In this configuration, either the ground plane beams or shunt beams in all sections are actuated simultaneously. Typical height non-uniformities in the bridges is approximately 0.1-0.3μm. Therefore, to ensure actuation in all sections, the applied pull-in voltage (V_p) for both states is 5V higher than that of the unit cell (40V for normal state and 33V for slow-wave state).

Figure 3.16 shows a comparison between measured and modeled data for the phase shifter in both states. The simulated results were obtained by cascading the equivalent circuit model for the unit cell in the ADS circuit simulator. The agreement between the measured data and the model is good through 50GHz. The measured S_{11} is below -22dB for both states from 1-50GHz. Furthermore, the measured and simulated differential phase shift are within 2%, with a measured value of 407° at 50 GHz. The worst-case insertion loss is approximately 1.3dB. The figure-of-merit in degrees per decibels for the phase shifter is approximately 310°/dB at 50GHz (consistent with unit cell performance). The discrepancy between model and measurements in S_{11} (slow-wave state) may be attributed to the height non-uniformities in the MEMS bridges.

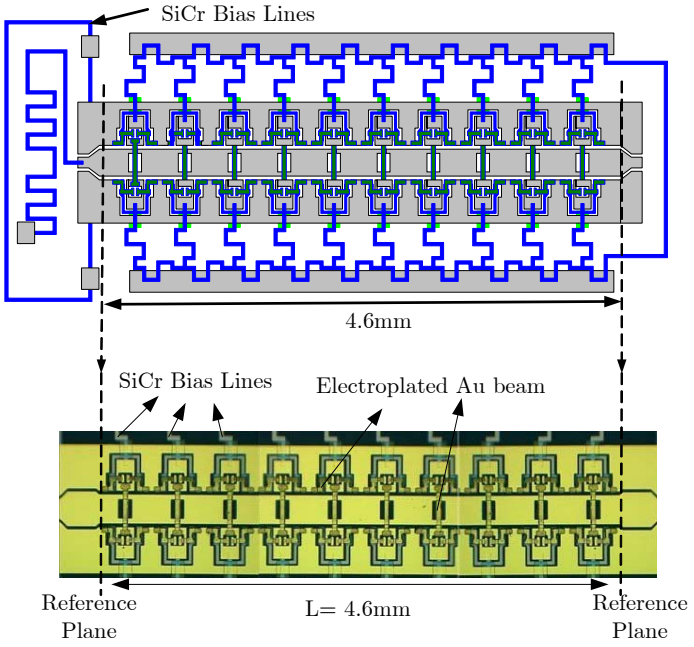
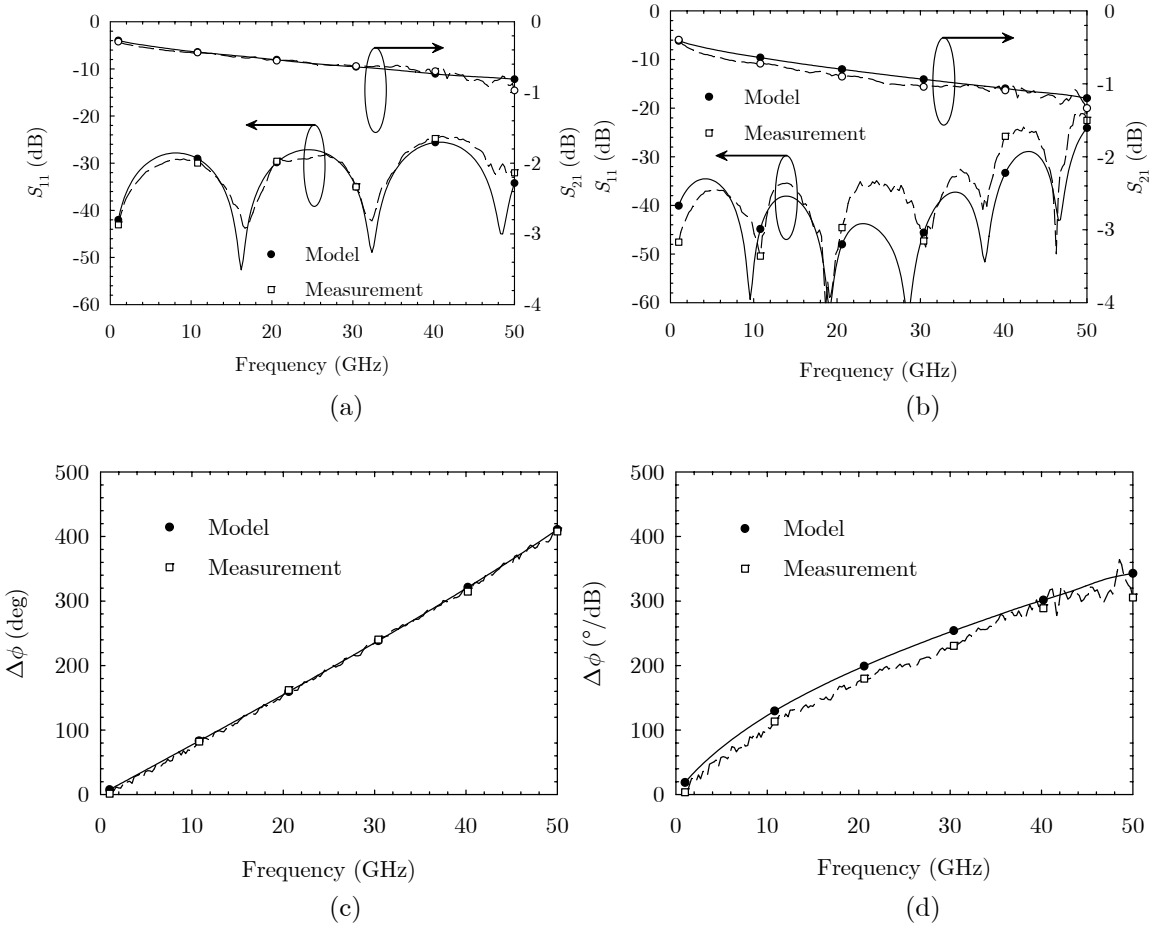


Figure 3.16: Schematic and photograph of the fabricated phase shifter. The phase shifter has 10 cascaded slow-wave unit-cells.

Figure 3.18 shows a comparison between the measured insertion loss for the phase shifter in both states and for a uniform 50Ω CPW line of equal length. Also plotted in this figure is the EM simulation for the phase shifter in both states. When comparing the measured phase shifter data and the uniform CPW line, it seen that the S_{21} for the phase shifter in the normal state is 0.9dB at 50 GHz, which is higher than the measured 50Ω line by 0.45dB. This increase in loss is due the contact resistance and small signal leakage via the SiCr bias lines. The signal leakage was verified by measuring a series resistor made of SiCr. It was found that the leakage through bias lines was less than -35dB through 50GHz.

Figure 3.19 shows the schematic and a photograph of the fabricated 4-bit phase shifter. The multi bit version is designed to provide $\Delta\phi$ of 45°, 90°, 180° and 225° at 30GHz. The 4-bit version also consists of 10 cascaded slow-wave unit cells (or 5 unit cell pair). Each unit cell pair provides a $\Delta\phi = 45°$ at 30GHz. For example, in the first bit ($\Delta\phi = 45°$), only one unit cell pair is operated in slow-wave state while the other pairs remain in the normal state. The second bit ($\Delta\phi = 90°$), consists of two unit cell pairs operated in the slow-wave state. The transition from the 1st bit to the 2nd bit is achieved by shorting the unit cell pair using

a wire-bond between the DC pads (as shown in Figure 3.19). Since the unit cell pairs are identical, there are five non-trivial phase states.



Normal State	Slow-wave state
$R_{bs} = 0.71\Omega$	$R_{bg} = 0.64\Omega$
$L_{bs} = 15.82$pH	$L_{bg} = 16.9$pH
$C_{bs} = 12.1$fF	$C_{bg} = 28.8$fF
$L_{p} = 11.1$pH	$L_{bend} = 14.9$pH
$R_{p} = 0.12\Omega$	$R_{bias} = 21.5$kΩ

(e)

Figure 3.17: Comparison between measurements and equivalent circuit model for the 1-bit phase shifter (a) S_{11} and S_{21} in the normal state, (b) S_{11} and S_{21} in the slow wave state, (c) Phase shift ($\Delta\phi$), (d) Phase shift per dB, (e) model parameters.

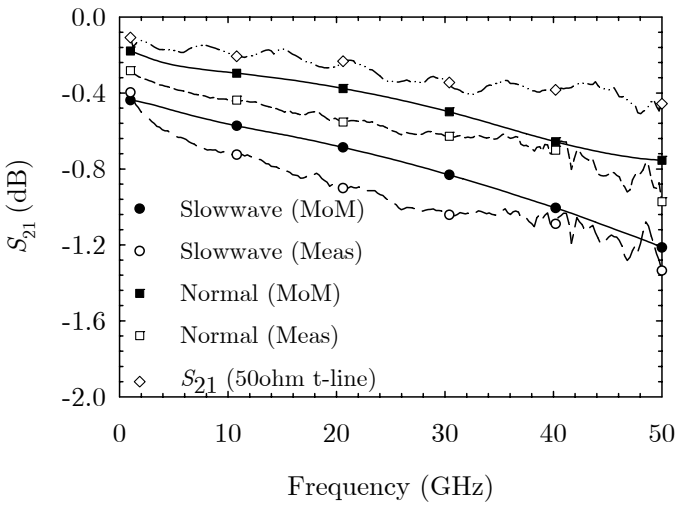


Figure 3.18: Measured S_{21} of the 1-bit phase shifter for both states and a 4.6mm long uniform 50Ω CPW line.

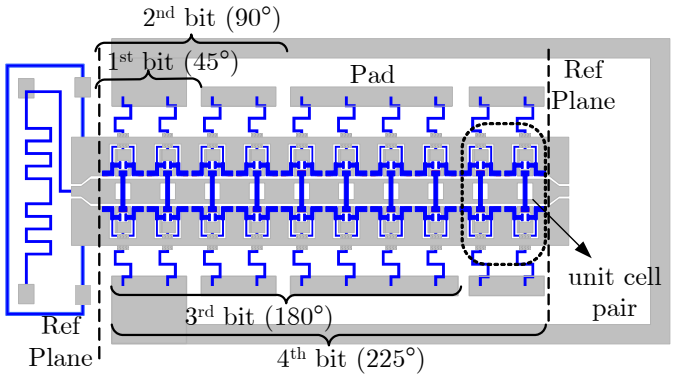


Figure 3.19: Schematic of the fabricated 4-bit phase shifter.

Figure 3.20 shows a comparison between measured multi bit phase shifter and the model for four states. It is seen from these plots that the agreement between measurements and model is good through 50GHz with S_{11} less than -21dB and worst-case S_{21} greater than -1.39dB. The comparison of $\Delta\phi$ between measured and modeled data is shown in Figure 3.21. The agreement between measured and modeled data is good through 50GHz with phase error less than 5.5° at 30GHz. The increase in S_{21} (~0.2dB) when compared with the 1-bit version is due to 15% decrease in bias resistance (R_{bias}) from 21.5kΩ to 18.3kΩ. Other model parameters were not altered in the circuit model.

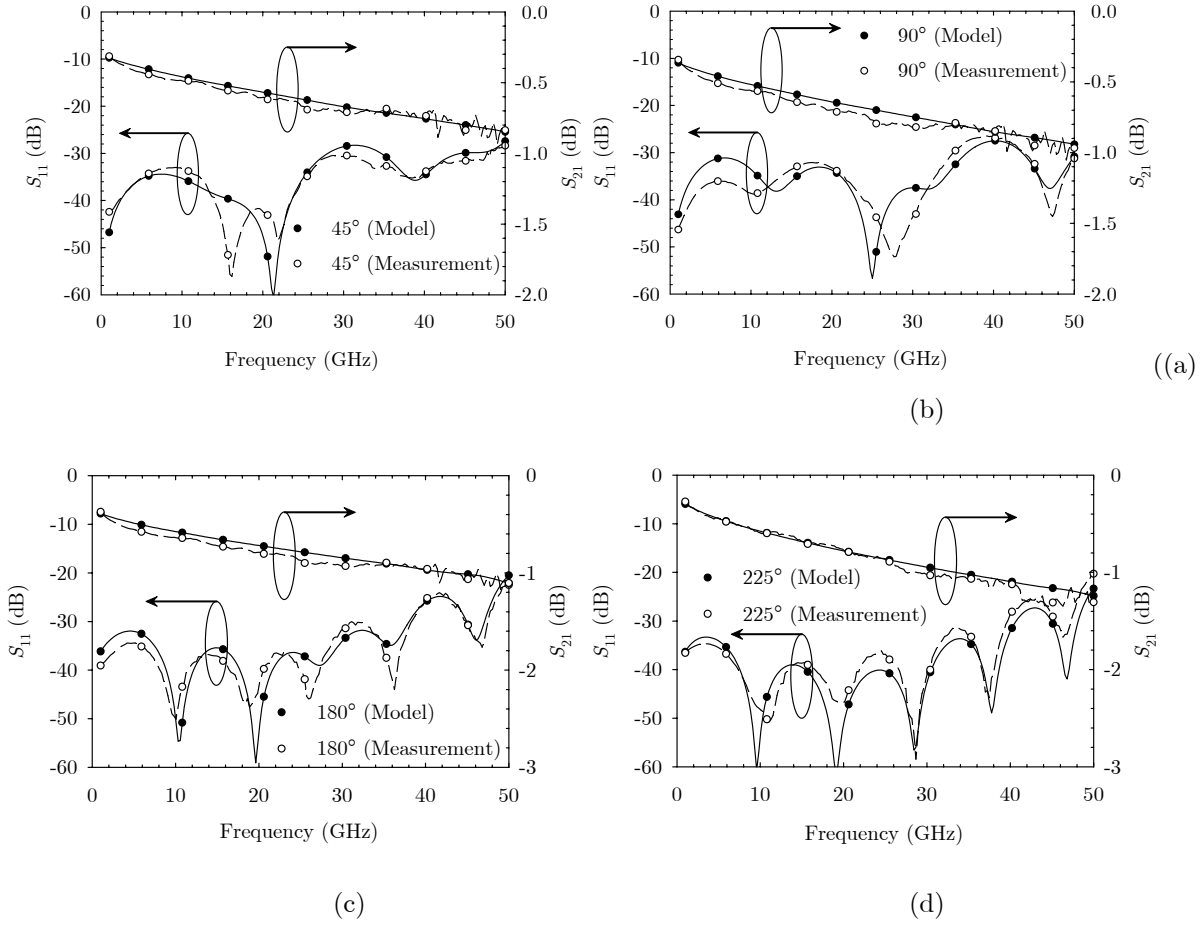


Figure 3.20: Comparison of S_{11} (dB) and S_{21} (dB) between measured data and equivalent circuit model; (a) 1st bit (45°); (b) 2nd bit (90°); 3rd bit (180°); 4th bit (225°).

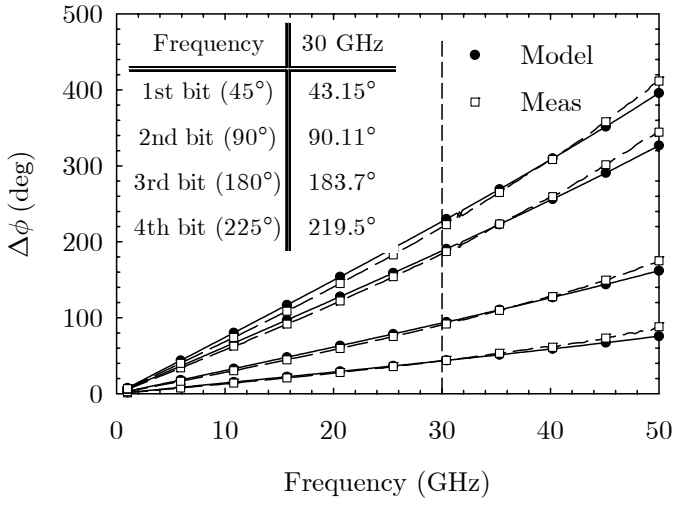


Figure 3.21: Comparison of $\Delta\phi$ between measured and modeled data for the multi bit phase shifter.

3.6 2nd Generation 1-bit Low Loss Phase Shifter Performance

The insertion loss of the phase shifter presented in section 3.4 is improved by using 3μm thick plated Au CPW lines. Furthermore, the Si_xN_y layer, previously located where the bias lines enter the ground conductor, is avoided and biasing to the beams enters through the ground plane cuts. An air-bridge (located 2-2.5μm) over the bias lines is used to connect the cut ground planes. It was found via EM simulations that the ground-plane cuts with the air-bridge have negligible effect on the S_{11} and $\Delta\phi$ of the unit cell. The maximum S_{11} value in the slow-wave state typically increased by a factor of 5dB (or 14% at 50GHz) for the three designs. However, the S_{11} value remained below -20dB through 50GHz in both the cases. The absolute phase in the slow-wave state typically decreased by a factor of 4% (or 1°).

Two phase shifter designs (design 1 and design 2) were fabricated on a 500μm thick quartz substrate. The CPW dimensions for the two designs are listed in Table 3.7. From Table 3.4, the optimum width for W and W_1 assuming G_1=G=300μm indicate W=250μm and W_1=50μm. To a 1st order, this is true for a given substrate. Therefore, a large width for W and small width for W_1 will be an ideal choice for the 2nd generation design. One of the shortcomings of this approach is that the f_B is dependent on the per unit length capacitance and inductance. Using (3.15), f_B versus center conductor widths (W and W_1) is shown in Figure 3.22 (assuming G=300μm and G_1=320μm). The variation of C_{bg} versus width (W and W_1) is also shown herein for comparison purposes. It is seen from this figure that calculated f_B is dependent on C_{bg} (ground-plane bridge capacitance) and the C_{ts} (capacitance per unit length of the unloaded line). In this work, footprints providing f_B lower than 120GHz were not considered. However, more $\Delta\phi$ can be obtained if a lower f_B can be tolerated.

The outline of the fabrication is similar to Figure 3.3 except that Si_xN_y layer is eliminated. The SiCr bias lines are defined first using the liftoff technique by evaporating a 900Å layer of SiCr using E-beam evaporation. Next the CPW lines are defined by evaporating a Cr/Au layer to ~1μm using liftoff technique. A 1.8-2μm thick PMMA sacrificial layer is spin coated and etched (2000Å Ti is used as masking layer) in a RIE chamber exposing the

CPW lines and the pedestals where the ground cuts need to be connected. The Ti layer is removed and a 100/1500Å Ti/Au seed layer is evaporated over the entire wafer and patterned with photoresist. The sample is Au electroplated to 1.8µm thick (total CPW metal is ∼2.8µm thick), followed by removal of the top photoresist and the seed layer. Another 2000Å Ti layer is deposited as a masking layer and the PMMA is etched where the pedestals for MEM bridges are located. The masking layer is then removed and an 80Å/2000Å Ti/Au seed layer is evaporated over the entire wafer. The bridges are then gold-electroplated to a thickness of 1µm, followed by removal of the top photoresist layer, seed layer. The sample is released after the two-step anneal. The photograph of the fabricated device is shown in Figure 3.23.

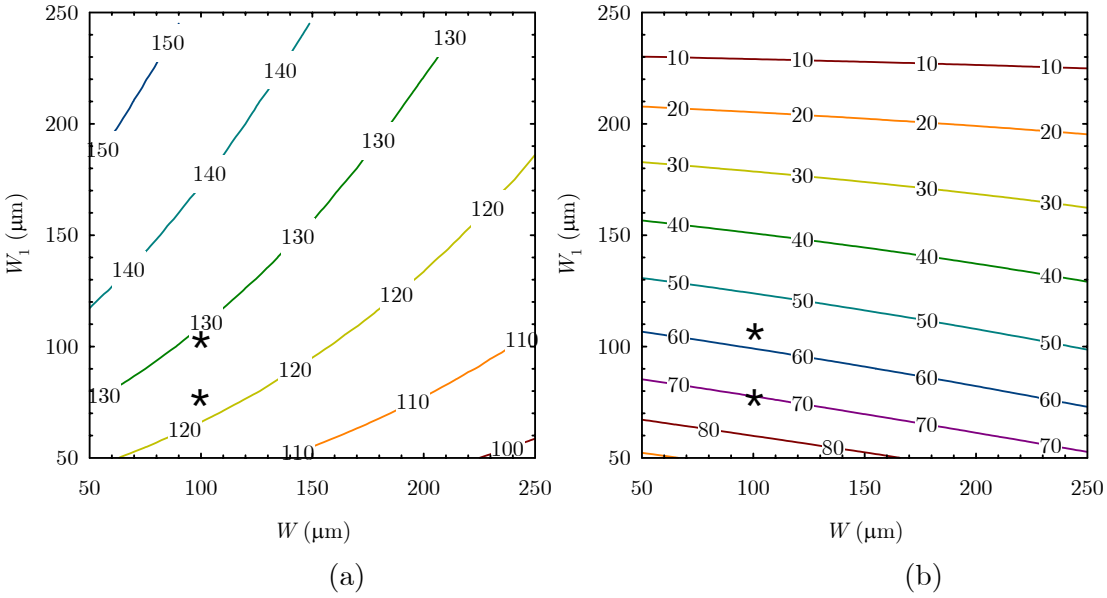


Figure 3.22: Calculated parameters for the slow-wave unit cell on quartz with G=300µm and G_1=320µm, a) f_B using (3.15), b) $2\times C_{bg}$. The two designs are marked in the figure.

The unit cell model in Figure 3.14 was optimized to the measured data (design 1 and design 2) using ADS. A full-wave EM simulation of the unit cell in both the states is performed to extract the parasitics and used as the starting value in the optimization routine. The simulated results for the 10-section phase shifter were obtained by cascading the equivalent circuit model for the unit cell in the ADS circuit simulator. The comparison between equivalent circuit model and measured data (S_{11}, S_{21}, and $\Delta\phi$) for design 1 and design 2 in both the states is shown in Figure 3.24.

Table 3.7: CPW and bridge dimensions for design 1 and design 2.

	CPW		Bridge	
	Normal State	Slow-wave State	Shunt	Ground-plane
design 1	W= 100μm S = 100μm	W_1= 120μm S_1= 100μm	l = 380μm w = 120μm V_p=28V	l = 270μm w = 90μm V_p=32V
design 2	W= 100μm S = 100μm	W_1= 80μm S_1= 135μm	l = 440μm w = 40μm V_p=35V	l = 285μm w = 70μm V_p=28V

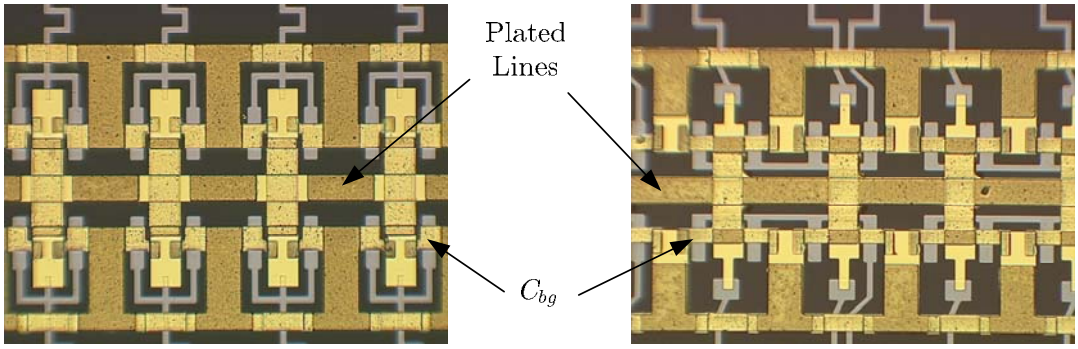


Figure 3.23: Photograph of the fabricated device, a) design 1, b) design 2.

The agreement between the measured data and the model for both the designs is good through 50GHz. The measured S_{11} is below -19dB for both states from 1-50GHz. Furthermore, the measured and simulated $\Delta\phi$ are within 1% for design1 and 3% for design 2, with a measured $\Delta\phi$ value of 391° for design 1 and 407° for design2 at 50 GHz. The worst-case insertion loss is approximately 1.1dB for design 1 and 1.15 for design 2. The figure-of-merit in degrees per decibels for the phase shifter is also shown herein and indicate a maximum $\Delta\phi$/dB of 345°/dB for design 1 and 354°/dB for design 2. When comparing with the 1st generation phase shifter results (see section 3.4) the current designs provide an improvement of 60% in $\Delta\phi$/dB for $f <$ 30GHz. Beyond 30GHz, there is only 10-15% improvement in $\Delta\phi$/dB.

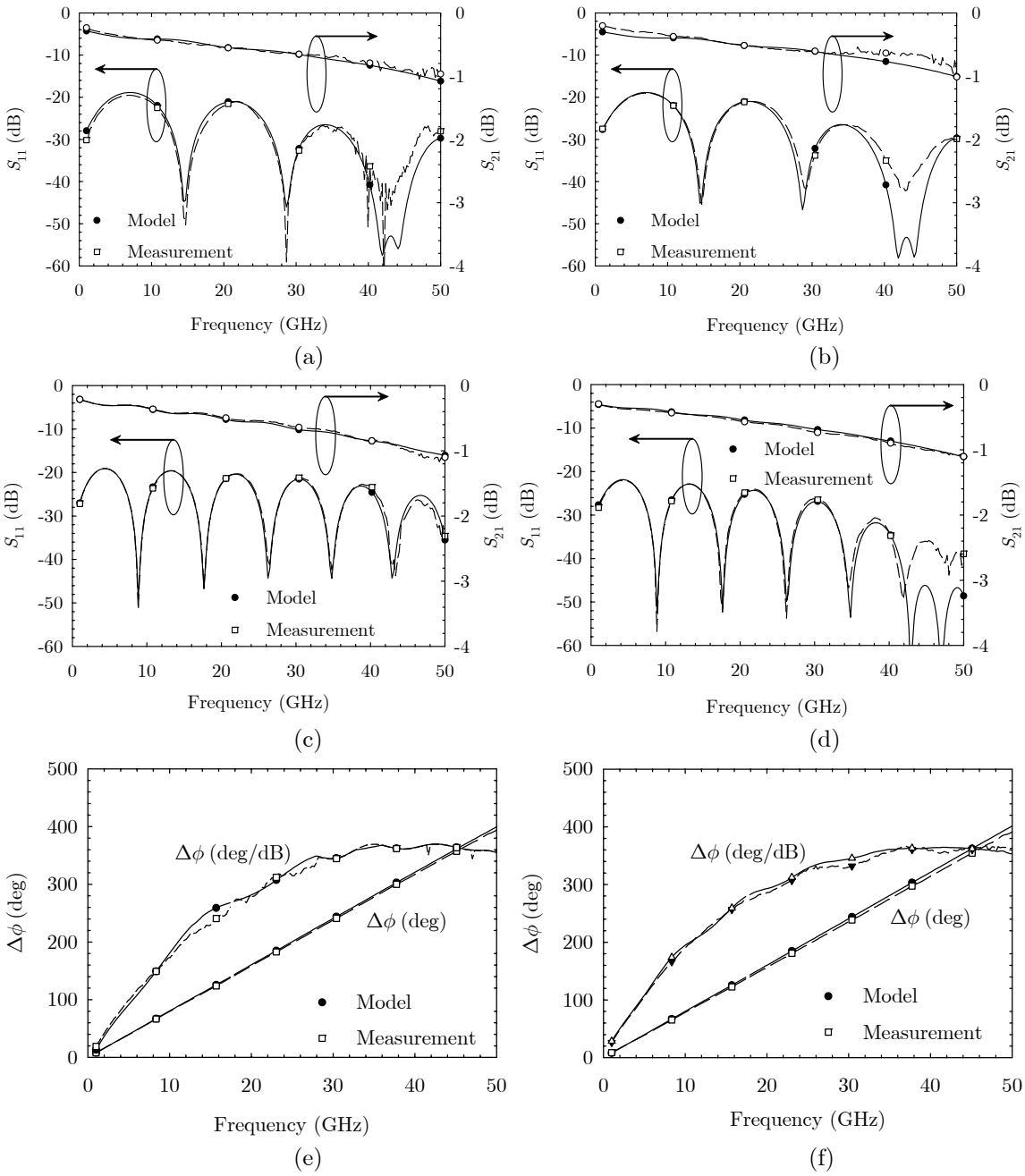


Figure 3.24: Comparison between measurements and equivalent circuit model for the 1-bit phase shifter, (a) S_{11} and S_{21} in the normal state for design 1, (b) S_{11} and S_{21} in the normal state for design 2, (c) S_{11} and S_{21} in the slow wave state for design 1, (d) S_{11} and S_{21} in the slow wave state for design 2, (e) $\Delta\phi$ and $\Delta\phi$/dB for design 1, (f) $\Delta\phi$ and $\Delta\phi$/dB for design 2.

3.7 Frequency Scaling (X and W-band designs)

The designs presented in the previous sections can be scaled to X-band (8-12GHz) or W-band (75-110GHz). The design technique is as follows:

- The ground-to-ground spacing (W) is set to $\lambda/5.5$ and $f_B = 2.6f_{max}$. Using (3.9) the spacing (s) between the shunt bridge and the capacitance C_{bs} is determined.

- From (3.7), approximate signal path through the slot is determined and this value of s_1 is used in (3.10) to find the ground-plane bridge capacitance.

- Accurate value of f_B is determined and $\Delta\phi$ per section is determined (3.12). The ground-to-ground spacing should be lower for the W-band design to reduce radiation loss.

Table 3.8 shows calculated parameters for X- and W-band design. Using Momentum and assuming a lossless metallization, the W-band design is simulated and the results for S_{11} and $\Delta\phi$ is shown in Figure 3.25. It is seen from this figure that the agreement between $\Delta\phi$ is not good. This may be due to reasons; a) the design equation does not account for inductive effect due to current bending and the parasitics associated with the bridge, b) due to non-linearity associated with the Bragg frequency beyond 100GHz.

Table 3.8: Design parameters for X-band and W-band design used in simulation.

	X-band	W-band
$S\,/\,W\,/S$ (μm)	100/100/100 (μm)	100/100/100 (μm)
$S_1/\,W_1/S_1$ (μm)	125/220/125 (μm)	50/40/50
s (μm)	1500	216
s_1 (μm)	3800	257
C_{bs} (fF)	95	29
C_{bg} (fF)	57	22

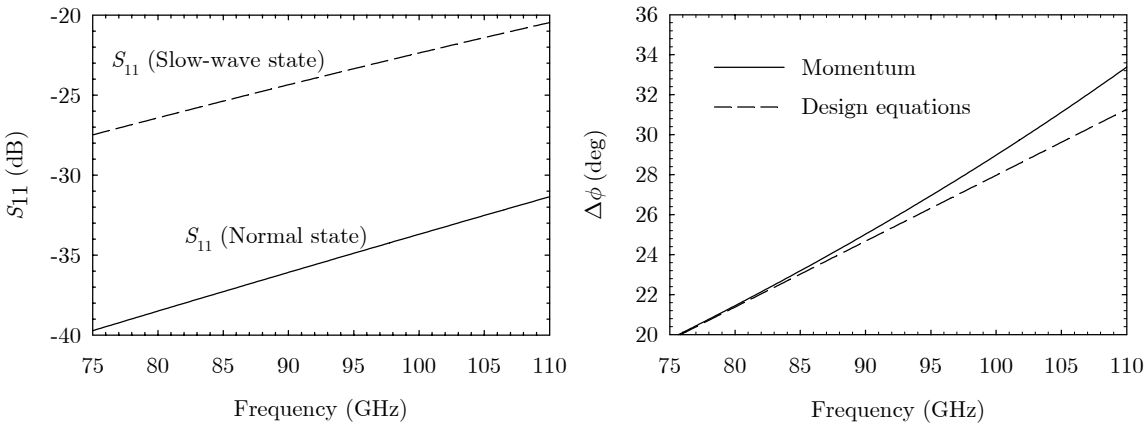


Figure 3.25: a) Simulated (Momentum) S_{11} in both the states for W-band design, b) comparison between simulated (Momentum) and calculated $\Delta\phi$.

3.8 Chapter Summary

The analytical model developed herein for the slow-wave phase shifter is based on the quasi-TEM approximation for a transmission line. For simplicity, the parasitics associated with the bridge is not included in the derivation. However, these equations were used to predict the optimal center conductor widths on different substrates. Using this as starting values, a semi-lumped model that include parasitics is derived. Experimental results for a 460μm long unit cell on quartz shows good agreement between measured and modeled data. A 1-bit (and 4-bit) phase shifter model is constructed by cascading 10 slow-wave unit cells. The agreement between the measured data and the model is good through 50GHz with 310°/dB at 50GHz. In the 2nd generation design, further improvement is seen by plating the lines and indicate loss-per-dB of 355°/dB. The result represent state-of-the-art performance for TTD phase shifter through 50GHz.

CHAPTER 4

Applications of Slow-wave Phase Shifter

The focus of this thesis is on the application of impedance matched slow-wave unit cell as low-loss millimeter-wave phase shifters. However, there are a number of other applications in which slow-wave unit cell can be useful. Some of the more significant applications are:

- Reconfigurable MEM transmission lines that can provide characteristic impedance tuning (Z_o-tuning) with constant phase.

- Electronically tunable multi-line TRL for automatic on-wafer calibration.

This chapter presents the results of using slow-wave unit cell for these applications, but no attempt is made to achieve the best performance.

4.1 Reconfigurable MEM Transmission Line with Z_o-tuning and β-tuning

The design of reconfigurable, multi-band radar and communications hardware can require dynamic adjustment of both time delays and characteristic impedance (Z_o) levels at various points within the signal paths. When considering just phased arrays, the need for time delay control is obvious. One example wherein the control of impedance levels is important is in the antenna design. There have been several published examples of reconfigurable antennas comprised of a radiating element(s) and Micro-Electro-Mechanical (MEM) switch(es); in such configurations the resonant frequency is varied and there may little change in the impedance at the selected operating frequency. However, when co-locating a MEMS device with a radiating element is undesirable, a more suitable solution may be a dynamic impedance-matching network.

This section presents a reconfigurable MEMS-based transmission line in which there is independent control of the propagation delay and the characteristic impedance. Variations of MEMS tuners that have recently been published include: stub-type topologies, with extensive Smith-chart coverage through 20 GHz [51-53]; and low loss, distributed MEM transmission lines (DMTLs), with a 5:1 (50Ω:10Ω) impedance match [54, 55]. The approach presented here differs in that separate control of inductive and capacitive MEMS devices in discrete unit cells is used either to maintain a constant LC product (constant Z_o) or a constant L/C ratio (constant β), while changing the ratio or product, respectively.

The tunable Z_o-line with constant β-mode is complimentary to the slow-wave phase shifter that was presented in chapter 3. The new design uses cascaded metal-air-metal (MAM) capacitors at the input and the output of the slow-wave sections. Experimental results for a 1-bit, 7.4mm (10 cascaded unit cells) long line demonstrate a Z_o tuning ratio of ~ 1.27 (52Ω/40Ω) through 50GHz with 2Ω variation over frequency. The 1-bit version can also be operated as a phase shifter by addressing the MAM capacitors differently. The measurement result indicate $\Delta\phi$/dB ~358°/dB (or 58°/mm) at 50GHz with S_{11} < -25dB. In a 5-bit version, the 1st bit is configured as a tunable Z_o element and other bits are operated as a phase shifter. Experimental results for the dual mode operation indicate a $\Delta\phi$/dB of ~ 300°/dB and impedance shift of 52Ω to 40Ω.

4.2 Design and Measured Performance

The unit cell shown in Figure 4.1 is comprised of a slow-wave section [56] with MAM capacitors at the input and output. The two distinct phase states of the slow-wave section are the *normal state* (when the ground plane beams are actuated and the shunt beam is non-actuated) and the *slow-wave state* (when the shunt beam is actuated and the ground plane beams are non-actuated). The measured performance for the 400μm long slow-wave section indicate $\Delta\phi$=46°, S_{11} < -25dB and worst-case S_{21} is -0.15dB. These results represent approximately 25% improvement over the 2nd generation slow-wave phase shifter result presented in chapter 3. The footprints of the slow-wave unit cell is listed in Table 4.1. The maximum conductor width (~600μm) is less than $\lambda g/8$ at 50GHz to maintain single-mode

operation, and typical actuation voltage for the beams is approximately 28-32V. Furthermore, for the spacing specified herein, the calculated f_B is approximately 138GHz.

Table 4.1: CPW dimensions and bridge capacitance (C_{bs} and C_{bg}) for the slow-wave unit cell that is used in this section.

f_B =138GHz	
$S/W/S$ (μm)	50/200/50
$S_1/W_1/S_1$ (μm)	100/120/100
s (μm)	200
s_1 (μm)	647
C_{bs} (fF)	12
C_{bg} (fF)	31

Z_o-tuning is realized by operating the slow-wave section in conjunction with the MAM capacitors: the low-Z_o mode (*state* 1) corresponds to the normal state with actuated MAM capacitors, while the high-Z_o mode (*state* 2) is realized in the slow-wave state with non-actuated MAM capacitors. Maintaining a constant propagation constant (β) with Z_o-tuning is achieved by proper selection of the capacitance ratio (C_r=C_{dn}/C_{up}) of the MAM capacitor. Specifically, $\Delta\phi$ due to the MAM capacitor ($\Delta\phi_{\text{MAM}}$), separated by a 270μm long uniform CPW line, offsets the $\Delta\phi$ due to the slow-wave section ($\Delta\phi_{\text{slow-wave}}$). For a given spacing ($s$) between capacitors and the total length (L), equation (4.1) is used to calculate C_r.

$$\Delta\phi = \frac{360\ \omega\sqrt{L_{tn}C_{tn}}}{2\pi}\left[\left(\sqrt{1+\frac{C_{bs}}{sC_{tn}}}\right)-\left(\sqrt{\left(1+\frac{C_rC_{bs}}{sC_{tn}}\right)}\right)\right]L \qquad \text{deg} \tag{4.1}$$

Where, L_{tn} and C_{tn} are the per-unit-length inductance and capacitance in the normal state [56]. Using (4.1), C_r=2.6 for $\Delta\phi$=46°, s=270 μm, C_b=24fF, L_{tn}=0.33 nH/mm, C_{tn}=0.07 pF/mm, and L=740 μm.

The different Z_o levels are determined by considering the transmission line section between MAM capacitors (the slow-wave section) as a uniform CPW line. The effective impedances (Z_{state1}, Z_{state2}) for both the states is then calculated using (4.2). For the distributed parameters used herein, these impedances can be set to approximately 50Ω or 38Ω; parasitic

loading of the shunt beam and other discontinuity effects increase the actual levels to the 40/52Ω values stated above.

$$Z_{state1} = \sqrt{\frac{L_{ts}}{1 + \frac{C_{bg}}{s_1 C_{tn}}}} \quad ; \quad Z_{state2} = \sqrt{\frac{L_{tn}}{1 + \frac{C_{bs}}{s C_{tn}}}} \tag{4.2}$$

The spacing s_1 is total length between the between the capacitors via the slow-wave section.

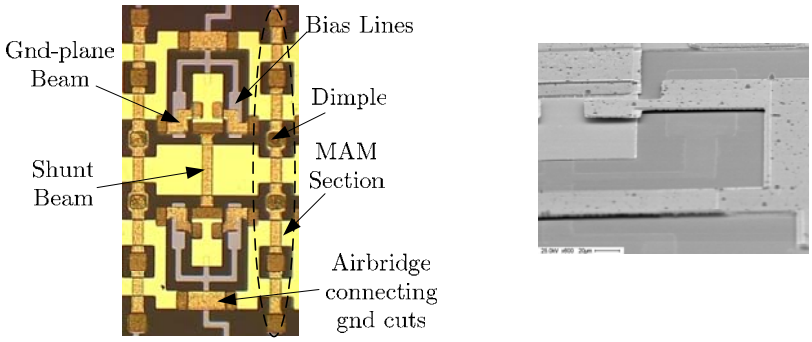


Figure 4.1: Microphotograph of the constant β tunable Z_o slow-wave unit cell (left) and SEM picture of the structure.

The tunable-Z_o unit cells were fabricated on a 500μm thick quartz substrate (ε_r=3.8, tanδ=0.0004) using the basic process described in chapter 3. The Si_xN_y layer previously located where the bias lines enter the ground conductor, is avoided and biasing to the beams enters through the ground plane cuts (the ground cuts are connected via air bridge). To simplify fabrication process, the CPW lines are not plated. The DC isolation between the MAM capacitors and the center conductor is realized by using a dimple in the slots that is 0.5μm higher than the metal layer and supports an interconnecting beam (Figure 4.1).

Measurements were performed from 1–50GHz using a Wiltron 360B vector network analyzer and 150μm pitch GGB microwave probes. Figure 4.2 (a) shows the measured S_{11} and extracted Z_o (Figure 4.2 (b)) from 2-port S-parameter data for the high- and low-Z_o modes (states 1 and 2 in the figure). A full wave EM simulation using ADS Momentum was performed and the results are included in the figure. The difference in S_{11} between the two Z_o-states (~15dB) is due to the change in the characteristic impedance from 40Ω to 52Ω. Extracted C_r from the measured data is approx 2.57 (=59.8fF/23.2fF) which agrees favorably using (4.2).

The measured phase difference between the states was less than 2.5° ($< 2\%$) for βl =150° at 50GHz. The worst-case S_{21} was approximately -0.15dB and -0.25dB for Z_{eff} =52Ω and 40Ω, respectively. The measured S_{21} at 50GHz for the MEMS transmission line is 0.08dB less than a uniform CPW line of equal electrical length. The increase in loss may be due to the contact resistance and small leakage in the bias circuitry.

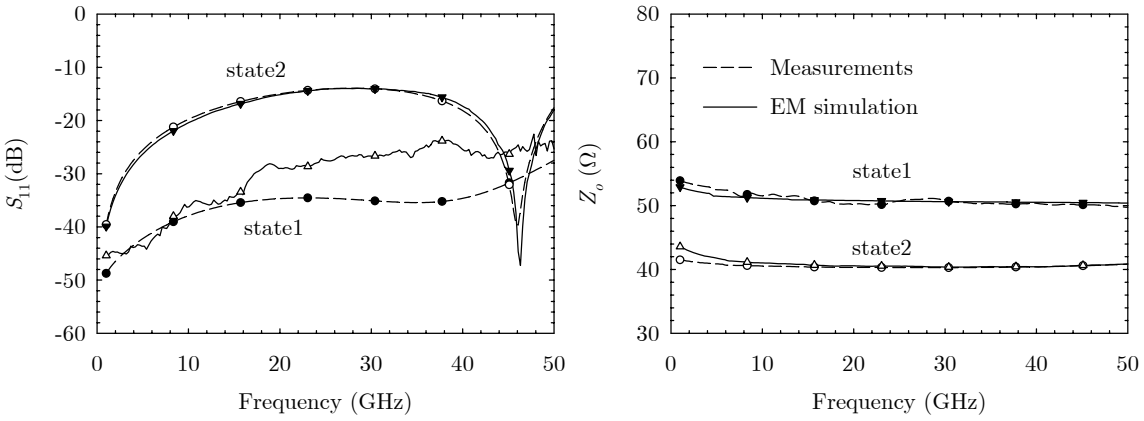


Figure 4.2: Measured S_{11} (dB) and extracted Zeff in state 1 and state 2 for the 1-bit tunable Z_o unit cell. Solid lines represent EM simulation data.

4.3 1-bit Tunable Z_o-line and 1-bit Phase Shifter Performance

The schematic of the 1-bit tunable Z_o line with ten cascaded sections (7.4mm long) is shown in Figure 4.3. As with the unit cell, the MAM capacitors are actuated only when the slow-wave section is operated in the normal state and remain in the non-actuated otherwise. Figure 4.4 shows a comparison between the measured and simulated S_{11} data referenced to 50Ω in both the states. The simulated results were obtained by cascading full-wave analysis data for the unit-cells in the circuit simulator. The extracted effective impedance in this case is 52Ω/41Ω and the worst-case S_{21} for both the states is approximately 1.23dB and 2.2dB at 50GHz.

Assuming an effective relative dielectric constant of 2.46 (from Multi-line TRL calibration), the effective length is approximately 1.6cm. The maximum phase difference between the states is less than 3.6% and absolute phase in both the states is shown in Figure 4.5. The measured S_{21} of the tunable Z_o-line is 0.3-0.45dB lower than a uniform CPW line of the same electrical length.

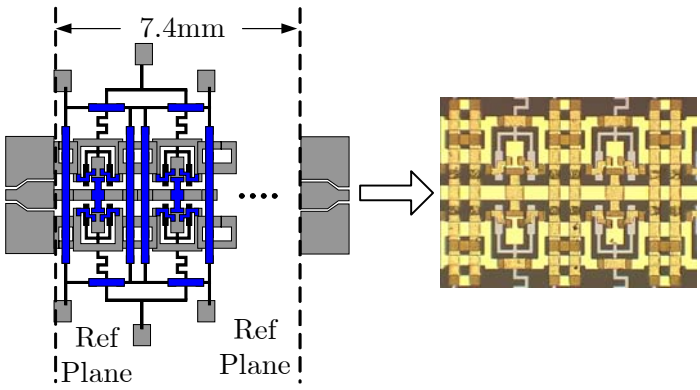


Figure 4.3: Schematic of 10-section cascaded tunable Z_o unit cell and a photograph two unit cells in the device.

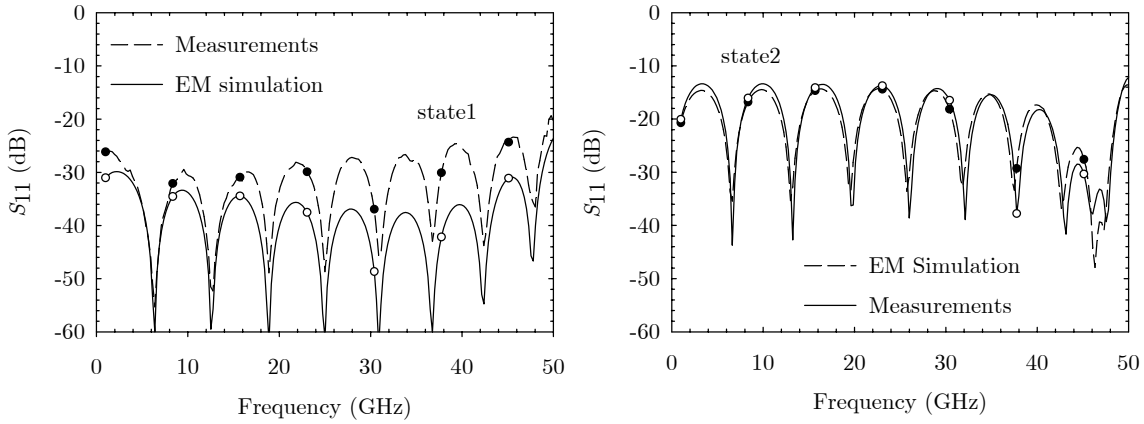


Figure 4.4: Comparison of measured (dashed) and simulated (solid) S_{11} (dB) of a 7.4mm long tunable Z_o- line with constant propagation constant in both states, a) state 1, b) state2.

The schematic shown in Figure 4.3 can be reconfigured to operate as a 1-bit phase shifter with maximum phase shift by actuating the MAM capacitors in the slow-wave state of the slow-wave sections. The limiting factor in this approach is the Bragg frequency (f_B). The calculated f_B for the design is approximately 51GHz with the MAM capacitors actuated [23]. The usable frequency range is then only up to 30GHz, since the non-linear effects are prominent around $0.5f_B$. Therefore, for 1-50GHz operation, the MAM capacitors remain in the non-actuated state and the phase shift is primarily due to the slow-wave section. A electromagnetic optimization was performed with the pedestal height as the variable. A initial guess value of 2μm was used and other unit cell parameter was fixed. The pedestal height for the shunt and the ground-plane bridge was varied by the same factor. For

example, if the pedestal height for the shunt bridge in the normal state is equal to 2μm, then the ground plane bridge for the slow-wave state also had the same value. The comparison between EM simulation (with gap height of 1.65μm) and measured data (S_{11} and $\Delta\phi$) for the unit cell in both the states is shown in Figure 4.6.

From Figure 4.6, the measured S_{11} is below -25dB for both states through 50GHz. Furthermore, the measured and simulated differential phase shift is within 6%, with a measured $\Delta\phi$= 430° at 50 GHz. The discrepancy in the predicted phase shift is due to the non-uniformities in height from unit cell to unit cell and irregular dimple height across the length of the transmission line in the fabricated device. Measured worst-case S_{21} was equal to -1.2dB at 50GHz, translating to $\Delta\phi$/dB of 360°/dB which is 40°/dB better than the 1st generation slow-wave results.

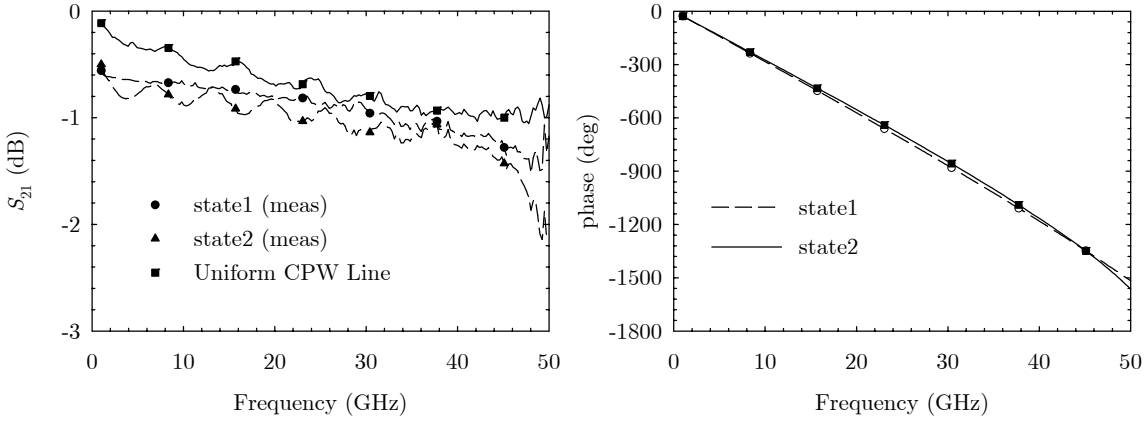


Figure 4.5: Measured performance of the 10-section 1-bit tunable Z_o device in both the states, a) S_{21} of the tunable transmission line and S_{21} data of a 1.6cm long 50Ω CPW line, b) $\Delta\phi$ in both the states.

4.4 Combined Z_o -Tuning and β-Tuning

A 5-bit version of the device in is designed to provide combined Z_o-tuning and β-tuning. This bi-modal operation is achieved by configuring one bit (2 unit cells) to provide Z_o-tuning and the other four bits to provide β-tuning. State 1 is operated such that the first bit acts as a 40Ω section and bits 2-5 are in the normal phase state. Conversely, in state 2 the first bit acts as a 52Ω section and bits 2-5 are in the slow-wave phase state. Figure 4.7

shows the measured S_{11} in both states and a comparison of the measured and simulated $\Delta\phi$ between the states. This example demonstrates the ability to control phase and impedance independently.

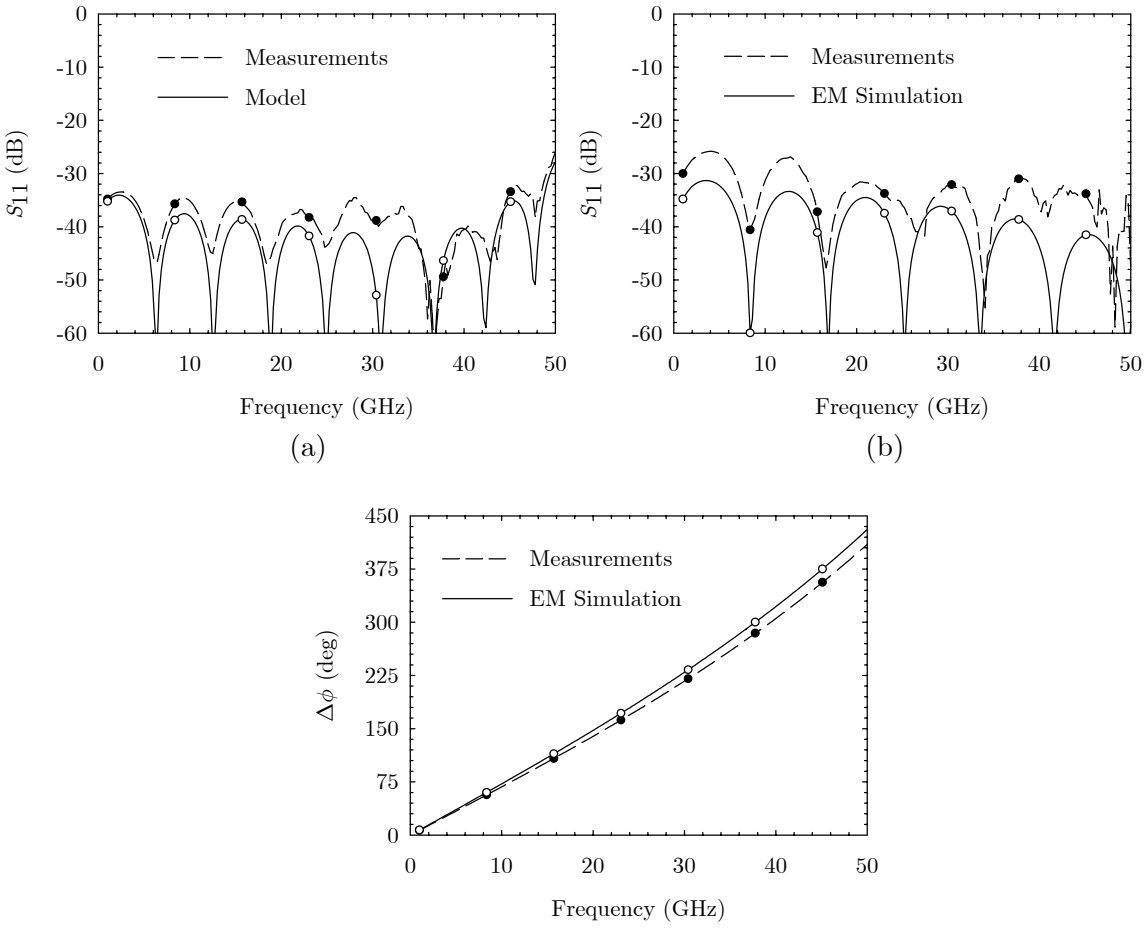
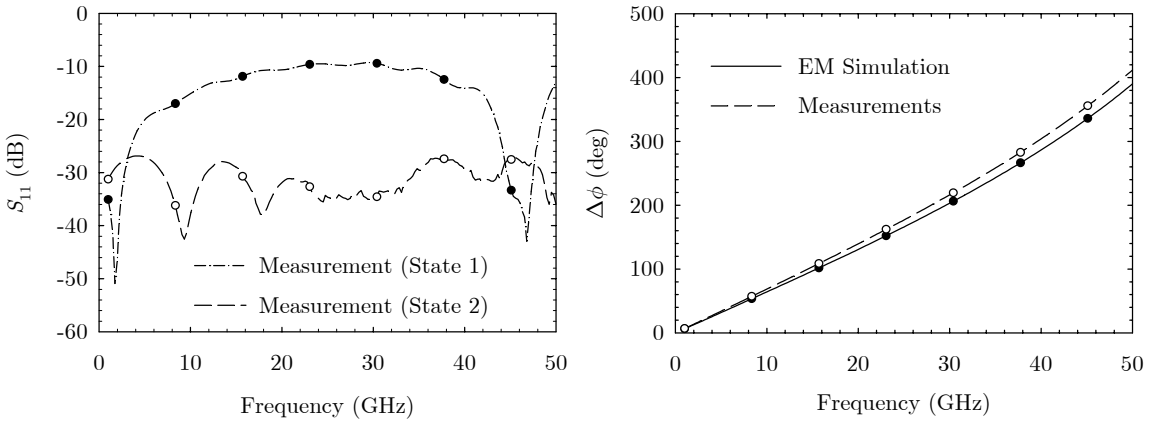


Figure 4.6: Comparison between measurements and optimized EM simulation for the 10-section device in phase shifter mode operation, a) S_{11} in the slow-wave state, b) S_{11} in the normal state, c) $\Delta\phi$. The solid line in each plot represent EM simulation data and the dashed line represent measured data.



(a) (b)

Figure 4.7: Measured performance of a 10-section device in a bi-modal operation, a) S_{11}, b) $\Delta\phi$. Solid lines represent EM simulation data and dashed lines represent measured data.

4.5 Electronically Tunable Multi-line TRL

Considerable effort has been made to develop accurate techniques for calibrating vector network analyzers (VNAs) based on the use of space conservative standards [57]. The multi-line Thru-Reflect-Line (TRL) method is very accurate for broad band calibration [58]; however the required use of two or more delay lines can lead to inefficient utilization of wafer surface area. Space conservative calibration methods such as the SOLT, LRM and LRRM provide accuracy that is close to a multi-line TRL, provided that broad band models for the standards are available. An alternative to reducing the footprint of standards is to use an electronic phase shifter that can represent multiple delay lines by changing its phase state. It is very important that there be minimal variation in the effective characteristic impedance between different phase shifter states, since the delay lines ideally differ only in transmission phase and loss. An added advantage of the electronic calibration approach is that a minimal number of probe placements is necessary, thereby minimizing this aspect of calibration error.

A multi-bit TTD phase shifter with a quasi-constant impedance can emulate multiple delay standards that is required for accurate broad band (1-50GHz) calibration. A DMTL based topology cannot be used for such large bandwidth since $\Delta\phi$/cm is only 180° for S_{11} < -

20dB. Typically, a commercial probing station can provide a maximum lateral (x-y) movement of only 1.5-1.6cm.

The goal of this work is to demonstrate the new phase shifter topology in a multi-bit configuration to realize the thru and delay lines of a TRL calibration set ("Tunable TRL"). Experimental results for the 1st generation 4-bit phase shifter that is 4.6mm-long demonstrate S_{11} less than -21dB through 50GHz with $\Delta\phi$/dB of approximately 317°/dB (or 91°/mm) at 50GHz (see chapter 3).

The multiple states of the phase shifter designed in this work provide $\Delta\phi$ of 45°, 90°, 180° and 225°at 35GHz. The MEMS tunable 4-bit phase shifter presented herein is used to realize four delay line calibration standards in a multi-line TRL. The normal-mode operation (or $\Delta\phi$=0°) of the phase shifter mimics the thru standard. The different bits of the slow-wave phase shifter are actuated in order to emulate the delay line standards. The open standard is realized using a separate, uniform CPW line. The effective offset lengths of the delay lines extracted from measured $\Delta\phi$ at 35GHz are approximately 739μm $\Delta\phi$=47°), 1460μm ($\Delta\phi$=93°), 2931μm ($\Delta\phi$=188°) and 3669μm ($\Delta\phi$=235°).

The results of a Tunable TRL calibration are compared with a calibration performed using uniform CPW line standards on the quartz substrate. The reference planes for both calibrations are established at the probe tips with Z_o corrected to 50Ω. Furthermore, same number of line standards was used in both the calibrations. The maximum error bound $|S_{ij}\text{-}S_{ij}'|_{max}$ between multi-line TRL standard on quartz (TRL1) and Tunable-TRL on quartz is computed using the calibration comparison method [58]. The comparison was also made between standard TRL on a CS-5[1] substrate (TRL2) and the Tunable TRL, as illustrated in Figure 4.8.

The calibration comparison method is based on the assumption that a perfect multi-line TRL calibration using conventional standards calculates the true scattering parameters S_{ij} of a device from uncorrected measurement data. However, an imperfect TRL calibration

[1] CS-5 is a commercial calibration substrate manufactured by GGB Industries, Naples, FL.

based on standards with errors (Tunable TRL) will result in calibration coefficients which differ from those of the perfect calibration. These imperfect calibration coefficients calculate scattering parameters S_{ij}', which differ from the actual scattering parameters S_{ij}. The calibration-comparison method determines an upper bound for $|S_{ij}\text{-}S_{ij}'|$ from differences in the perfect and imperfect calibration coefficients when $|S_{ij}| < 1$ and $|S_{12}\,S_{21}| < 1$. The upper bounds indicate the maximum possible difference in any of the four *S*-parameters for a 2-port passive device.

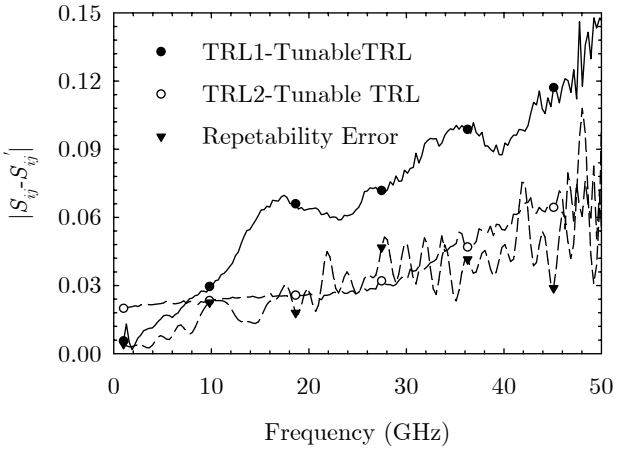


Figure 4.8: Upper bound error $|S_{ij}\text{-}S_{ij}'|_{max}$ between standard TRL and Tunable TRL.

It is seen from Figure 4.8 that the upper bound between TRL1-Tunable TRL and TRL2-Tunable TRL increases linearly with a maximum bound of 0.14 at 50GHz for TRL1-Tunable TRL calibration sets. The increase in the error bound is due to the slight increase in the insertion loss and a 2% deviation from 50Ω for the 4-bit phase shifter when compared to uniform CPW line. For completeness, the repeatability of the two Multi-line TRL calibrations on the quartz substrate is also shown in the figure. In order to verify the accuracy of the predicted error bounds two verification devices were measured:

a) 9mm long delay line standard on quartz substrate

A 9mm long uniform CPW line was measured after performing a Tunable TRL and a TRL1. It is seen from (a) that the measurement results performed using the Tunable TRL and TRL1 agree well. Furthermore, the maximum vector difference between the two measured S-parameters is within the estimated error bounds.

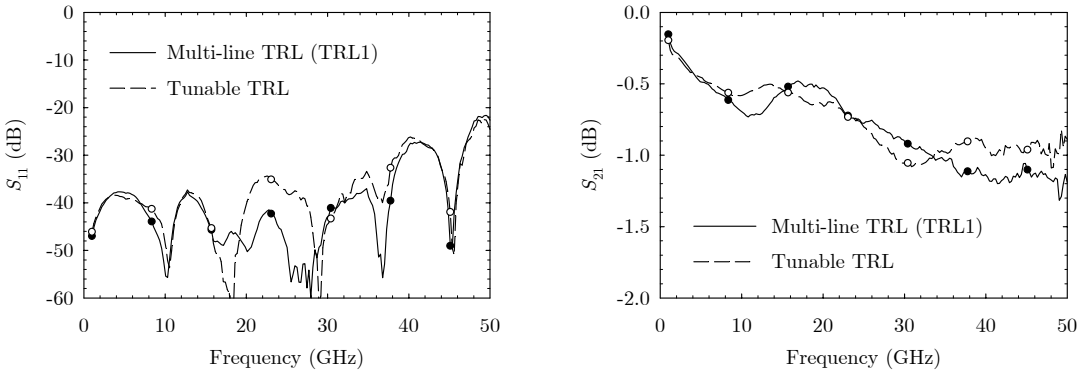


Figure 4.9: S_{11} and S_{21} of 9mm long verification structure. The line was measured after a Tunable TRL calibration and a standard TRL on quartz (TRL1).

b) 25Ω *Load on a CS-5 substrate*

A 25Ω load verification structure was measured on 700μm thick CS-5 substrate (ε_r=9.9, tanδ=0.002) after performing a on-wafer calibration (TRL2) using uniform CPW line standards. It is seen from Figure 4.10 that the measurement results performed using Tunable TRL and TRL2 agree well and the maximum vector difference between the S-parameters is within the predicted error bound. Several other DUT such as 12.5Ω, and 100Ω load on GaAs substrate was measured and it was found that the agreement between Tunable TRL and TRL calibration is within the error bounds predicted using calibration comparison method.

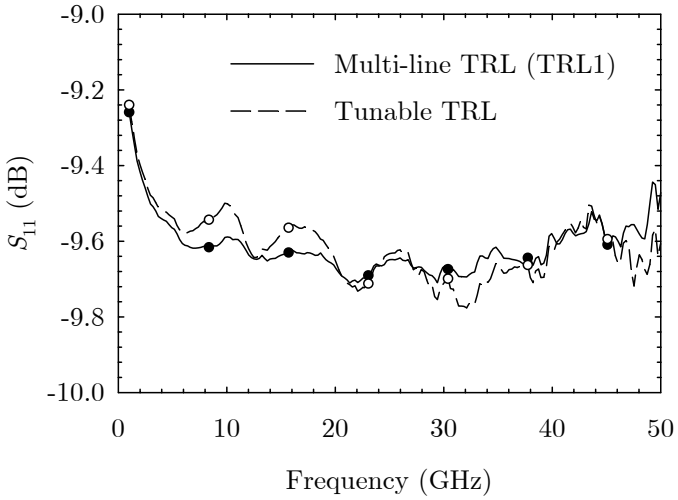


Figure 4.10: S_{11} of a 25Ω load verification structure on a 700μm thick CS-5 substrate.

4.6 Chapter Summary

In this chapter two novel applications that utilize slow-wave phase shifter is presented. A reconfigurable MEMS transmission line based on cascaded capacitors and slow-wave sections has been developed to provide independent Z_o- and β-tuning. Experimental results for the Z_o-mode of operation, provides Z_o-tuning from 52 to 40Ω (+/-2Ω) with constant phase between the states through 50GHz. The same transmission line is reconfigured by addressing the MEM elements differently for β-tuning. Furthermore, the combined effect of Z_o- and β-tuning is also demonstrated. Furthermore, an electronically tunable TRL calibration set that utilizes a 4-bit phase shifter topology is presented. The accuracy of the tunable TRL is close to a conventional multi-line TRL calibration. The Tunable TRL method provides for an efficient usage of wafer area while retaining the accuracy associated with the TRL technique, and reduces the number of probe placements. The measured results presented herein is state-of-the-art performance for both the applications.

CHAPTER 5

Summary and Future Work

This thesis presented the application of periodically loaded slow-wave unit cell and focused on the use of this as a millimeter wave phase shifter. Optimized phase shifters were developed at 50 GHz with a maximum performance of 350°/dB or 360° phase shift with 1.1 dB loss. These are the lowest loss millimeter wave phase shifters reported to date. Furthermore, for the same $\Delta\phi$ the size of these devices are 75% smaller than the state of the art results presented till date. In current phased array systems, there is a PA/LNA chip at each antenna element in order to limit the effect of the loss in the phase shifters. However, with 1 dB insertion loss or less, the number of PA/LNA chips needed could be reduced by using one chip for several antenna elements. This would greatly reduce the cost of large phased array systems which typically have thousands of antenna elements.

In addition, the slow-wave phase shifter was applied to a tunable transmission line that can provide independent Z_o-tuning with a tuning ratio of 1.2 and β-tuning with $\Delta\phi$/dB of $\sim$ 300°/dB. Such performance would lead to new innovative designs for phased array systems.

An electronically tunable calibration (1-50GHz) is made possible by realizing all the line standards using the multi-bit phase shifter in a typical multi-line TRL. The Tunable TRL method provides for an efficient usage of wafer area while retaining the accuracy associated with the TRL technique, and reduces the number of probe placements from five to two (with potentially no change in probe separation distance).

5.1 Future Work

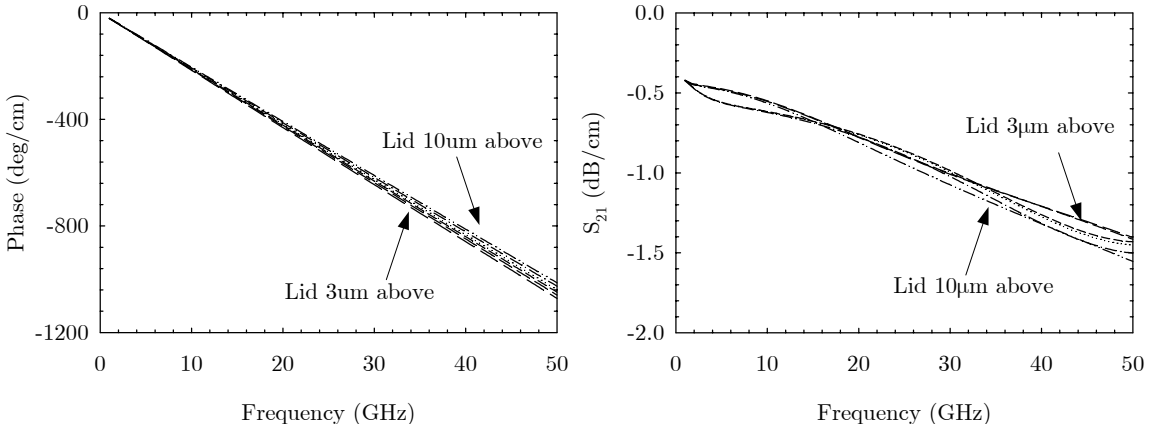
a) Tunable Filter

The low loss performance of the slow-wave unit cell can be used in a high Q filter design by cascading two or more unit cells to emulate a $\lambda/4$ or $\lambda/2$ open resonators. Conventional tunable filters typically utilize YIG resonators, active resonators or varactors as the tuning element. Varactor-based tunable filters have relatively low Q values in the range of 2-3 [45], due to the high series resistance of the diodes. Tunable filters which maintain excellent filter performance will greatly enhance the functionality of receiver systems and reduce the need for space consuming filter banks. A 0.1dB Chebyshev prototype bandpass filter is designed on quartz using $\lambda/2$ shunt open stubs and $\lambda/4$ connecting lines. Although, the slow-wave unit cell can be used to implement these transmission lines, it was not attempted in this work. However, they were implemented on 500μm thick quartz substrate using DMTL. The comparison between measured and EM simulation is presented in Appendix D.

b) *Phased Array*

The applications of phase shifter in high frequency circuits are numerous, but the most important application is in a phased array system. It is easier to integrate the phase shifter described in this work with a planar antenna (example: microstrip, CPW, or slot-line) to realize a phased array system than a waveguide or coaxial based antenna. For example, in a aperture coupled antenna the lid (where the radiating element is typically located) can act as a package for the MEM device (0-level wafer package) [59]. The design of aperture coupled antenna is given in [59, 60, 61]. Before such integration is attempted it is desirable to understand the effect of lid on the phase shifter performance. As an example, a 1cm long 50Ω line on quartz (25/250/25) is simulated using momentum with a 100μm thick quartz lid (ε_r=3.8) on top of the CPW line. The lid is simulated with a minimum location of 3μm above the CPW (since MEM structures are located 2μm above the CPW). Quartz lid is chosen so that the mismatch in the dielectric half-space above the CPW plane is minimized. Figure 5.1 shows the simulated data for absolute phase (deg) and S_{21} (dB/cm). It is seen

from this figure that there is ∼7% change in absolute phase and 10% increase in S_{21} (dB/cm) when the lid is located at 3μm versus 10μm. Furthermore, it was found that in order to avoid any interference from the lid, a spacing of 20μm or more is required. Experimental verification of the above claim is required before using the phase shifter in an aperture coupled antenna or packaging the device with a quartz lid. Similar studies can be done with other dielectric constant to find the optimum packaging material.



(a) (b)

Figure 5.1: Momentum simulation of a 1cm long line on 500μm thick quartz with 100μm thick quartz lid at different heights above CPW line, a) Absolute phase in deg, b) S_{21} (dB/cm).

c) *Power Handling Measurement*

Power handling measurement of the phase shifter needs to be done. The power handling of the phase shifter can be limited by either the current density on the transmission line causing excessive heating or by the MEMS bridges being pulled down due to the average RF voltage on the line. Since the electrostatic force attracts the bridge towards the center conductor with either a positive or negative voltage, it appears as a rectified RF voltage and the average voltage level of the rectified sine wave due to the RF power on the line is pulling on the bridge ("*self-actuation*") [32].

The average voltage of a rectified sine wave is given by:

$$V_{avg} = \frac{1}{T}\int_{0}^{T/2} V_o \, sin\,(\omega t)\, dt = \frac{V_o}{\pi} \tag{5.1}$$

where $T = 2\pi/\omega$. The RF power in terms of the peak voltage, V_o is given by:

$$P = \frac{{V_o}^2}{2Z_o} \tag{5.2}$$

Where, Z_o is the characteristic impedance of the transmission line and typically near 50Ω. Using (5.2), the RF power on the DMTL can be written as:

$$P = \frac{\pi^2 {V_{avg}}^2}{2Z} \tag{5.3}$$

Using this equation, the predicted RF power level at which the slow-wave unit cell, with a 25V pull down voltage, will be pulled down is 61.6W while for a pull-down voltage of 20 V, the RF power level is 39.5W.

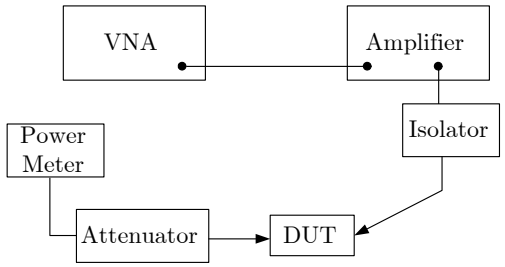


Figure 5.2: Typical setup for power handling measurement of slow-wave phase shifter.

Typical setup for power handling measurement is shown in Figure 5.2 [24]. It is believed that the slow-wave phase shifter can handle higher power than DMTL or other electrostatic based MEM device where the anchor is typically located on the CPW ground. This is because, the shunt bridges (C_{bs}) is not anchored on the CPW ground and the ground-plane bridges (C_{bg}) does not interact with the center conductor. Therefore, high power RF signal does not have affect the bridge movement.

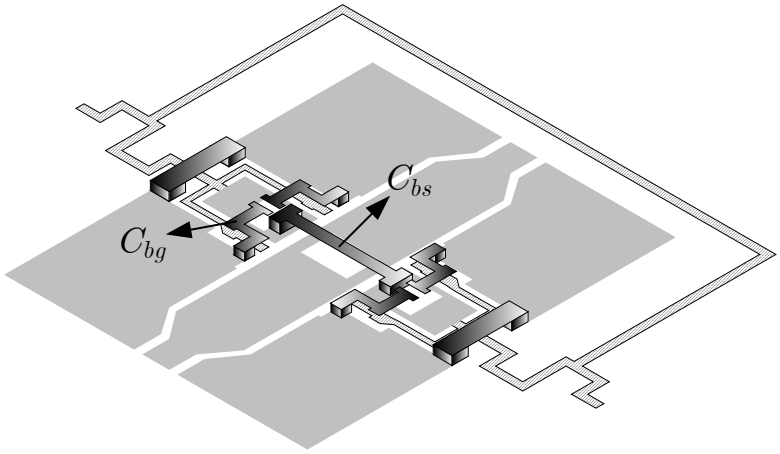


Figure 5.3: Schematic of the slow-wave unit cell.

However, it is possible that the large amount of RF current in the center conductor can heat up the bridges such that some amount of annealing occurs resulting in a higher pull-down voltage. For quartz based designs, this heating is worse due to low thermal conductivity of quartz (0.014W/cm-K), compared to the thermal conductivity of silicon which is 1.5 W/cm-°C [23].

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APPENDICES

APPENDIX A: CPW TRANSMISSION LINE LOSS

A.1 CPW Lines on Quartz

This appendix presents measured and predicted results for loss (dB/cm) on 500μm thick quartz substrate. For all the measured data presented herein, the line is measured on a 700μm thick air cavity to avoid any excitation of parallel-plate waveguide mode [55] and the reference impedance is set to the line Z_o. The conductor loss (α) calculated from conformal mapping technique in [46] is quoted again in (A.1):

$$\alpha(W,S) = \frac{8.686R_s\sqrt{\varepsilon_{eff}}}{4\eta_o SK(k)K(k')\left(1-k^2\right)}\left[2\left(\pi+\ln\left(\frac{4\pi W(1-k)}{t(1+k)}\right)\right)\right] + \frac{8.686R_s\sqrt{\varepsilon_{eff}}}{4\eta_o SK(k)K(k')\left(1-k^2\right)}\left(\frac{2S}{W}\left(\pi+\ln\left(\frac{4\pi W(1-k)}{t(1+k)}\right)\right)\right) \quad dB/length \tag{A.1}$$

where $K(k)$ is the complete elliptic integral of the first kind, $k = W/(W+2S)$, $k' = \sqrt{1-k^2}$, t is the metal thickness, R_s is the surface resistance given by $R_s = \left(\pi f\mu/\sigma\right)^{-1/2}$, and σ is the conductivity of the metal.

a) 1μm *thick evaporated metallization* (*Cr/Au*)

The CPW lines (in Table A.1) were fabricated on 500μm thick quartz (ε_r=3.8) with 200Å of Cr and 1μm thick evaporated Au. The predicted loss (in dB/cm) using (A.1) versus frequency and the measured data for (Line 1 and Line 7) is shown in Figure A.1. As can be seen, for the same metal thickness, two different correction factors are required to match the measured loss data. This was verified for all the lines and loss versus CPW pitch ($= W/(W+2S)$) at 50GHz is shown in Figure A.1. The multiplication factor is chosen such that best possible match is obtained through 50GHz (instead of just matching the 50GHz data point). Therefore, some of the data points shown in this figure is slightly off the predicted curve.

Table A.1: CPW dimensions for the lines used in this section. The resistance per unit length of each line is extracted from the measured data.

	W	S	R_t (Ω/cm) at 50GHz
Line 1 *	76	112	10.97
Line 2	100	100	7.98
Line 3	120	90	7.68
Line 4	144	78	8.25
Line 5	160	70	8.87
Line 6	110	45	11.29
Line 7 *	140	30	13.92
Line 8	230	35	11.15

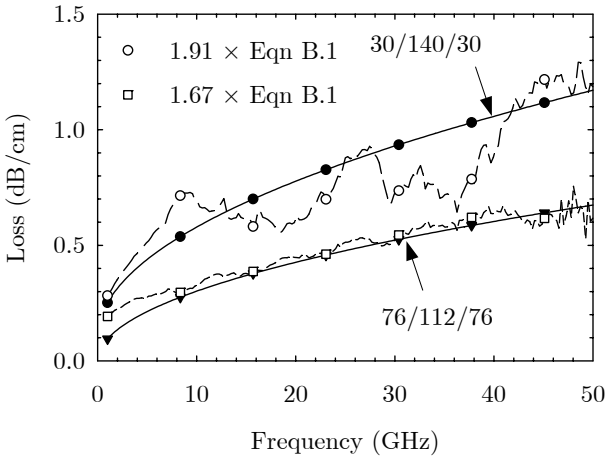


Figure A.1: Comparison between measured and predicted loss versus frequency.

b) 3μm *Electroplated metallization* (*Ti/Au*)

The CPW lines in Table A.1 was electroplated up to 3μm and the comparison of measured and predicted loss (Line 2 and Line 8) versus frequency is shown in Figure A.3. In Figure A.4 the comparison between measured and predicted loss (dB/cm) versus CPW pitch at 50GHz. It is seen that the correction factor required to match the measured data is the same for the lines (except for Line 1 and 7).

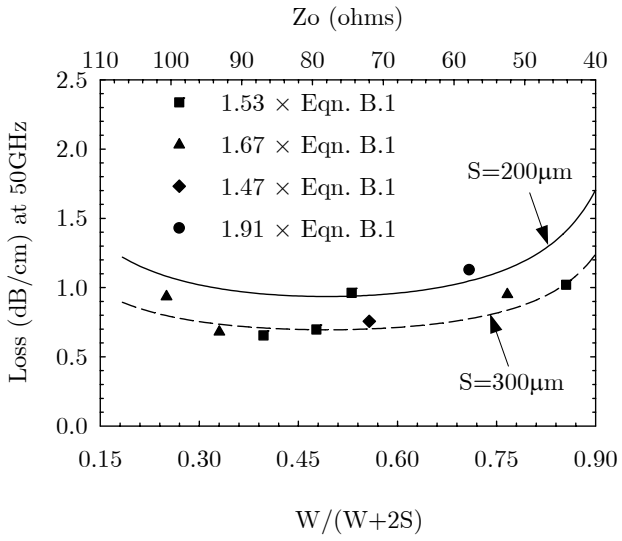


Figure A.2: Comparison between measured and predicted loss at 50GHz versus CPW pitch for 1μm evaporated line. For the data presented herein, four different correction factor is used to match the measured data. The characteristic impedance for the lines is listed above the plot.

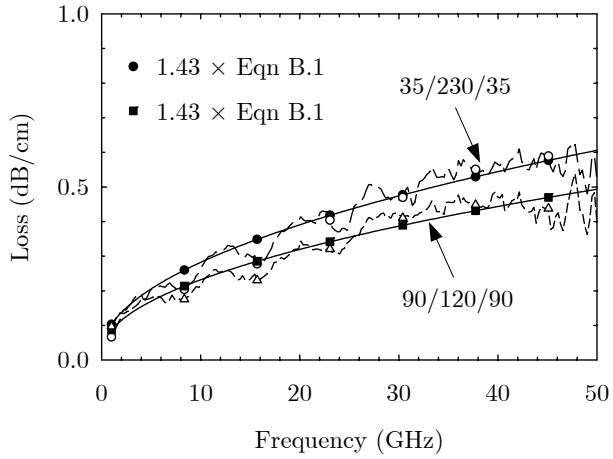


Figure A.3: Comparison between measured and predicted loss (dB/cm).

A.2 CPW Lines on Silicon

This section presents measured and modeled data for CPW lines measured on 425μm thick silicon ($\rho > 2000\Omega$-cm). Table A.2 shows the footprints of the lines used in this work. The comparison between measured and modeled loss (dB/cm) data for the two lines ("*" in Table A.2) is shown in Figure A.5. As with the measured data on quartz, the loss data on

silicon required a multiplication factor that varies with CPW pitch (Figure A.6). This multiplication factor is used in calculating the (dB/cm) versus CPW pitch and the result is shown in Figure A.7.

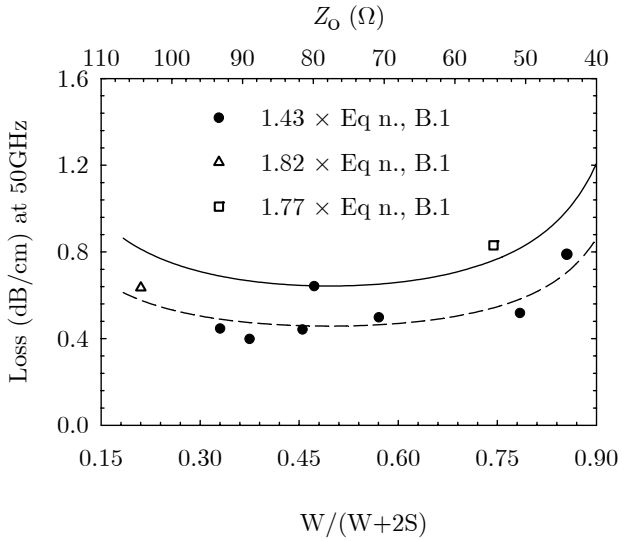


Figure A.4: Comparison between measured and predicted loss at 50GHz versus CPW pitch for 3μm plated lines.

Table A.2: CPW footprints used on high resistive silicon (ρ >2000Ω-cm) substrate.

W	S	Z_o (Ω)	W	S	Z_o (Ω)
40 *	17.5	46.06	80	45	49.6
30	22.5	53.82	180	60	42.91
55	22.5	45.2	124	75	50.82
40	30	53.84	100 *	100	58.81
170	30	35.99	120	100	54.13
250	35	34.02	54	101	70.05

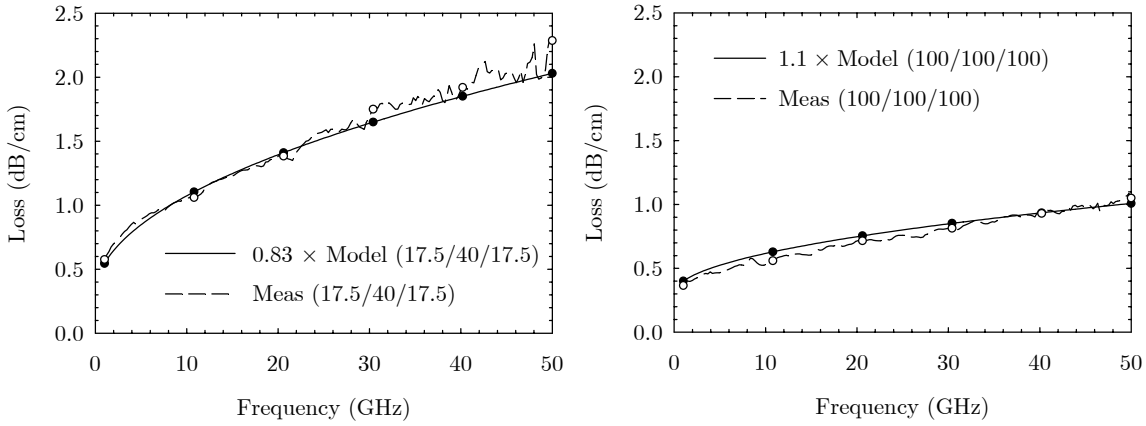


Figure A.5: Comparison between measured and modeled loss (dB/cm) data on a 425μm thick high resistive (ρ > 2000Ω-cm) silicon substrate, a) $W/S/W$=17.5/40/17.5, b) $W/S/W$=100/100/100.

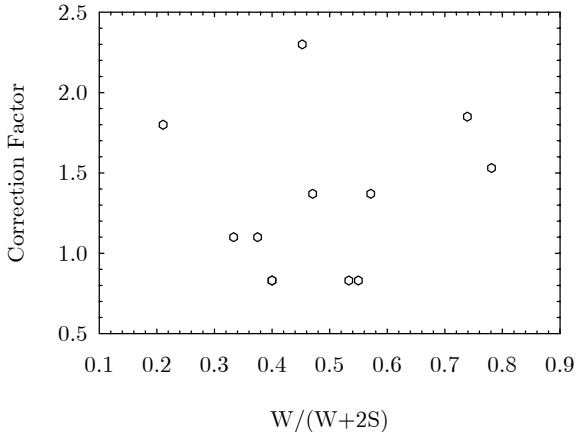


Figure A.6: Multiplication factor required to match the measured data on high resistive silicon substrate.

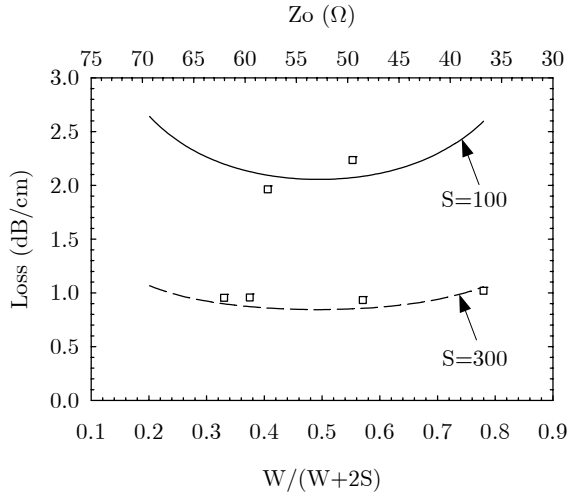


Figure A.7: Comparison between measured and predicted loss at 50GHz versus CPW pitch. The multiplication factor in Figure A.6 is used for the measured data.

APPENDIX B: DETAILED FABRICATION PROCESS

This appendix discusses the fabrication process used for the slow-wave MEMS phase shifter discussed in this chapter 3. The quartz substrate is 500μm thick, 2 inch square, and single-sided polished.

1. Wafer Cleaning:

(a) Immerse the wafer for 15-20 sec in 50:1 HF:H_2O with gentle agitation. This step is followed by 3 rinse cycles (∼3min) in de-ionized (DI) H_2O.
(b) Blow dry with N_2. Dehydrate bake on a 130°C hotplate for 4 minutes.

2. SiCr bias lines lift-off:

(a) Spin coat with NR-3000PY[(1)] photoresist (PR) at 3000 rpm for 40 sec.
(b) Soft bake on a 155°C hotplate for 1 min.
(c) Align a clear-field mask, exposing areas where the SiCr bias lines is to be lifted off.
(d) Expose at 13-14 mW/cm^2 for 17 sec.
(e) Pre-develop bake on a 110°C hotplate for 1min.
(f) Develop using RD-6[(2)] developer for 25 sec, rinse in DI H_2O for 1min and dry with N_2.
(g) Evaporate SiCr using E-beam evaporation to 1000-1500Å.
(h) Soak in RR4[(3)] PR remover at 110° with agitation for 5min in order to lift-off undesired metal, rinse in DI H_2O for 1min and dry with N_2.

3. Si_xN_y Ground Isolation Layer:

(a) Clean in a 200 mT O_2 Plasma at 100 W for 90 sec.
(b) Spin coat with NR-3000PY photoresist (PR) at 3000 rpm for 40 sec.

[(1),(2),(3)] NR-3000PY, RD-6, RR-4 is manufactured by Futurrex, Inc., Franklin, NJ.

(c) Soft bake on a 155°C hotplate for 1 min.

(d) Align a clear-field mask, exposing areas where the Si_xN_y areas is to be lifted off.

(e) Expose at 13-14 mW/cm^2 for 17 sec.

(f) Pre-develop bake on a 110°C hotplate for 1min.

(g) Develop using RD-6 developer for 25 sec, rinse in DI H_2O for 1min and dry with N_2.

(h) Sputter Si_xN_y using RF-magnetron at 3mT, 20SCCM Ar, and 225W RF power to 3000-4000Å.

(i) Soak in RR4 PR remover at 110° with agitation for 5min in order to lift-off undesired Si_xN_y, rinse in DI H_2O for 1min and dry with N_2.

(j) Alternatively, the after step (a) the Si_xN_y can be blanket deposited and etched subsequently using CF_4/O_2 plasma with the same light-field mask and a positive-tone PR (Shipley-1827). The etch recipe used in this work is listed in Table B.1.

Note: The Si_xN_y layer is not used in the 2nd generation slow-wave phase shifter designs.

Table B.1: Sputtered Si_xN_y etch recipe used in this work.

Si_xN_y Etch	
Gas (in SCCM)	CF_4:O_2 = 20: 2
Pressure	150mT
RF Power	150W
Time	17 min

4. CPW metal lift-off:

(a) Clean in a 200 mT O_2 Plasma at 100 W for 90 sec.

(b) Spin coat with NR-3000PY photoresist (PR) at 3000 rpm for 40 sec.

(c) Soft bake on a 155°C hotplate for 1 min.

(d) Align a clear-field mask, exposing areas where the CPW metal areas is to be lifted off.

(e) Expose at 13-14 mW/cm^2 for 17 sec.

(f) Pre-develop bake on a 110°C hotplate for 1min.

(g) Develop using RD-6 developer for 25 sec, rinse in DI H_2O for 1min and dry with N_2.

(h) Evaporate Cr/Au to ∼1μm thickness. Alternatively, a Cr/Ag/Cr/Au metallization stack can also be used with the 8000Å of Ag and 2000Å of Au. There was no noticeable difference in the insertion loss for the two cases up to 65GHz.

(i) Soak in RR4 PR remover at 110° with agitation for 5min in order to lift-off undesired Si_xN_y, rinse in DI H_2O for 1min and dry with N_2.

5. Sacrificial Layer Deposition:

(a) Clean in a 200 mT O_2 Plasma at 100 W for 90 sec.

(b) Spin coat adhesion promoter Hexamethyldisilazane (HMDS) at 1600-1700 rpm for 45 sec.

(c) Spin coat PMMA (950K, 9% in anisole solvent) at 1600-1700 rpm for 45 sec.

(d) Bake on a 180° hotplate for 90-120 sec.

(e) Flood evaporate 1500-2000Å of Ti.

(f) Spin coat HMDS at 3000 rpm for 30 sec.

(g) Spin coat with Shipley 1827 PR at 3000 rpm for 30 sec.

(h) Soft bake on a 105°C hotplate for 90 sec.

(i) Align a dark-field mask, exposing the pedestal areas.

(j) Expose at 13-14 mW/cm^2 for 22 sec.

(k) Develop in MF319 for 70 sec. Rinse in DI and dry with N_2.

(l) Etch Ti in 1:10 HF:DI for ∼7-10 sec. Rinse in DI and dry with N_2.

(m) Flood expose for 50 seconds at 13 mW/cm^2.

(n) Develop in MF319 for 70 sec. Rinse in DI and dry with N_2.

(o) Etch PMMA in 50 mT, 100 SCCM O_2 plasma 250W, for 12 minutes.

(p) Remove Ti in 1:10 HF:DI for 10 sec. Rinse in DI and dry with N_2.

5. MEM bridge fabrication and release:

(a) Evaporate Ti/Au 80/2000Å seed layer using E-beam evaporation.

(b) Spin coat with Shipley 1827 PR at 3000 rpm for 30 sec.

(c) Soft bake on a 105°C hotplate for 90 sec.

(d) Align a dark-field mask, exposing the areas to be electroplated that include pedestal, beam and CPW lines. Expose for 18 sec at 13-14mW/cm^2.

(e) Develop in MF319 for 60 sec. Rinse in DI and dry with N_2.

(f) Skip hard bake step. Electroplate Au using TG-25E[4] for 30min resulting in 1-1.2μm thick Au layer.

(g) Flood expose for 50 seconds at 13 mW/cm^2.

(h) Develop in MF319 for 60 sec. Rinse in DI and dry with N_2.

(i) Anneal on 105°C hotplate for 60 sec.

(j) Anneal on 120°C hotplate for 90 sec. Allow samples to reach room temperature.

(k) Spin coat with Shipley 1827 PR at 3000 rpm for 30 sec.

(l) Align mask and expose for 17 sec at 13-14mW/cm^2.

(m) Wet etch Au in gold etchant. The etch rate is approximately 28Å/s at 25°C.

(n) Etch Ti in 1:10 HF:DI for 6-8 sec. Rinse in DI and dry with N_2.

(o) Heat Shipley 1165 to 80°C. Soak the samples completely for 5min.

(p) Transfer to Shipley 1165 solution at 40C. Release MEM bridges overnight.

(q) Rinse in DI for 5 min.

(r) Transfer from DI to IPA and then to fresh IPA to remove all DI. Repeat this step twice.

(s) Transfer to methanol and then to fresh methanol. Repeat this process twice.

(t) Dry samples using Critical-Point-Drying (CPD) [46].

(u) If necessary, clean the samples in a 200 mT O_2 plasma at 100W for 3 min.

[4] TG-25E Au plating solution manufactured by Technic Inc., Cranston, Rhode Island.

APPENDIX C: TUNABLE BANDPASS FILTER USING DMTL

A 0.1dB Chebyshev prototype bandpass filter is designed on quartz using $\lambda/2$ shunt open stubs and $\lambda/4$ connecting lines (Figure C.1). The series and the shunt transmission lines are implemented using DMTL instead.

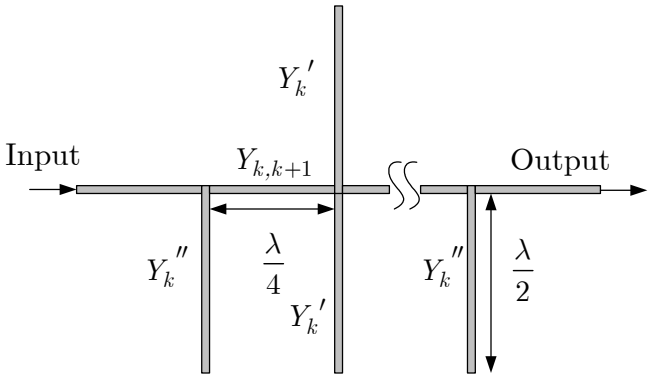


Figure C.1: Schematic of the tunable filter utilizing $\lambda/2$-open stubs and $\lambda/4$ series connecting sections [36].

The design is carried out first to give $\lambda/4$ length for series and shunt short circuit stub sections for a desired pass-band characteristic and bandwidth from the low-pass to band-pass transformation [58]. Then each shunt, quarter-wave length short-circuited stub of characteristic admittance (Y_k) is replaced by a shunt, $\lambda/2$ open-circuited stub having a impedance (Y_k') given by:

$$Y_k' = \frac{Y_k\left(a\,tan^2\,\theta_1 - 1\right)}{(a+1)\,tan^2\,\theta_1} \tag{5.1}$$

$$a = cot^2\left(\frac{\pi\omega_\infty}{2\omega_0}\right) \tag{5.2}$$

$$Y_{k,k+1} = Y_A\left(\frac{J_{k,k+1}}{Y_A}\right) \tag{5.3}$$

Where, $\theta_1 = \pi\omega_1/2\omega_0$, and ω_1/ω_0 is the bandwidth and ω_∞ is the frequency at which the shunt lines present short circuits to the main line and cause ∞ attenuation. In this work, the value of $Y_k'' = Y_k'$.

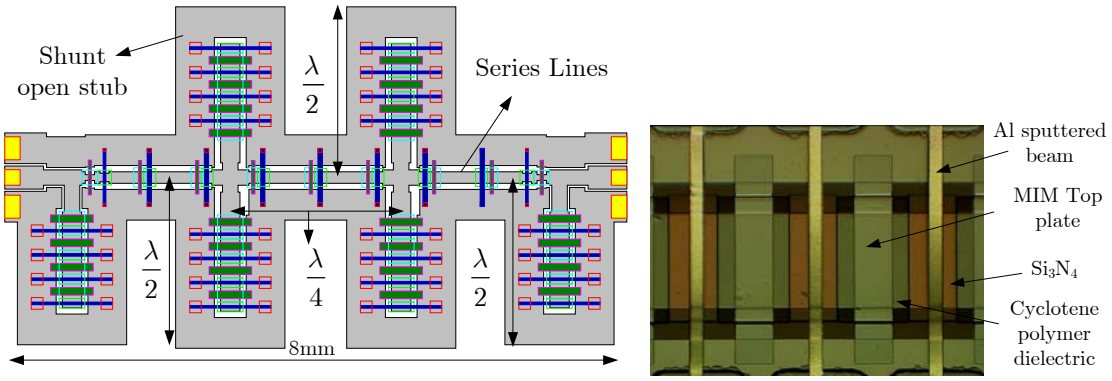
The bandpass filter presented herein consists of nine reactive elements: six open stubs that are $\lambda/2$ long and three series $\lambda/4$ long connecting lines between the open stubs (Figure C.2). The open stub design is preferred over a short end $\lambda/4$ stub design because it is easier to DC bias the circuit using coaxial bias tees. The series connecting sections (unloaded Z_o~80Ω) are periodically loaded with three shunt capacitors, each spaced by 850μm . The shunt $\lambda/2$ stubs (unloaded Z_o~70Ω) utilize four capacitors with a separation of 350μm . The beams used for the capacitors in the series and shunt sections are approximately 755μm and 970μm long, respectively; the beam width is held constant at 35μm. The overall footprint of the filter is 8mm×4.7mm and a total of 33 capacitive bridges are used. The widths of the center conductor and the slot for the feed are 300μm and 30μm, respectively.

The series DMTL section is required to be approximately $\lambda/4$ long at each design center frequency. For an unloaded line on quartz, the corresponding lengths would be 2220μm at 22GHz and (2200+741=) 2961μm at 16.5GHz. The phase shift required to emulate the additional length of 741μm at 16.5GHz is found to be approximately 20°. The required phase shift ($\Delta\phi$) as a function of the CPW line characteristic impedance can be calculated using equations presented in chapter 2 [22].

Three capacitive bridges separated by 850μm provide the necessary variation in characteristic impedance and result in a 90° phase shift at each of the desired frequencies (22GHz when MEM bridge in the up-state and 16.5GHz when MEM bridge in the down-state). The upstate and the downstate values of each MEMS capacitor are approximately 0.07pF and 0.1pF, respectively.

The shunt open stubs are $\lambda/2$ long at each design center frequency (5942μm at 16.5GHz; 4456μm at 22GHz). The length difference translates to a 44° phase difference at 16.5GHz. In this case, four capacitive bridges separated by 350μm are used. The upstate and the downstate capacitance for these capacitors are approximately 0.2 and 0.4pF, respectively. The higher capacitance values, relative to those used in the series sections, are used for two

reasons: to reduce the size of the filter by increasing the loading, and to reduce the number of required bridges. It was also found that the increased distributed loading yields a better response than that obtained with a comparable design using shunt stubs that are terminated in large, single capacitors for length reduction.



(a) (b)

Figure C.2: Schematic of the tunable filter designed with DMTL.

Table C.1 gives the capacitance values for the series and shunt sections. In order to design low capacitance ratios that are feasible to fabricate, MIM capacitors are used in series with the MEM bridges [59]. The MIM capacitors are placed 40-50μm away from each MEMS capacitor (Figure C.2(b)).

Table C.1: Capacitance values for the series $\lambda/4$ sections and the open $\lambda/2$ stubs in the upstate and downstate.

	C_{up} [pF]	C_{down} [pF]
Series $\lambda/4$ sections	0.07	0.1
Shunt $\lambda/2$ sections	0.2	0.4

The starting values for the admittances of the shunt stubs were calculated using equations given in [8]. The final values of the admittances were found by circuit level simulation, after accounting for parasitics extracted via numerical EM simulation. Full-wave simulations were performed using ADS Momentum™. The parasitic effects due to the cross and the tee-junction discontinuities required the length of the shunt and series sections to be adjusted.

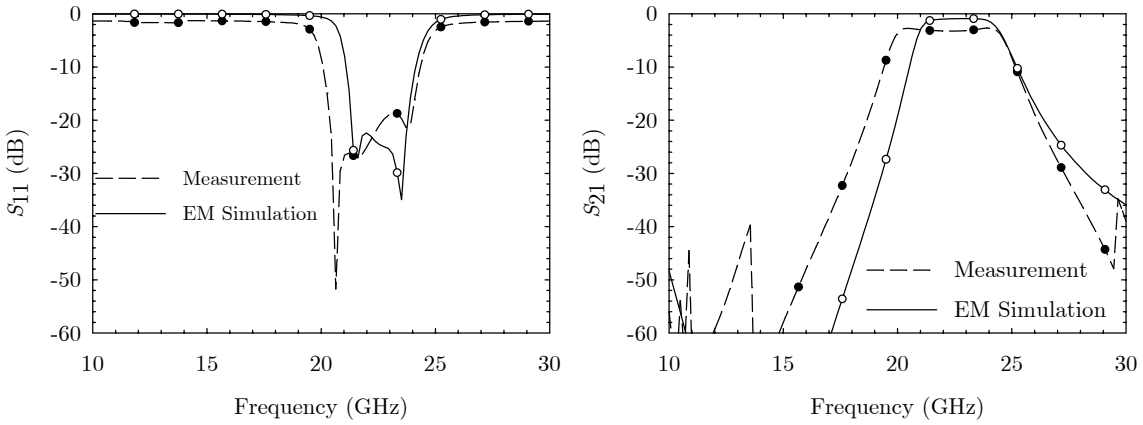
The filter is fabricated on a 480μm thick quartz substrate (ε_r=3.78, tanδ=0.0004). The fabrication steps are as follows:

- A 0.5um thick Si_3N_4 is blanket deposited using RF magnetron sputtering to improve the adhesion of metal lines on the quartz. Alternatively, a thin Cr layer can be used but this approach requires etching in subsequent fabrication steps.
- Lift–off processing is used to define metal lines to a thickness of 1μm (Cr/Ag/Cr).
- A 3μm thick photosensitive cyclotene™ polymer (ε_r=2.7) is used to form a MIM capacitor dielectric layer.
- A 0.5μm thick Si_3N_4 is deposited using RF magnetron sputtering.
- Contact pads (0.2μm thick) comprised of Cr/Au are formed using liftoff processing for RF probing.
- Pedestal areas are patterned with photoresist and the 3μm thick cyclotene™ polymer is used to form the posts.
- A 0.8μm thick Al layer is sputtered on top the sacrificial photoresist layer and subsequently etched to form the capacitor beam geometry.
- The sacrificial photoresist is removed and critical point drying is used to release the MEMS capacitors.

Measurements were performed from 10–30GHz using a Wiltron 360B VNA and 250μm pitch GGB microwave probes. A Thru–Reflect–Line (TRL) calibration was performed using calibration standards fabricated on the wafer. A high voltage bias tee was used to supply voltage through the RF probe to avoid damaging the VNA test ports. Typical actuation voltage of the beams is approximately 45-50V. This is because the Al sputtered beam after release had some amount of tensile stress and buckle up by a factor of 0.3-0.5μm (10-16% of 3μm height). Further optimization of process parameter to make the bridge flat was not attempted since the sputtering chamber was not available for metal deposition.

Figure C.3 shows the comparison between the measured and simulated filter response in the upstate. The measured response has S_{11} < -19dB and a maximum S_{21} of -3.3dB in the pass-

band. The relative bandwidth of the filter in the upstate is approximately 16.5% (20.4-24GHz) and the out of band rejection is better than 25dB over the measured frequency range. The measured data shows a larger bandwidth and higher insertion loss when compared to the simulation results. The increased bandwidth is attributed to fabrication tolerance, resulting in a higher capacitance of the MEM bridges. The higher insertion loss is due to the resistance of the bridges (not accounted for in the simulations).



(a) (b)

Figure C.3: Comparison between measured data and modeled data in the up-state, a) S_{11}, b) S_{21}. Solid lines represent EM simulation data and dashed lines represent measured data.

Figure C.4 shows the comparison between the measured and simulated data in the downstate. The measured S_{11} is less than -30dB and S_{21} is approximately -2.3dB in the pass-band (15.7-17.8GHz). The measured and the modeled filter results exhibit a spurious response above 25GHz that is associated with the $2\omega_0$ pass-band characteristic. The relative bandwidth of the filter is approximately 11.5%. The absolute bandwidth in the upstate and downstate is approximately 3.6GHz and 2.8GHz, respectively.

In order to maintain absolute bandwidth in both the states, independent β- and Z_o-tuning of the $\lambda/2$ and $\lambda/4$ section is required. However, DMTL implementation such as shown herein, can provide only β-tuning with dependent Z_o levels. Therefore, maintaining absolute bandwidth between tunable states becomes difficult. However, the slow-wave unit cell

configured in a manner similar to the tunable MEMS transmission (see chapter 4) can be used in the filter design resulting in constant bandwidth between tuned states.

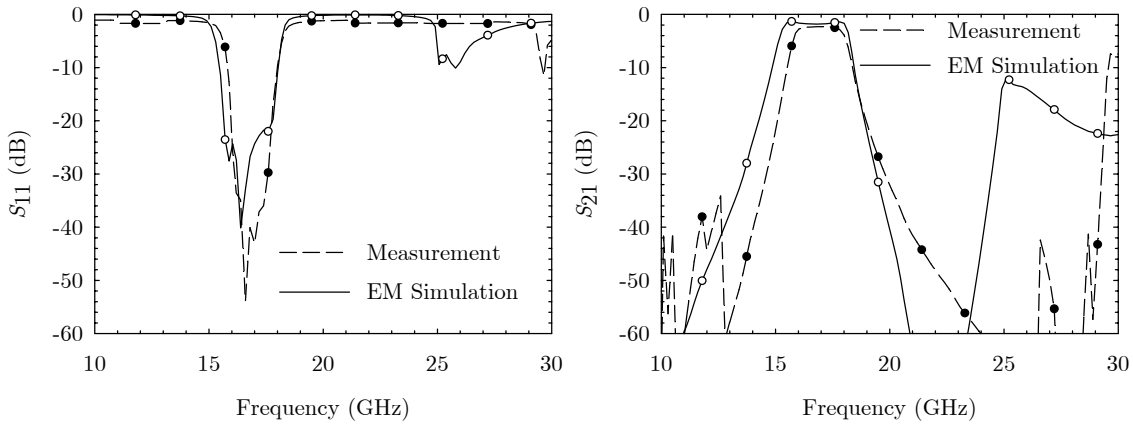


Figure C.4: Comparison between measured data and modeled data in the down-state, a) S_{11}, b) S_{21}. Solid lines represent EM simulation data and dashed lines represent measured data.

In order to maintain absolute bandwidth in both the states, independent β- and Z_o-tuning of the $\lambda/2$ and $\lambda/4$ section is required. However, DMTL implementation such as shown herein, can provide only β-tuning with dependent Z_o levels. Therefore, maintaining absolute bandwidth between tunable states becomes difficult. However, the slow-wave unit cell configured in a manner similar to the tunable MEMS transmission (see chapter 4) can be used in the filter design resulting in constant bandwidth between tuned states.

ABOUT THE AUTHOR

Balaji Lakshminarayanan received his BS and MS degrees in 1995 and 1999 respectively. His research interests are in the area of RF-MEMS techniques for microwaves, application of micromachining for mm-wave circuits, and electromagnetic modeling of VLSI and microwave circuits.