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Modeling and Optimization of Time Delay Unit Network Architectures for Reducing Complexity of Ultra- Wideband Phased Antenna Arrays

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Modeling and Optimization of Time Delay Unit Network Architectures for Reducing Complexity of Ultra- Wideband Phased Antenna Arrays

by

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Dedication

To my wife, daughters, parents, grandparents, and siblings.

Acknowledgments

First, I would like to thank my incredible wife, Tori, for her unconditional love, gracious support, and tremendous amount of patience throughout this rather lengthy process, without which this endeavor would not have been possible. I want to thank my daughters, Shiloh and Galilee, who are too young to even understand how much their love and approval motivates me to accomplish more than I thought possible. I would also like to thank my parents and siblings who have always been a source of encouragement in those moments I second guess myself and always keep me grounded. I am also very thankful for my colleague and dear friend, Dylan McQuaide, who not only provided countless hours in discussion and review, but also challenged and encouraged me to push beyond simply good enough; this contribution cannot be overstated.

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List of Acronyms

Acronym	Definition
PAA	Phased Antenna Array
TDU	Time Delay Unit
TTD	True Time Delay
TDU-A	Time Delay Unit Architecture
VSWR	Voltage Standing Wave Ratio
RL	Return Loss
ILP	Integer Linear Programming
RF	Radio Frequency
LSB	Least Significant Bit
MSB	Most Significant Bit
RMS	Root Mean Squared

Abstract

This dissertation presents a systematic technique for modeling and optimization of the hierarchical time delay unit (TDU) architectures of ultra-wideband (UWB) phased antenna arrays (PAAs). The first major contribution of this dissertation is the optimization of a linear PAA by casting the problem in the standard form of integer linear programming (ILP) optimization with an objective function that targets minimizing the total number of TDUs within the RF feed network fanout while maintaining phase error and manufacturability constraints. This optimization can significantly reduce the cost, power, and complexity of UWB PAAs in contrast to prior methods that iteratively converge on a manufacturable hierarchical architecture without considering the total number of TDUs. Three linear PAA optimization examples are presented with a requirement of less than 5° phase error. These examples clearly show that there are many TDU architectures (TDU-A) that can satisfy this phase error requirement, yet only one TDU-A is superior by exhibiting the minimum number of TDUs. If the presented optimization method is omitted, the superior TDU-A is highly likely to be missed because traditional iteration based design approach almost always places the TDUs as close as possible to the antenna elements within the RF feed network fanout. On the other hand, the superior TDU-A is shown to exhibit TDUs starting from much lower levels (i.e., farther away from the antenna elements) of the RF feed network fanout.

The second contribution of this dissertation is the investigation of practical implementations for UWB PAAs. Specifically, the method is considered for linear UWB PAAs and their feed networks which include non-idealities when practical implementations of their circuit components are pursued. These non-idealities are shown to cause additional time delay

errors that must be modeled within optimization to achieve the best performance from the UWB PAA. For the considered practical implementation, these delay errors are induced by frequency dependent variations in power divider isolation and load mismatch, component VSWRs, and dispersion. By properly modeling these errors in the TDU-A optimization leads to a TDU-A that has the necessary delay range required to steer the beam towards the desired wide scan angles. For experimental verification, a 16 element linear PAA TDU-A is optimized for operating from 5-30 GHz by modeling the non-idealities of the feed network that is implemented to steer the beams towards boresight, 25°, and 50°. Simulation and measured performances demonstrate the UWB operation with stable radiation patterns. Most importantly, it is shown that the physical realizations of the UWB PAAs fed with TDU-As that are optimized by accounting the non-idealities of the feed network components can be calibrated for achieving the desired scan performance.

The third contribution of this dissertation is a calibration demonstration of a 16 element linear UWB PAA as a study case. Calibration of its optimized TDU-A implementation is shown to excite each antenna element within the quantized time delay error bound. The calibration study presented assumes an instantaneous bandwidth (IBW) of 1 GHz for the UWB PAA operating from 5 to 30 GHz. It is demonstrated that variation in side lobe level (SLL) when compared to the ideal is imperceptible below -26 dB after calibration.

The final contribution of this dissertation is the expansion of the optimization to general 2D rectangular PAAs. It is shown that more than one optimal solution exists which eliminate the ability to use ILP. Therefore, a new algorithm is developed to locate an optimal architecture and two examples are presented with an objective of less than 5° phase error. The examples clearly demonstrate that many TDU-A variants satisfy the performance requirement but very few TDU-A variants achieves performance while significantly minimizing TDU and bit count.

Chapter 1: Introduction

There are two technologies used to steer a phased antenna array (PAA) beam: phase shifters (PS) and time delay units (TDU). The ideal PS provides constant phase over frequency which causes beamsquint; however, a PS is generally low loss and physically small. On the other hand, the ideal TDU delivers constant true time delay (TTD) which provides a stable beam by eliminating beamsquint; however, a TDU is higher in loss, physically large, and complicated to implement [1-6]. For this reason, PS are commonly used in PAAs which can tolerate or ignore beamsquint over the system bandwidth. In general, beamsquint increases with system bandwidth when PS are employed. Systems with advanced performance, such as higher data rates in a satellite communications link or finer resolution in a radar system, require broader bandwidths which necessitates the use of TDUs [7-29]. Traditionally, the entirety of the required delay is placed adjacent to each antenna element in broadband systems, however PAAs with a high number of antenna elements leads to TDUs that are too lossy and physically large to place behind each antenna element without significantly degrading performance, size, weight, and power consumption. This degradation is mitigated by forming hierarchical TDU networks within the RF-fanout [4-5,30-33].

1.1 Motivation and Research Focus

The process of forming a hierarchical TDU architecture (TDU-A) is generally iterative as the architect balances performance and manufacturability as shown in [3] and implied in [4]. Larger PAAs need TDUs with longer time delays and more bits to maintain the required maximum scan angle. However, allowances in manufacturing and other constraints, such as the physical line

length of the transmission lines and high loss associated with long delay lines, can make such TDUs impractical to be employed under each antenna element of the PAA [9-12]. Hence, designers pursue a multi-layered RF-fanout approach where TDUs with fewer total number of bits and different least significant bits (*lsbs*) are placed at different division levels. Complexity of designing TDU architecture grows exponentially with increased antenna elements, division levels, bits, and layers [4]. The location of the TDUs within the RF-fanout varies the cost, power, and complexity of the PAA leading to a trade of economy [12] since each TDU has a cost, power consuming amplifier, and requires multiple control/bias lines [11]. Hence, the optimal solution to the TDU-A is the one which minimizes the TDU count while maintaining performance requirements and manufacturability. The traditional techniques for determining the location of the TDU layers within the RF-fanout division levels do not take the entirety of these trade-offs into consideration. For example, reference [4] employs an iterative approach whereby longer time delay bits are transferred from one division level to the previous while the changes in performance, such as side lobe level, are observed. This becomes necessary because large values of time delay lead to long transmission lines which may exceed a size that is manufacturable within available board/circuit space. Consequently, there may be a physical constraint on the TDU's most significant bit (*msb*) at each level of division which becomes more stringent with each division level. The available physical space for wide scanning arrays is typically half-wavelength of f_{high} at the highest division level that is directly under the antenna elements. The goal in [4] is to ensure that the design meets specification (such as a maximum phase error across all antenna elements) with an architecture that is manufacturable. However, this does not guarantee the usage of the minimum number of TDUs, which would attain the lowest complexity. For instance, in the case of a 256×256 element PAA with 3 TDU layers, there are 15,000 architecture variants when TDUs are allowed to exhibit

2 to 5 bits. Only one of these architectures provides the minimum TDU and bit counts while meeting the defined phase error specification. Following the traditional method of moving bits backwards a single layer at a time [4], one may have found that architecture variant 738 meets the requirement with the 3 TDU layers distributed amongst the highest 3 division levels closest to the antenna elements. This would lead to an RMS phase error that is 4.8°, which satisfies the constraints; however, this architecture has 16368 more TDUs compared the optimal architecture, which is an increase of 23.5%, as will be shown in Chapter 2.

Other methods of optimizing the modularization of subarrays based on sum and difference methods have been presented [34-36] which focus on optimizing the architecture by achieving minimal differences between the modularized array pattern and the ideal pattern. Although these methods will also generally converge to an architecture solution that meets the required pattern performance, they do not consider the economy trade. Hence, there is no guarantee that the lowest possible TDU and bit count is employed within the TDU architecture.

1.2 Contributions

Chapter 2 investigates the feasibility of a new method for locating the optimal TDU architecture in a linear PAA with a set of constraints in manufacturability and performance by using integer linear programming [47]. Linear programming has been demonstrated in beamforming algorithms [37] and circuit simulation problems [38-40]; however, it has not been applied to PAA TDU architectures until now. The presented method can be scaled to various array sizes, as demonstrated in Section 2.5 and 2.6, and broadened to include additional constraints. Section 2.2 and 2.4 present the method by detailing the process through an example 8 element linear PAA with a maximum of 5° phase error. Section 2.5 and 2.6 provide more compelling examples with a 128 element linear PAA and a 256×256 element PAA. It is verified through

simulation that a significant reduction in TDU count is achievable while performance goals are maintained.

Despite the comprehensiveness of Chapter 2, the optimization model introduced focuses on ideal implementations of feed networks such as with the assumptions of perfectly matched and isolated power dividers with ideal transmission lines. This also seems to be the approach taken in the existing literature. Even though different approaches for designing TDU-As are presented [1, 4-5], literature does not provide a consideration of the impact of non-ideal responses of the circuit components that form the TDU-A in its practical implementation. In practice, the designs of the circuit components within a TDU-A are typically carried out independently by different engineers in a way to meet a set of requirements imposed by the TDU-A system architect. Although these requirements can be strict, they are far from being ideal (e.g., return loss (RL) >15 dB vs RL >∞ across the UWB). The major circuit components in the TDU-A example in Chapter 2 are the 2-way power dividers, TDUs, and antennas. The non-idealities in the network responses of these components and their frequency dependent variation lead to time delay errors. Therefore, it is of interest to account for these non-idealities in the optimization model shown in Chapter 2. If these errors are left unaccounted for, antenna pattern degradations that cannot be resolved with PAA calibration occur due to the unavailibility of required delay lengths within TDUs which is especially pronounced at the wider scan angles.

Chapter 3 investigates the delay error effects and offers three contributions to this dissertation. The first is the transfer equation derivation through signal flow diagram of key componts within the physical TDU-A implementation and relating the transfer equation into time domain in order to account for delay ripple when ports of the components are not terminated with idealistic perfectly matched impedances. The second is to incorporate these non-idealities (i.e.

delay ripples) within the optimization model of Chapter 2 to obtain the optimal TDU-A. The final contribution is the first experimental demonstration of the TDU-A designed based on the optimization results and thereby closing the modeled to measured loop. The demonstration TDU-A is designed for an $M = 16$ element linear PAA consisting of Vivaldi antenna elements operating from 5 GHz to 30 GHz. By using fixed length delay lines to represent the TDU states within the TDU-A, three feed networks and PAAs are designed and fabricated to investigate the performance of radiation patterns steered towards 0°, 25°, and 50° scan angles. It is important to note that, although the manuscript considers stationary beam steering for the ease of implementation, the optimizaton method is directly applicable to the electrically steered PAAs that incorporate controled TDU devices.

Chapter 4 demonstrates that the TDU-A optimized in Chapter 3 can be calibrated to obtain the desired radiation patten from the UWB PAA. The 16-element linear PAA is considered as a case study for 5-30 GHz operation. Optimal TDU-A is found in Chapter 3 for the desired ±50° scan range and the feed network is configured for 25° scan with stationary delay lines (but with varying with discrete delay lengths to mimic a realistic reconfigurable implementation). The feed network is full wave simulated to obtain the PAA phase excitations. The operation is repeated for a calibrated feed network to demonstrate side lobe level (SLL) performance of the PAA remains within optimization constraints.

Finally, Chapter 5 extends the method outlined in Chapter 2 and presents a method for optimizing TDU-As of general rectangular PAAs defined as M elements in the x-direction and N elements the y-direction where M and N are integers. Accomplishing this requires us to revisit and revise the algorithm and key equations from Chapter 2. Throughout sections 5.2-5.4 a 10×6 element PAA TDU-A example is used to demonstrate the development of the matrices which keep

track of the TDU-A variant configurations, the performance vector which keeps track of the performance of each TDU-A variant configuration, as well as the formulation of the optimization problem. Section 5.5 presents a more compelling 256×120 element array example to validate the use of the proposed method. In each case, it is shown that the number of TDUs is minimized while achieving the performance criteria.

Chapter 6 provides a summary of the accomplishments presented in this dissertation and outlines several opportunities for future work in TDU-A optimization.

Chapter 2: Time Delay Unit Architecture Optimization for Linear Phased Antenna Arrays Using Integer Linear Programming[1]

Time delay units are comprised of individual true-time delay bits that alternate between a reference path and a delay path as shown in Fig. 2.1. The least significant bit (*lsb*, Bit 1) provides the smallest possible time delay change (τ_1) and it is determined based on the required phase error in beam steering at the highest operation frequency. The higher order bits provide time delay variations in multiples of the *lsb* (i.e., Bit 2 $\tau_2 = 2\tau_1$, Bit 3 $\tau_3 = 2^2\tau_1$,…, Bit n $\tau_n = 2^{n-1}\tau_1$). In the classical scenario where TDUs are placed adjacent to the antenna elements, the total number of bits (n) required is determined based on the required total time delay due to the PAA size, desired scan angle, and bandwidth. A TDU will generally include transmission lines, switches, and an amplifier to compensate the losses. A large number of DC lines that deliver bias and control will be needed in PAA implementation to achieve the electronic control and operation.

Larger PAAs need TDUs with longer time delays and more bits to maintain the required maximum scan angle. However, allowances in manufacturing and other constraints, such as the physical line length of the transmission lines and high loss associated with long delay lines, can make such TDUs impractical to be employed under each antenna element of the PAA [8-11]. Hence, designers pursue a multi-layered RF-fanout approach where TDUs with fewer total number of bits and different *lsb*s are placed at different division levels. Fig. 2.2 shows a three-division level RF-fanout for an 8-element antenna array, where TDUs can be placed at each level with different *lsb*s and n. Complexity of designing this *TDU architecture* (TDU-A) grows exponentially

[1]Portions of this chapter have been previously published in the IEEE Transactions on Antenna and Propagation [47] and have been reproduced with permission from IEEE.

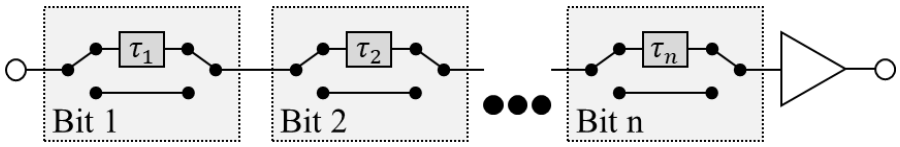

Figure 2.1 A TDU with n bits each with τ_n of delay and an amplifier.

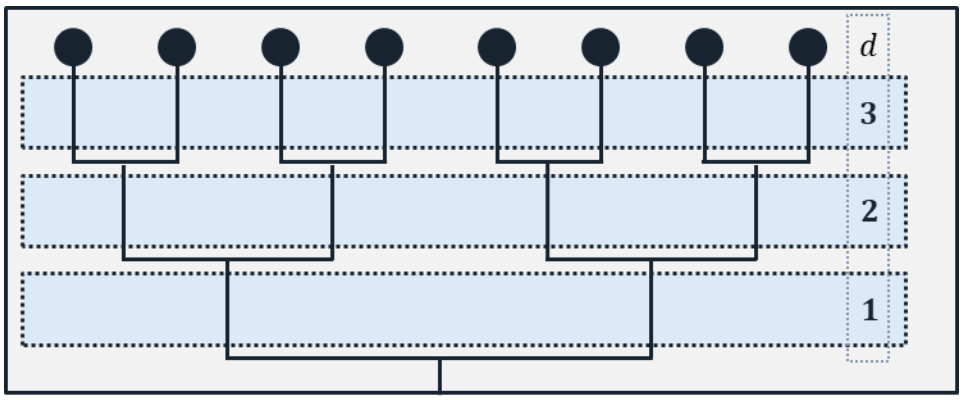

Figure 2.2 Three division level RF-fanout of an 8 element linear array, where TDU bits can potentially be placed in each division level with different combinations.

with an increased number of antenna elements, division levels, bits, and layers [4]. The location of the TDUs within the RF-fanout varies the cost, power, and complexity of the PAA leading to a trade of economy [30] since each TDU has a cost, power consuming amplifier, and multiple control/bias lines [33]. Hence, the optimal solution to the TDU architecture is the one which minimizes the TDU count while maintaining performance requirements and manufacturability.

This Chapter investigates the feasibility of a new method for locating the optimal TDU architecture with a set of constraints in manufacturability and performance by using integer linear programming (ILP). The presented method can be scaled to various linear array sizes, as demonstrated in Sections 2.5 and 2.6, and broadened to include additional constraints. Sections 2.2-2.4 present the method by detailing the process through an example 8 element linear PAA with

a maximum of 5° phase error. Section 2.5 and 2.6 provide more compelling examples with a 128 element linear PAA and a 256×256 element PAA.

2.1 TDU Architecture Variants of a Linear PAA

We first calculate the number of TDU architecture variants, which in turn sets the total quantity of variables in the optimization. The TDU architecture variants represent all the different permutations of TDU locations in the RF-fanout. If we assume 2-way divisions for a linear array of M elements where M is a power of 2, the number of division levels is

$$D = \log_2(M) \tag{2.1}$$

For the 8 element linear array example (see Fig. 2.2) $D = 3$. In Fig. 2.2, d $(1, 2, \dots, D)$ represents the division levels of the PAA. Each division level can have no TDUs (i.e., $T_d = 0$), a single layer of TDUs (i.e., $T_d = 1$) or cascaded layers of TDUs (i.e., $T_d = 2, 3, \dots L$) where L denotes the total number of TDU layers that will be employed within the RF-fanout. A layer of TDUs, TDU_l ($l = 1, .., L$), consists of identical TDUs placed at each branch in the division level of an RF-fanout. Placement of these TDU layers create different architecture variants. To illustrate this, Fig. 2.2 shows two unique architecture variants for the 8-element PAA with $D = 3$ when $L = 2$ TDU layers are employed. In Fig. 2.3, TDU_1 consists of $b_1 = 4$ bit TDUs placed in $d = 1$ level and TDU_2 consists of $b_2 = 5$ bit TDUs placed in $d = 3$ level. Placement in Fig. 2.3 implies $T_1 = 1, T_2 = 0$, and $T_3 = 1$. In Fig. 2.4, TDU_1 and TDU_2 are in $d = 1$ and $d = 2$ levels, respectively. For Fig. 2.4 variant $T_1 = 1, T_2 = 1$, and $T_3 = 0$. The total number of architecture variants (V_{DL}) due to the placement of TDU layers within division levels of the RF-fanout can be calculated with

$$V_{DL} = \frac{(L+1)^{\overline{(D-1)}}}{(D-1)!} \tag{2.2}$$

where L is the total number of TDU layers in the RF-chain and the notation $x^{\overline{n}}$ denotes a rising

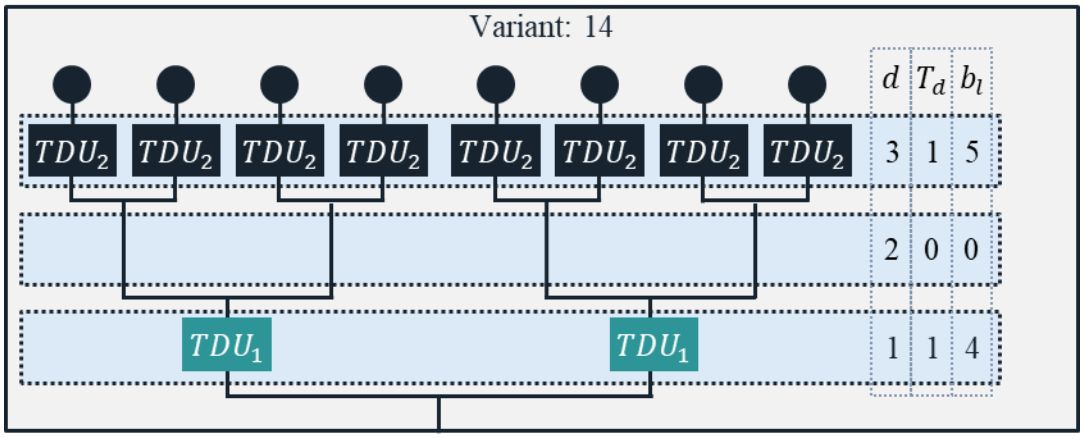

Figure 2.3 Architecture variant example for a $D = 3$ division level 8 element PAA with a 5 bit TDU layer in $d = 3$ and a 4 bit TDU layer in $d = 1$ with no TDU in $d = 2$.

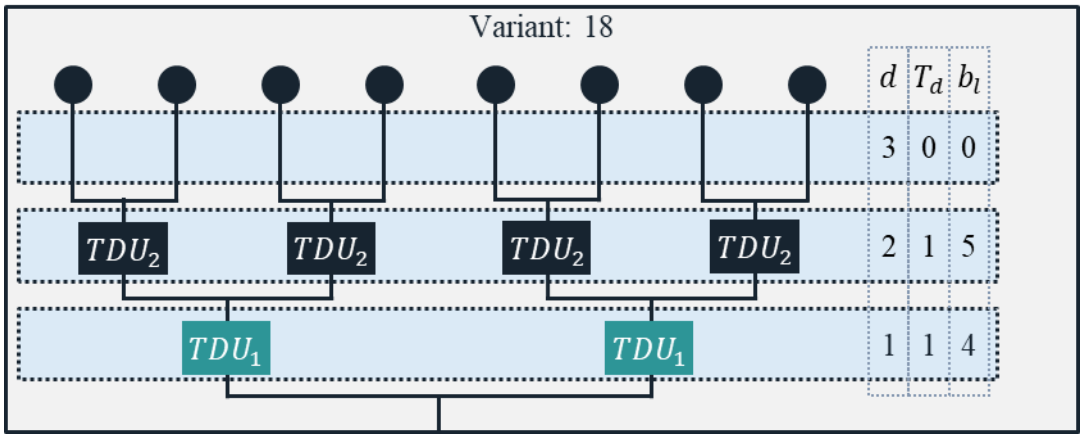

Figure 2.4 Architecture variant example for a $D = 3$ division level 8 element PAA with a 5 bit TDU layer in $d = 2$ and a 4 bit TDU layer in $d = 1$ with no TDUs in $d = 3$.

factorial where $x^{\bar{n}} = x(x+1) \ldots (x+n-1)$. For Fig. 2.2, $L = 2$ and $D = 3$ lead to $V_{DL} = 6$. Equation (2.2) grows exponentially with number of layers and division level.

The number of bits used for implementing the TDUs adds additional complexity to the number of architecture variants. The parameter b_l $(l = 1, .., L)$ represents the number of bits used in implementing TDU_l. Since minimizing the bit counts is important, flexibility in bit counts

Table 2.1 Variant matrix ($\boldsymbol{\Psi}$) of the 8 element PAA

v	T_1	T_2	T_3	b_1	b_2
1	0	0	2	4	4
2	0	0	2	4	5
3	0	0	2	5	4
4	0	0	2	5	5
5	0	1	1	4	4
6	0	1	1	4	5
7	0	1	1	5	4
8	0	1	1	5	5
9	0	2	0	4	4
10	0	2	0	4	5
11	0	2	0	5	4
12	0	2	0	5	5

v	T_1	T_2	T_3	b_1	b_2
13	1	0	1	4	4
14	1	0	1	4	5
15	1	0	1	5	4
16	1	0	1	5	5
17	1	1	0	4	4
18	1	1	0	4	5
19	1	1	0	5	4
20	1	1	0	5	5
21	2	0	0	4	4
22	2	0	0	4	5
23	2	0	0	5	4
24	2	0	0	5	5

should be provided during optimization. To do so, we set $b_l \in [b_{min}, b_{max}]$ where b_{min} and b_{max} represent the minimum and maximum number of bits allowed in the architecture, respectively. For simplicity, let us set $b_{max} = 5$ and $b_{min} = 4$ for the 8 element PAA example. Consequently, the architecture variants due to the allowable bits (V_{AB}) in the TDUs becomes

$$V_{AB} = (b_{max} - b_{min} + 1)^L . \tag{2.3}$$

For the 8 element PAA, $V_{AB} = 4$. The total number of variants due to the contributors of equations (2.2) and (2.3) is

$$V = V_{DL} V_{AB}. \tag{2.4}$$

Therefore, with the choices made, the RF-fanout of the 8 element PAA can support $V = 24$ architecture variants.

We proceed by organizing the architecture variants in a matrix $\boldsymbol{\Psi}$. The variant matrix of the 8 element PAA discussed so far is shown in Table 2.1. Each row v represents an architecture variant. The first D columns represent the number of TDU layers on the d^{th} level of division (i.e., T_d). The last L colums represent the bit counts of TDU_l (i.e., b_l). The division level of TDU_l

belonging to variant v is stored in a separate matrix exhibiting column values of d_l. The architecture variants shown in Fig. 2.2 correspond to the rows 14 and 18 of the matrix. In each row of the matrix, the sum of the numbers in the first d columns is 2 because $L = 2$. This constraint in generating the variant matrix and can be written as

$$\sum_{d=1}^{D} \boldsymbol{\Psi}_{v,d} = L, \quad v = 1, 2, \dots V \tag{2.5}$$

Algorithm 2.1 is used to generate the variant matrix for the 8-element PAA. The parameters of the algorithm $(T_d, L, D, b_{min}, b_{max})$ and size of the matrix $\boldsymbol{\Psi}_{V\times(D+L)}$ can be scaled up to generate the variant matrix for representing all TDU architecture variants of any size linear PAA with a total number of elements that is a power of 2.

Algorithm 2.1 Generation of Variant Matrix

$v = 1$; $T_1 = T_2 = T_{d=D=3} = 0$;
for $T_1 \le L$; for $T_2 \le L$; for $T_{d=D=3} \le L$;
    for $b_{min} \le b_1 \le b_{max}$; for $b_{min} \le b_{l=L=2} \le b_{max}$;
        if $T_1 + T_2 + T_{d=D=3} = L$;
            $\boldsymbol{\Psi}(v, :) = [T_1, T_2, T_{d=D=3}, b_1, b_{l=L=2}]$;
            $v = v + 1$;
end; end; end; end; end;

Next, we define a branch in the RF-fanout as an interconnect between a divider output at division level d and divider input at the next division level $d + 1$. At $d = D$, the branches are connected to the antennas. A vector that represents the number of branches on each level of division can be created as

$$\boldsymbol{m} = [2^1 \quad 2^2 \quad \dots \quad 2^D]^T. \tag{2.6}$$

By representing the columns of the $\boldsymbol{\Psi}$ as

$$\boldsymbol{\Psi} = [\boldsymbol{\psi}_1, \boldsymbol{\psi}_2, \dots, \boldsymbol{\psi}_D, \boldsymbol{\psi}_{D+1}, \dots, \boldsymbol{\psi}_{D+L}] \tag{2.7}$$

and by multiplying the first D columns of $\boldsymbol{\Psi}$ with $\boldsymbol{m}$ as

$$\boldsymbol{\eta}_{TDU} = [\boldsymbol{\psi}_1, \dots, \boldsymbol{\psi}_D]\boldsymbol{m} \tag{2.8}$$

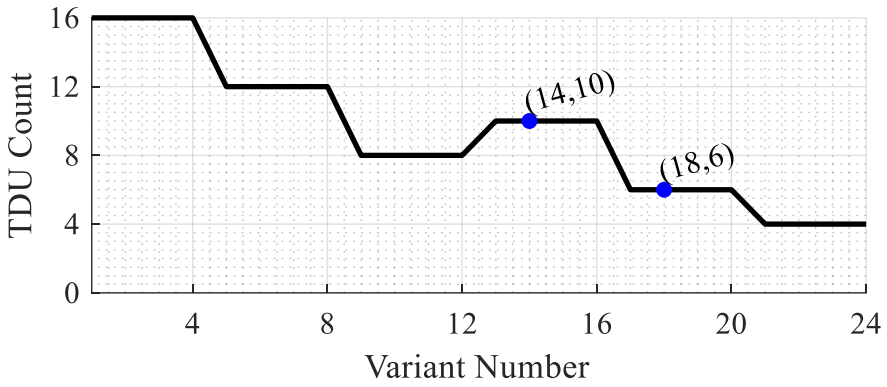

Figure 2.5 TDU count vs variant number of the 8 element PAA. Data points correspond to variants shown in Figs. 2.3 and 2.4.

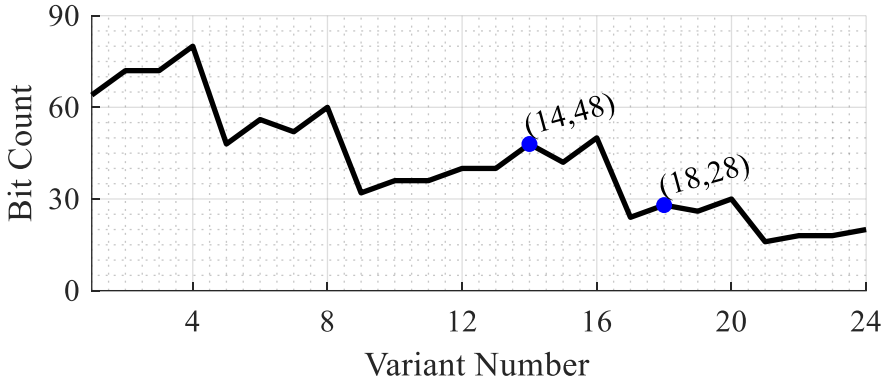

Figure 2.6 TDU bit count vs variant number of the 8 element PAA. Data points correspond to variants shown in Figs. 2.3 and 2.4.

we obtain the $\boldsymbol{\eta}_{TDU}$ vector that represents the total TDU count for each architecture variant. For example, for the architecture variant 14 shown in Fig. 2.3, $\boldsymbol{m} = [2 \quad 4 \quad 8]^T$ and $\Psi_{14,1:3} = [1 \quad 0 \quad 1]$ resulting in $\boldsymbol{\eta}_{TDU}(14) = [1 \quad 0 \quad 1][2 \quad 4 \quad 8]^T = 10$. Fig. 2.5 shows the relationship between the TDU count and the variant number. The two data points shown in Fig. 2.5 correspond to the architecture variants 14 and 18 with corresponding TDU counts of 10 and 6, as illustrated and verified in Fig. 2.2. Variants having TDUs at lower division levels exhibit lower TDU counts

as expected. The bit count for each variant, $\boldsymbol{\eta}_{bits}$, is calculated as

$$\boldsymbol{\eta}_{bits}(v) = \sum_{l=1}^{L} \boldsymbol{m}(d_l)\, b_l\,, \qquad v = 1,2,\dots,V. \tag{2.9}$$

Again considering variant 14 as an example, $\boldsymbol{\eta}_{bits}(14) = 2 \times 4 + 8 \times 5 = 48$ as depicted in Fig. 2.6 that shows the relationship between the bit count and the variant number. Fig. 2.6 also shows that variants utilizing TDU layers in lower division levels in general benefit from reduced bit counts. However, this general trend may be altered if excessive number of bits is used in the TDU layers of a variant. A comparison of Fig. 2.5 and Fig. 2.6 demonstrates that the change in TDU count is not necessarily followed by a similar change in bit count.

2.2 Architecture Variants Performance Matrix of a Linear PAA

The performance matrix $\boldsymbol{A}$ acts as the coefficient matrix in the integer linear program optimization and it gets weighted against performance constraints. For simplicity, in this section, the construction of the $\boldsymbol{A}$ matrix is again demonstrated through the 8 element PAA example by using $D = 3$, $L = 2$, $b_{max} = 5$, and $b_{min} = 4$ as in previous section. $\boldsymbol{A}$ matrix takes the form

$$\boldsymbol{A} = [\boldsymbol{a}_{\phi_e} \quad \boldsymbol{a}_{d=1_{msb}} \quad \boldsymbol{a}_{d=2_{msb}} \quad \boldsymbol{a}_{D=3_{msb}}] \tag{2.10}$$

where $\boldsymbol{a}_{\phi_e}$ is the vector that contains the quantization phase error of each variant and $\boldsymbol{a}_{d_{msb}}$ terms are the vectors that contain the time delay of the most significant bit (*msb*) at each level of division for each variant.

We first investigate the quantization phase error. To do so, we let the PAA operate within the frequency band defined by f_{min} and f_{max}. As is often the case, the element pitch is taken as $e_p = \lambda_{min}\,/2$ where λ_{min} is free space wavelength at f_{max}. In this paper, for numerical examples, we will select f_{max} as 30 GHz. Quantization phase error is due to discretization of selectable delay states [4]. Since phase is a function of frequency, the largest phase error occurs at f_{max}. For a

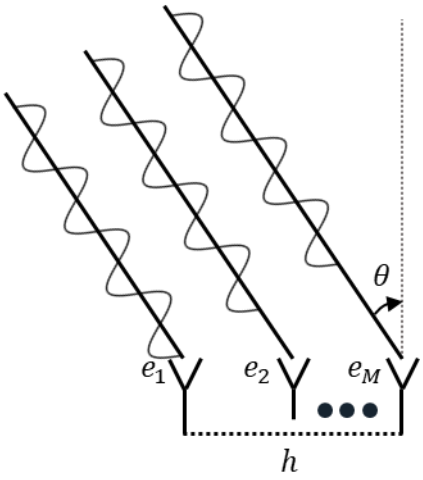

Figure 2.7 Illustration of maximum element distance for a linear array when a single TDU layer is placed directly under elements.

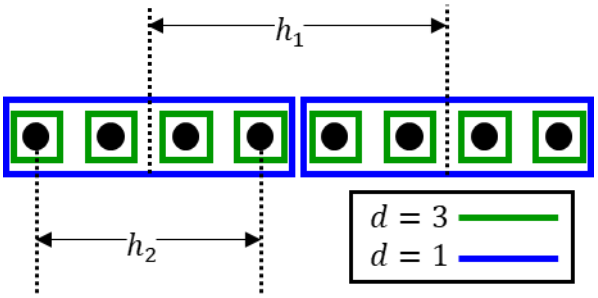

Figure 2.8 Illustration of maximum element distance for a linear array when two TDU layers are placed in the 8 element PAA architecture variant shown in Fig. 2.3.

linear array with a single layer of TDUs in division level D, the required scan distance is

$$h_{scan} = h * \sin(\theta_{max}) \tag{2.11}$$

where θ_{max} is the maximum desired scan angle of the array from boresight and h is the distance from the first element to the last element as illustrated in Fig. 2.7. This distance is translated into time to provide the maximum required time delay within the PAA as

$$\tau_{max} = h_{scan}/c \tag{2.12}$$

where c is the speed of light. The time delay of the *lsb* is then calculated as

$$\tau_{lsb} = \tau_{max}/(2^b - 1) \tag{2.13}$$

where b is the number of bits used for the TDUs. Equation (2.13) assumes even spacing from 0 (all bits at reference state) to τ_{max} (all bits are in delay state).

For a multi-layer TDU architecture, the quantization error is passed from layer to layer. The derivation begins at the lowest layer of TDU closest to the common RF feed point (i.e., TDU_1 in Fig. 2.2) and moves towards the highest layer closest to the antenna element (i.e., TDU_2 in Fig. 2.2), carrying the quantization error of the lower layers to the higher layers. The scan distance that is used in phase error derivation is no longer based on the distance between the furthest two elements of the PAA. Instead, the scan distance is based on the distance between the centers of the furthest subarrays corresponding to the respective division level. To illustrate the calculation of distances, Fig. 2.8 shows the subarray partitions of the architecture variant shown in Fig. 2.3. TDU_1 layer at the $d = 1$ division level creates 2 subarrays where each subarray consists of 4 antenna elements. The maximum spacing between these subarrays is h_1. TDU_2 layer at the $d = 3$ division level can be envisioned to create 4 subarrays (i.e., individual elements) within the subarray of the lower layer. The maximum spacing between these subarrays is h_2. The first step in calculating the h_l distances in an array is to find the number of elements, M_l, which represents all elements fed by the output of a single TDU from division level d_{l-1}. The number of elements is found by

$$M_l = 2M_{l-1}/2^{d_l - d_{l-1}} \tag{2.14}$$

where d_l is the division level where TDU_l is located, $M_0 = M$, and $d_0 = 0$. Next, a generic formula for calculating the maximum distances within division levels d_l can be given as

$$h_l = M_l * e_p \left(1 - \frac{1}{2^{d_l - d_{l-1}}}\right) \tag{2.15}$$

where e_p is the element pitch. Equations (2.14) and (2.15) can be illustrated using Fig. 2.8 where $e_p = \lambda/2$, $d_1 = 1$, and $d_2 = 3$ leading to $M_1 = 8$, $M_2 = 4$, $h_1 = 2\lambda$, and $h_2 = 3\lambda/2$. Similar to

(11), the scan distance can be solved as

$$h_{scan_l} = h_l * \sin(\theta_{max}) . \tag{2.16}$$

Using the scan distance, we can calculate the maximum time delay needed from TDU_l, τ_{max_l}, as

$$\tau_{max_l} = h_{scan_l}/c + \tau_{qe_{l-1}} \tag{2.17}$$

where $\tau_{qe_{l-1}}$ is the quantization error from the previous TDU layer (i.e., TDU_{l-1}) and $\tau_{qe_0} = 0$. When there are no TDUs located at a division level, then $d \notin [d_1 \dots, d_L]$ and $\tau_{max_d} = 0$. Before calculating the quantization error for a given layer, the *lsb* is calculated for that layer as

$$\tau_{lsb_l} = \tau_{max_l}/(2^{b_l} - 1) . \tag{2.18}$$

The quantization error at TDU_l (i.e., τ_{qe_l}) can be calculated as

$$\tau_{qe_l} = \tau_{lsb_l}/2 \tag{2.19}$$

because the maximum error made in digitally approximating a desired time delay value is half of τ_{lsb_l}. Equations (2.14)-(2.19) are solved iteratively starting from $l = 1$ and moving forward to $l = L$. If TDU_L is located at a division layer $d_L < D$, then there is at least one division following d_L without TDU based beam steering. This leads to an uncompensated time delay, $\tau_{max_{L+1}}$, which accounts for the delay from d_L to D that must be included in the final phase error calculation. To illustrate the relevance of this uncompensated distance, let us observe the architecture shown in Fig. 2.4. In this architecture, after $TDU_{L=2}$, there is one more level of division which does not contain a TDU. This leads to a grouping of two antenna elements receiving the same time delay. However, to scan the beam to some angle, θ_{scan}, the two elements would be required to have different delays to compensate for the distance between them, $h_{scan_{L+1}}$. Without element level delay states, this distance remains uncompensated in the overall architecture which increases the overall phase error. To find the uncompensated time delay caused when TDU_L is located at any division layer $d_L < D$, first equations (2.14)-(2.16) are solved with $l = L + 1$ where $d_{L+1} = D$.

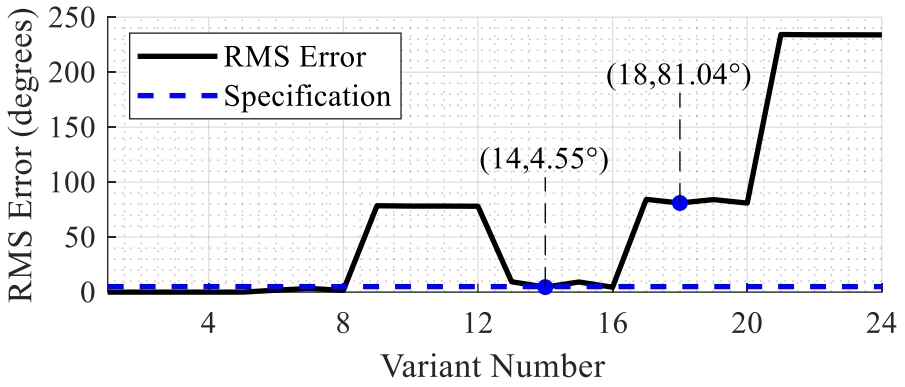

Figure 2.9 Demonstration of the non-linear relationship between RMS phase error and the variant number for the 8 element PAA.

After $h_{scan_{L+1}}$ is found, the uncompensated time delay is calculated as

$$\tau_{max_{L+1}} = h_{scan_{L+1}}/c. \tag{2.20}$$

Because large PAAs typically have many elements, the quantization phase error at the element level will be randomly distributed across the PAA. Hence, expressing phase error in terms of the root mean square (RMS) value is a more common practice and is calculated as $\tau_{qe_L}/\sqrt{3}$ [4]. However, the uncompensated distances are not randomly distributed, but are periodic, so there is no random distribution. Therefore, the phase error can be calculated as

$$\phi_{e,deg} = \left[\frac{\tau_{qe_L}}{\sqrt{3}} + \frac{\tau_{max_{L+1}}}{2}\right] * f_{max} * 360 \tag{2.21}$$

When TDU_L is located on the last level of division, $d_L = D$, the uncompensated delay is $\tau_{max_{L+1}} = 0$. The equations outlined above were used to calculate the quantization phase error for each architecture in the 8 element PAA example to form $\boldsymbol{a}_{\phi_e}$. Fig. 2.9 shows the modeled quantization phase error varies non-linearly with variant number. The specification shown in Fig. 2.9 is 5° which produces a grating lobe level of approximately -26 dB [1].

Let us now describe the construction of the $\boldsymbol{a}_{d_{msb}}$ vectors. As described in Section I, the

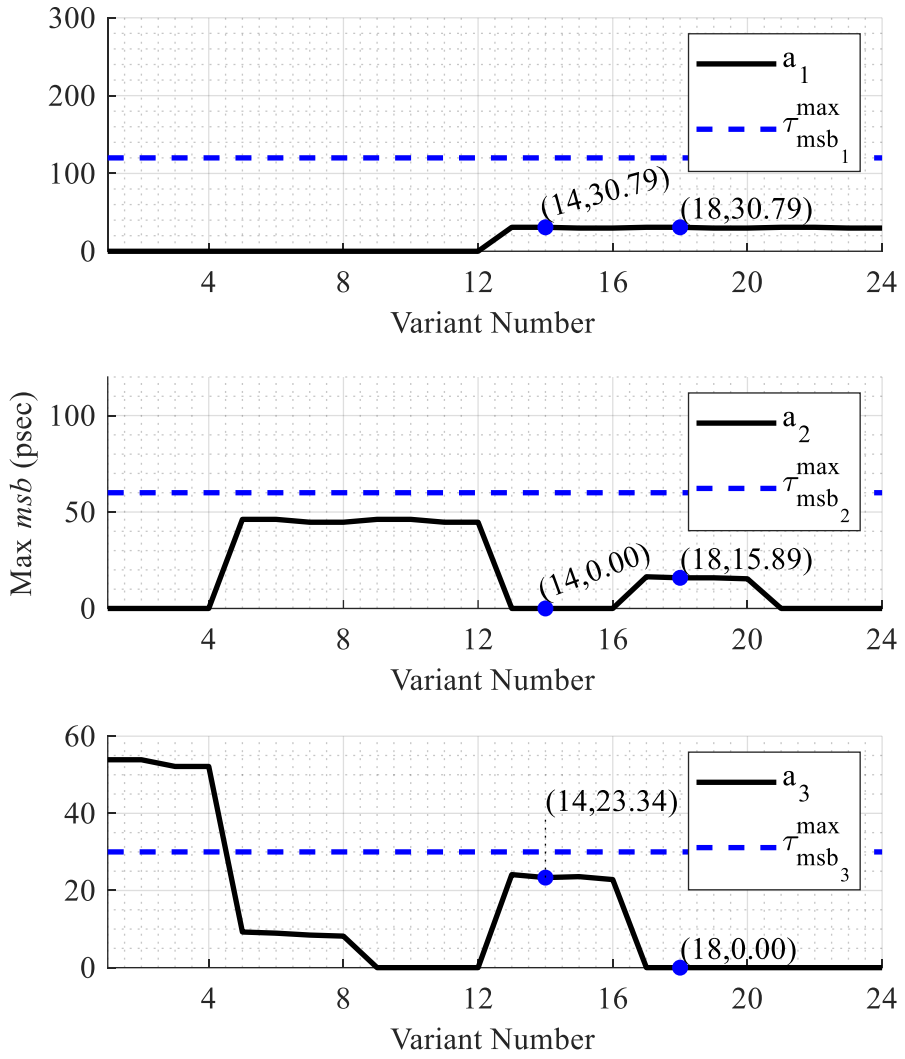

Figure 2.10 Demonstration of the non-linear relationship between the max *msb* for each level of division and the variant number for the 8 element PAA.

msb must remain under a certain size to enable manufacturability. The time delay of *msb* at each level of division can be calculated as

$$\tau_{msb_{d_l}} = \tau_{lsb_l} * 2^{b_l - 1}, v = 1,2 \dots V \tag{2.22}$$

and stored in $\boldsymbol{a}_{d=d_{l_{msb}}}$. If there are no TDUs located at a division level of a variant v, then $d \notin [d_1, \dots, d_L]$ and $\boldsymbol{a}_{d_{msb}}(v) = 0$. For the 8-element PAA example, the simulated relationship of the longest *msb* delay bit at each level of division to the variant count is shown in Fig. 2.10. The dashed

Table 2.2 Performance matrix (***A***) for the 8 element PAA

v	ϕ_e	a_1	a_2	a_3	v	ϕ_e	a_1	a_2	a_3
1	0.7	0.0	0.0	53.9	13	9.4	30.8	0.0	24.1
2	0.3	0.0	0.0	53.9	14	4.5	30.8	0.0	23.3
3	0.3	0.0	0.0	52.1	15	9.2	29.8	0.0	23.6
4	0.2	0.0	0.0	52.1	16	4.4	29.8	0.0	22.8
5	3.6	0.0	46.2	9.2	17	84.3	30.8	16.4	0.0
6	1.7	0.0	46.2	8.9	18	81.0	30.8	15.9	0.0
7	3.3	0.0	44.7	8.4	19	84.1	29.8	15.9	0.0
8	1.6	0.0	44.7	8.2	20	80.9	29.8	15.4	0.0
9	78.5	0.0	46.2	0.0	21	234.2	30.8	0.0	0.0
10	78.2	0.0	46.2	0.0	22	234.0	30.8	0.0	0.0
11	78.2	0.0	44.7	0.0	23	234.0	29.8	0.0	0.0
12	78.1	0.0	44.7	0.0	24	233.9	29.8	0.0	0.0

specification lines in Fig. 2.10 will be explained in Section 2.3. Similar to the modeled phase error demonstrated in Fig. 2.9, the maximum *msb* within a variant has a nonlinear relationship with the variant number. Since the entirety of the performance vectors in ***A*** vary nonlinearly with variant number, it is exceedingly difficult to locate the optimum architecture with larger arrays due to the exponential increase in variant counts. The entities of ***A*** belonging to the 8 element PAA example is provided in Table 2.2 for illustration and verification purposes.

It should be noted that the presented derivations assume that each TDU bit will exhibit ideal time delays and amplitude responses. Although an idealized response is the goal in TDU design, it is still common to observe that TDU bits exhibit phase and amplitude variations among each other and with respect to the reference state [46]. These variations depend on the circuit topology and fabrication tolerances. Generally, the magnitude of the variation will grow with increased TDU bit length. Such variations may possibly be included in the optimization by adding new columns to ***A*** to bound the performance degradation due to these variations. However, inclusion of these variations requires further literature review and modeling work. This was out of

the scope of the work presented in this chapter and will be addressed in Chapter 3. Hardware implementation such as a multilayered PCB with mounted TDUs, delay lines, and interfacing with antennas may also be sources of phase and amplitude errors. A fully functional hardware implementation is demonstrated in Chapter 3.

2.3 Setting up the Integer Linear Programming Equations for a Linear PAA

Linear programing aims to minimize a linear function within linear constraints and will converge efficiently on a global solution if it exists, otherwise the constraints are infeasible [41]. Integer linear programming is a special case of linear programming when the optimization variables can only take the form of integers. Integer linear programming is well suited for this work because the aim is to select a single integer variant while the constraints on the performance are linear, despite performance being a non-linear function of variant number, and the objective function is linear. Using linear programming, rather than integer linear programming, leads to mathematically optimal solutions that include fractions of TDU-A variants which is non-physical. Before a solution can be targeted, the problem being optimized is placed into standard form which can be solved using many methods including readily available software functions such as MATLAB's intlinprog. The integer linear program utilizes a variable vector, $\boldsymbol{x}$, an objective function, $\boldsymbol{Kx}$, and constraints, $\boldsymbol{A}^T\boldsymbol{x} \leq \boldsymbol{b}$. The form for expressing these for the TDU architecture problem is

$$\begin{array}{ll} minimize & \boldsymbol{Kx} \\ subject\ to & \boldsymbol{A}^T\boldsymbol{x} \leq \boldsymbol{b} \\ & x_1 + x_2 + x_3 + \cdots + x_V = 1 \\ & x_v = 0\ or\ 1\ \forall\ v = 1, \ldots, V \end{array} \tag{2.23}$$

where $\boldsymbol{x} = [x_1, x_2, \ldots, x_V]^T$, $\boldsymbol{K}$ is the coefficient vector for the objective function, and $\boldsymbol{b}$ is a column vector that contains the specification constraints determined by the number of performance constraints in the optimization. The summing constraint, $x_1 + x_2 + x_3 + \cdots + x_V = 1$, along with

the integer constraint, $x_v = 0\ or\ 1\ \forall\ v = 1,\ldots,V$, ensures that the solution will be $x_o = 1$, where subscript o stands for the optimum variant, and all other variables are zero.

The objective function $\boldsymbol{Kx}$ sets the goal of the optimization, which is to minimize the number of TDUs, the number of bits, and the quantization phase error for the TDU architecture. Hence, $\boldsymbol{Kx}$ can be expressed as

$$\boldsymbol{Kx} = [w_{TDU} \quad w_{bits} \quad w_{\phi}][\boldsymbol{\eta}_{TDU} \quad \boldsymbol{\eta}_{bits} \quad \boldsymbol{a}_{\phi_e}]^T \boldsymbol{x} \tag{2.24}$$

where and w_{TDU}, w_{bits}, w_{ϕ} are the weights for the contributions of the TDU count, bit count, and phase error, respectively. The weights allow for prioritizing some objective function coefficients over others. In this manuscript, the priority will be set to minimize TDU count, which will be followed by bit count, and then phase error with the weight selection of $[w_{TDU} \quad w_{bits} \quad w_{\phi}] = [1 \quad 0.1 \quad 0.001]$.

To illustrate the formation of constraint $\boldsymbol{b}$ for the TDU-A optimization, let us consider the 8 element PAA once again. Based on the $\boldsymbol{A}$ matrix given in (2.10) and formed in Section 2.3, the $\boldsymbol{b}$ vector takes the form

$$\boldsymbol{b} = [\phi_{max} \quad \tau_{msb_{d=1}}^{max} \quad \tau_{msb_{d=2}}^{max} \quad \tau_{msb_{D=3}}^{max}]^T \tag{2.25}$$

where ϕ_{max} and $\tau_{msb_d}^{max}$ stand for the allowable maximum phase error throughout the PAA and allowable maximum *msb* at division level d. Section 2.3 already defined $\phi_{max} = 5°$ for the numerical examples that will be pursued in this chapter. Based on the discussion given in introduction, a reasonable method for defining the allowable maximum *msb* in $d = D$ level is to consider the available physical space within the unit cell of an antenna element which can be taken to be a square area by following the discussion of [4]. With an element spacing of $\lambda_{min}/2$, the area is $\lambda_{min}^2/4$. If we assume that the TDUs will be implemented with off-chip printed circuit board (PCB) striplines in a dedicated PCB layer, [4] shows that half the square area will be consumed

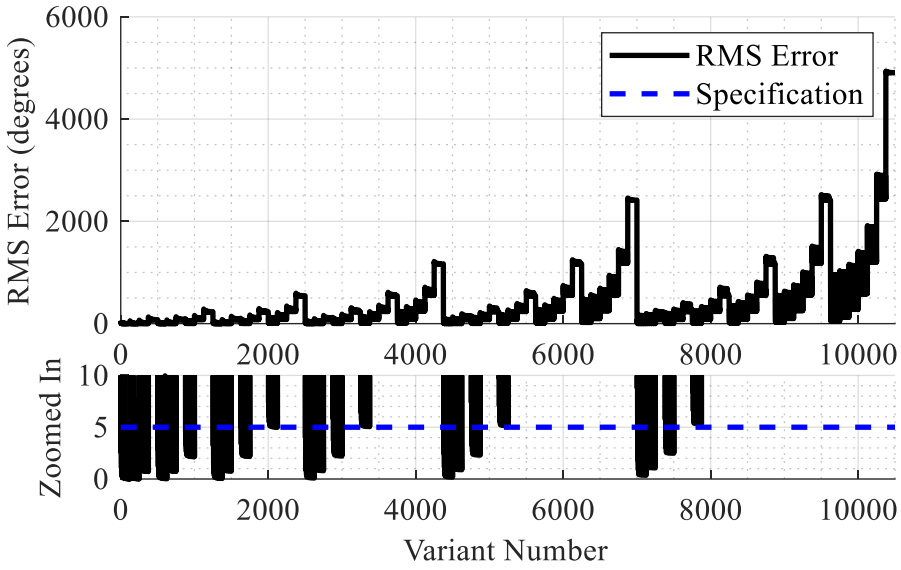

Figure 2.11 RMS phase error vs. variant number in the 128 element PAA.

by a meandered line of length $3\lambda_{min}/2$ while providing adequate isolation from PCB traces in adjacent cells. At $f_{max} = 30$ GHz, $3\lambda_{min}/2$ is 15 mm. Since some of this length may be occupied by on-chip TDU switches and interconnects, we will limit the *msb* to be no longer than 10 mm or ~30 psec with the assumption that a low dielectric constant PCB is utilized. With this choice of $\tau_{msb_3}^{max} = 30$ psec, we can increase the allowable maximum *msb* by a factor of 2 and 4 to get $\tau_{msb_2}^{max} = 60$ psec and $\tau_{msb_1}^{max} = 120$ psec since the physical space in the lower division levels increases with these factors. These specifications are shown in Fig. 2.10 along with τ_{msb_d} of the architecture variants. With these settings, the integer linear program was run on the 8 element PAA and produced the optimal architecture to be $o = 14$. Properties of variant 14 has been already shown in several figures (i.e., Figs. 2.3, 5, 6, 8, 9, and 10). It provides $\boldsymbol{a}_{1_{msb}}(14) = 30.8$ psec, $\boldsymbol{a}_{2_{msb}}(14) = 0$ psec, $\boldsymbol{a}_{3_{msb}}(14) = 23.3$ psec and $\boldsymbol{a}_{\phi_e}(14) = 4.55°$ using a total of 10 TDUs with 48 total bits in division levels $d = 1$ and $d = 3$. A full derivation example of the $\boldsymbol{A}$ and $\boldsymbol{K}$ matrices is demonstrated in Appendix C for variant 14.

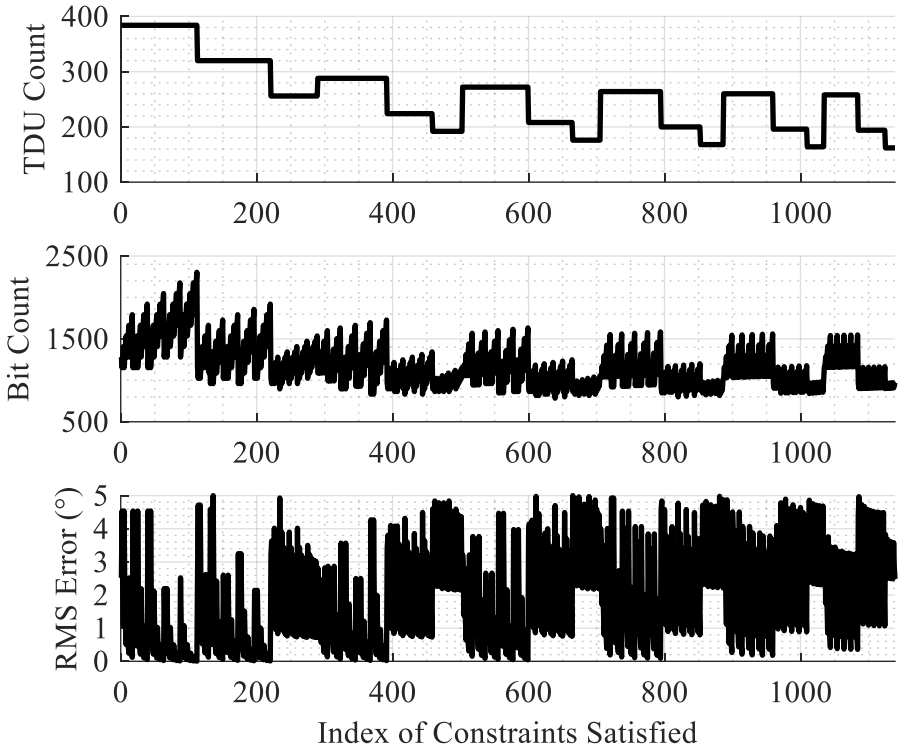

Figure 2.12 TDU count, bit count, and RMS phase error across variants of the 128 element PAA that meet the performance constraints.

2.4 Application to Large Linear PAAs

As an example, in this section we consider an $M = 128$ element linear PAA with $\theta_{max} = 60°$, $f_{max} = 30$ GHz, and $e_p = \lambda_{min}/2$. We set $L = 3$, $b_{min} = 2$, and $b_{max} = 6$. Due to 2-way power division, there are $D = 7$ division levels. Equations (2.2)-(2.4) show that there are 10500 architecture variants. We set $\phi_{max} = 5°$. Fig. 2.11 depicts the modeled phase error as a function of the variant number. The zoomed in version of Fig. 2.11 clearly shows that there are numerous architectures that satisfy the phase error. Eliminating the architectures that do not simultaneously meet the $\tau_{msb_d}^{max}$ criteria still leave out 1,139 architectures (i.e., ~11% of all architectures) suitable to meet the performance goals. Fig. 2.12 shows how the TDU and bit count varies across these 1,139 variants. Without a method to find the optimal solution, previous approaches demonstrated

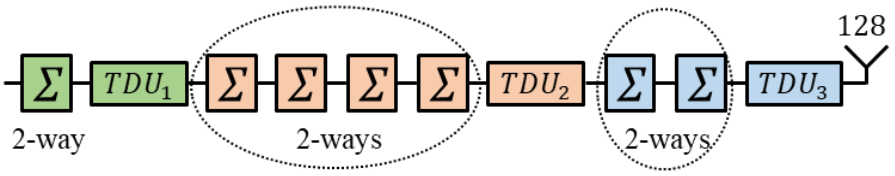

Figure 2.13 Optimum TDU architecture for the 128 element PAA where TDU_1 has 2 bits and $\tau_{lsb} = 307.9$ psec, TDU_2 has 4 bits and $\tau_{lsb} = 68.0$ psec, and TDU_3 has 6 bits and $\tau_{lsb} = 1.2$ psec.

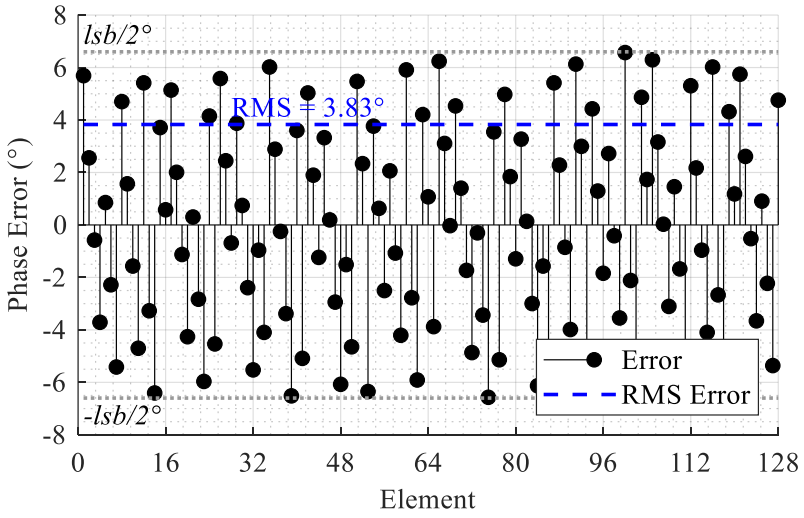

Figure 2.14 Phase error at each element of the 128 element PAA which is bounded by half the lsb at TDU_3. The phase error exhibits an RMS value of 3.83° at $f_{max} = 30$ GHz and $\theta_{scan} = 60°$.

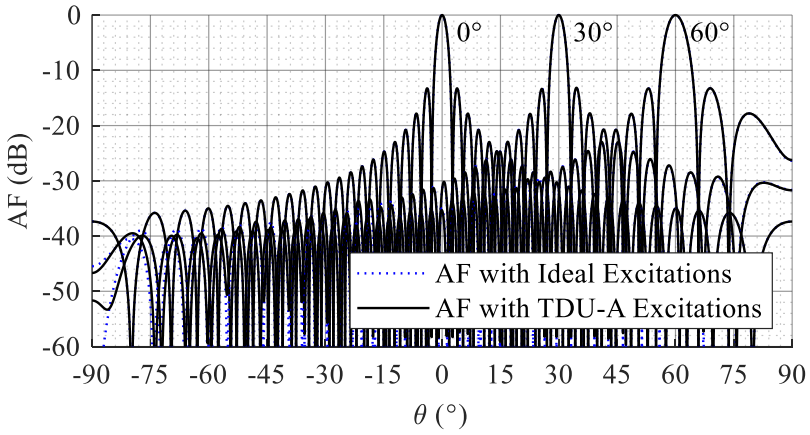

Figure 2.15 Normalized array factor of 128 element linear PAA at $f = 10$ GHz when it employs the optimum TDU architecture (TDU-A) excitations shown in Fig. 2.13 and ideal excitations.

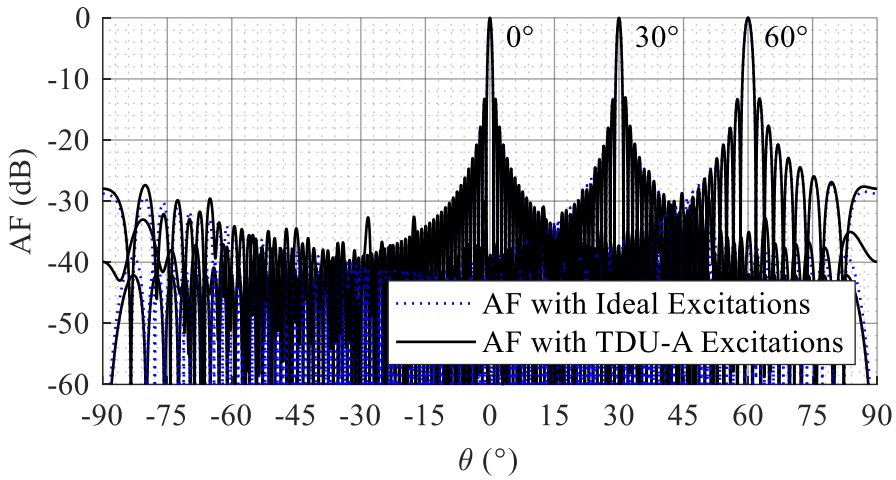

Figure 2.16 Normalized array factor of 128 element linear PAA at $f = 30$ GHz when it employs the optimum TDU architecture (TDU-A) excitations shown in Fig. 2.13 and ideal excitations.

for TDU architecture design are likely to select a variant that meets phase specifications but does not simultaneously minimize the TDU and bit count, and therefore does not minimize the cost, power, and complexity. Next, the optimization was placed into standard form and the integer linear program was run. The optimal architecture was found to be variant 7390 which has a phase error of $\boldsymbol{a}_{\phi_e}(7390) = 3.83°$ and a total of 162 TDUs. Fig. 2.13 shows the optimum architecture. An architecture that simultaneously meets all constraints can exhibit TDU counts as high as 384, which is more than double the TDU counts exhibited by the optimum architecture. The array factor (AF) is plotted to demonstrate the validity of the optimum architecture [5]. This is accomplished by calculating the ideal phases required to steer the beam to $60°$ at 30 GHz and approximating these ideal phases as closely as possible by using the bit settings of the optimum TDU architecture. The absolute phase error at each element due to the discretization of the time delay by the optimum architecture is shown in Fig. 2.14. It is seen that the error is bounded by the $\tau_{lsb_3}/2$, which is the last layer of time delay. The RMS value of the error distribution across the PAA is 3.83° which is lower than ϕ_{max}. The modeled results of the normalized AF for a 0°, 30°, and 60° scan angle at

$f = 10$ and 30 GHz is shown in Figs. 2.15 and 2.16. The agreement between the ideal AF pattern and the one generated by the optimum TDU architecture is quite good. The increase in side lobe levels due to the quantization error happens at lower than 26 dB as specified. Note that Appendix A demonstrates how to configure the TDUs within the TDU-A to steer the array as demonstrated in Figs. 2.15 and 2.16.

2.5 Application to Large Square Lattice 2D PAAs

The presented integer linear programming formulation can be extended to optimize the TDU architecture of 2D square lattice PAAs with minor modifications when the number of elements is power of 4 (i.e., $M = 4^{D/2} \times 4^{D/2}$) and assuming a symmetric scan (i.e., $\theta_{max} = \theta_0$ in all azimuth cuts). As an example, we consider a PAA with $M = 256 \times 256$ elements, $\theta_{max} = 60°$, $f_{max} = 30$ GHz, and $e_p = \lambda_{min}/2$. We select $L = 3$, $b_{min} = 2$, and $b_{max} = 6$. The linear PAAs discussed in the previous sections exhibited 2-way power divisions in its RF-fanout. Instead, 4-way power divisions can be employed in the considered square lattice PAAs. The total number of division levels is determined using (2.1) with base 4 as $D = 8$. Subsequently, (2.2) is used to determine the architecture variant count due to division levels as $V_{DL} = 120$. Equation (2.3) is invoked to determine the total number of variants due to the allowable bit counts as $V_{AB} = 125$. Finally, the total number of TDU architecture variants is found using (2.4) as $V = 15000$.

The generation of the variant matrix $\boldsymbol{\Psi}$ follows the Algorithm 2.1. The total TDU count and total bit count are found using (2.8) and (2.9), however $\boldsymbol{m}$ is modified as

$$\boldsymbol{m} = [4^1 \quad 4^2 \quad \ldots \quad 4^D]^T \tag{2.26}$$

due to 4-way power divisions. The performance matrix $\boldsymbol{A}$ is generated by following the method outlined in Section 2.3. Scan distances are again calculated based on the center locations of the subarrays formed by the division levels carrying the TDU layers. Since the goal is to provide

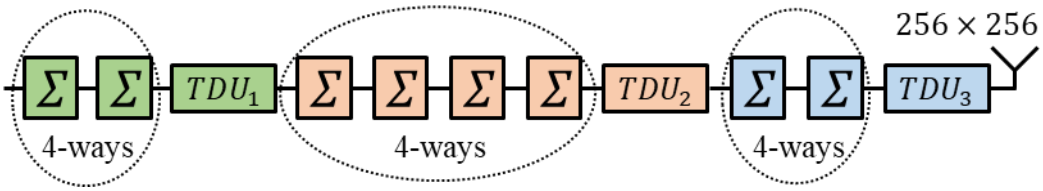

Figure 2.17 TDU architecture variant 7395 of the 256×256 element PAA where TDU_1 has 2 bits and $\tau_{lsb} = 1306.4$ psec, TDU_2 has 5 bits and $\tau_{lsb} = 60.6$ psec, and TDU_3 has 6 bits and $\tau_{lsb} = 1.5$ psec.

$\theta_{max} = 60°$ in all azimuth cuts, the largest distance among the subarrays should be considered to determine the worst-case phase error and set the *lsb* and *msb* of the TDUs. For the square array, the largest distance among the subarrays is between those along the diagonal. This necessitates to update h_l in equation (2.15) as

$$h_l = M_l\sqrt{2} * e_p\left(1 - \frac{1}{2^{d_l - d_{l-1}}}\right) \tag{2.27}$$

where the only change is the multiplication of $\sqrt{2}$ which accounts for the diagonal. Next, the procedure outlined in (2.16)-(2.21) is followed for calculating the phase error of the 2D PAA. The phase error in this example is again set as $\phi_{max} = 5°$.

The optimization was placed into standard form and the integer linear program was run. Eliminating the architectures that does not meet the maximum allowable RMS phase error criteria leaves 897 of 15000 possible architectures. The optimal architecture is found to be variant 7395 which is shown in Fig. 2.17 and has an RMS phase error of $\boldsymbol{a}_{\phi_e}(7395) = 4.15°$ with a total of 69648 TDUs. To compare the performance of the ideal phase settings and the modeled discretized architecture, the AF at $\theta = 60°, \phi = 45°$ scan angle is shown in Fig. 2.18 and 2.19 in sine space where $u = \sin(\theta)\cos(\phi)$ and $v = \sin(\theta)\sin(\phi)$. The scan angle $\theta = 60°, \phi = 45°$ was selected because it is the direction of the longest dimension and will produce the highest error. Increased

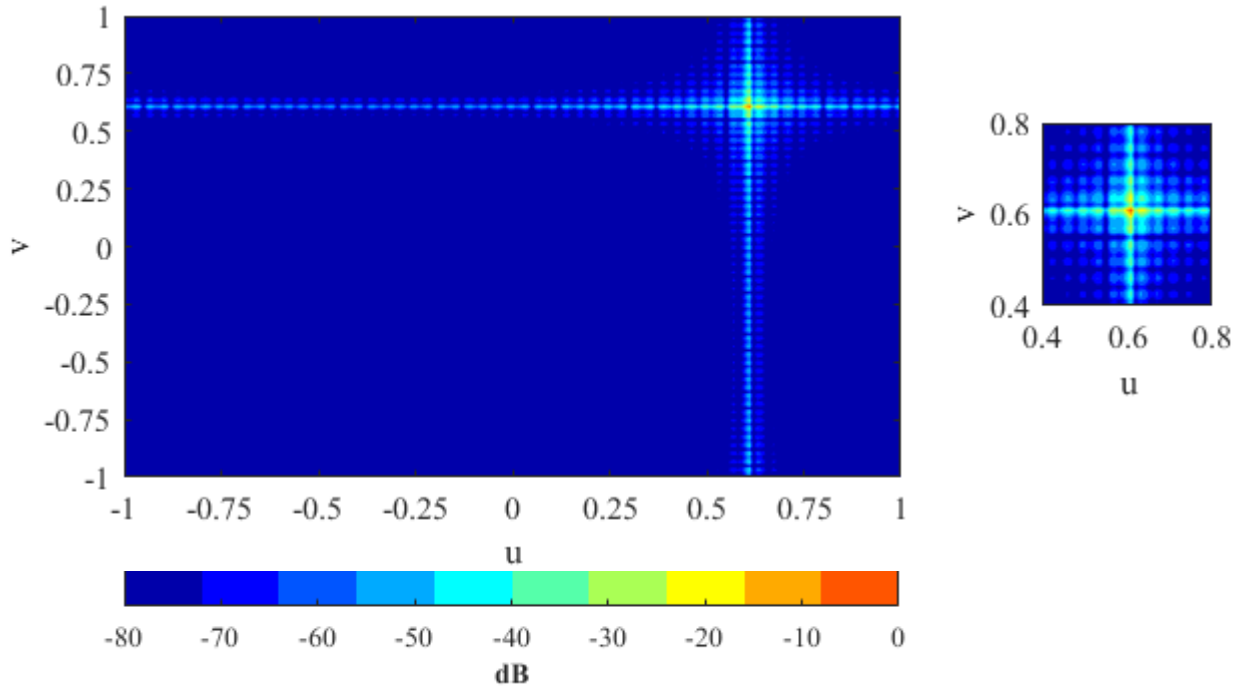

Figure 2.18 Array factor of 256×256 PAA when beam is scanned to $\theta = 60°, \phi = 45°$ using phase delays that are ideal.

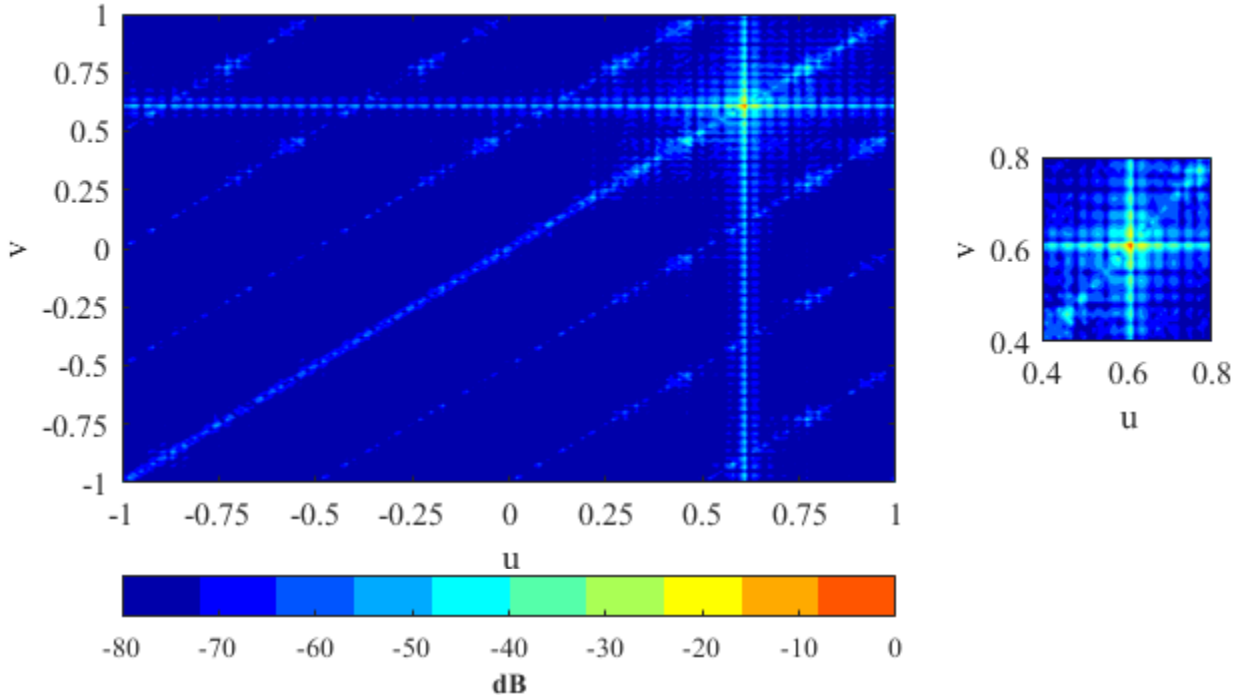

Figure 2.19 Array factor of 256×256 PAA when beam is scanned to $\theta = 60°, \phi = 45°$ using phase delays that are generated by the TDU architecture in Fig. 2.17.

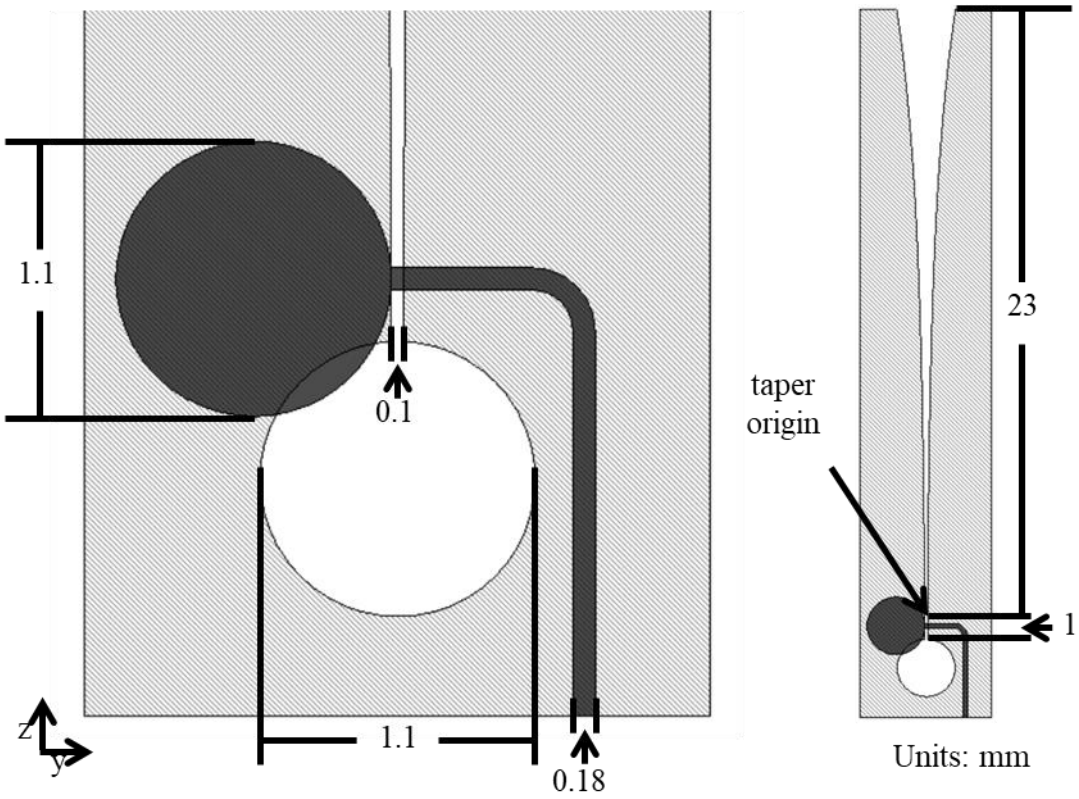

Figure 2.20 Antenna element geometry (dimensions are in mm).

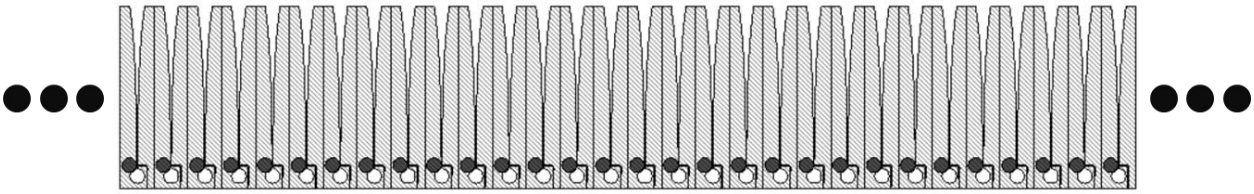

Figure 2.21 A demonstration section from the 128 element array model.

side lobe levels due to the quantization error is observed however these degradations are below 26 dB. Similar performance is achieved at additional frequencies and scan angles.

Following the traditional method of moving bits backwards a single layer at a time [4], one may have found that architecture variant 738 meets the requirement with the 3 TDU layers distributed amongst the highest 3 division levels closest to the antenna elements. This would lead

to an RMS phase error that is 4.8°, which satisfies the constraints; however, this architecture has 16368 more TDUs compared the optimal architecture, which is an increase of 23.5%.

2.6 Verification Through Full-Wave Simulation of a Linear PAA

The presented TDU architecture optimization does not consider the mutual coupling and impedance matching effects at the element ports of the PAA. This section resorts to full-wave electromagnetics simulations to demonstrate that the optimized architecture nevertheless provides an excellent performance when applied to broadband PAAs. Specifically, a broadband (4 GHz – 30 GHz) 128 element linear PAA performing with 3:1 VSWR up to 50° scan angle and less than ~4:1 VSWR at 60 degree scan is designed in Ansys Electronics Desktop 2021R1 HFSS modeler and excited according to the excitation coefficients obtained by the TDU architecture (TDU-A) in Section V. At 10 GHz and 30 GHz, VSWR is less than 3:1 for all scan angles. The antenna elements of the PAA are Vivaldi antennas and designed based on the well-established approaches outlined in [42-43] by employing 1D periodic boundary conditions. Figs. 2.20 and 2.21 depict the design geometry where the element metallizations are placed on both sides of a 16 mil thick substrate with a dielectric constant of 3.55 and a loss tangent of 0.0027 (Rogers 4003). The elements and are excited by stripline feed in the center of the substrate as shown by the black colored geometries in Fig. 2.20 and 2.21. The equations used for the exponential taper of the slot is $y = 0.05e^{0.135z}$. The pitch of the array is 5 mm, implying $\lambda/2$ at $f = 30$ GHz. It is important to note that literature presents various Vivaldi PAAs with modified design aspects to achieve better performances in terms of scan range and bandwidth [44-45]. However, such optimized designs are beyond the scope of this presented work. The full wave simulation of the 128 element PAA demonstrates a peak broadside realized gain of 22.1 dBi at 10 GHz and 27.3 dBi at 30 GHz with a total efficiency of 96.1% and 87.9%, respectively. Fig. 2.22 compares the modeled AF pattern

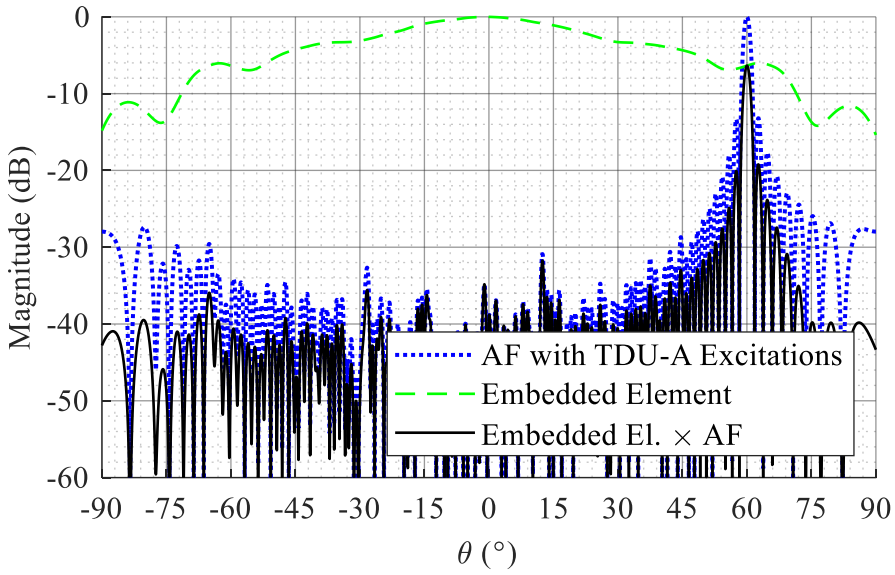

Figure 2.22 Normalized patterns for the 128 element Vivaldi antenna array at 30 GHz with a 60° scan.

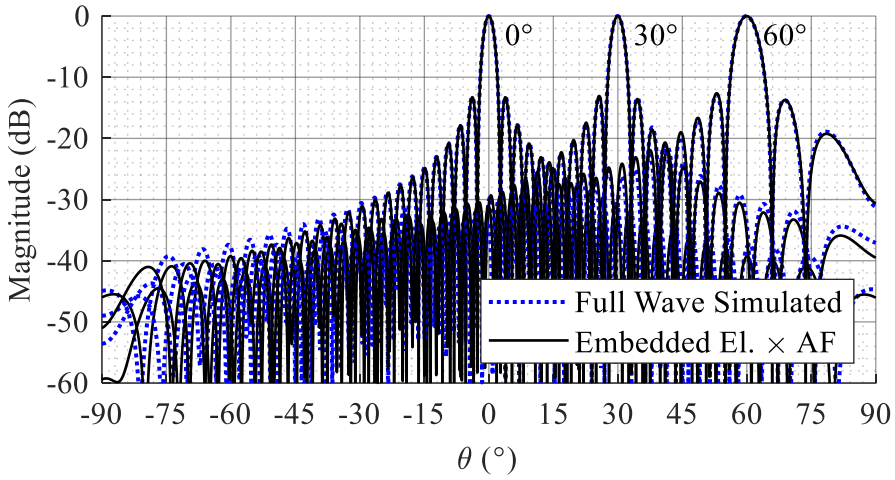

Figure 2.23 Normalized full wave simulated 128 element PAA pattern compared with [embedded element × AF] pattern at $f = 10$ GHz employing the optimum TDU architecture shown in Fig. 2.13.

with the [embedded element × modeled AF] pattern at 30 GHz with a scan angle of 60° when AF is excited with the excitations obtained from optimized TDU architecture. Embedded element

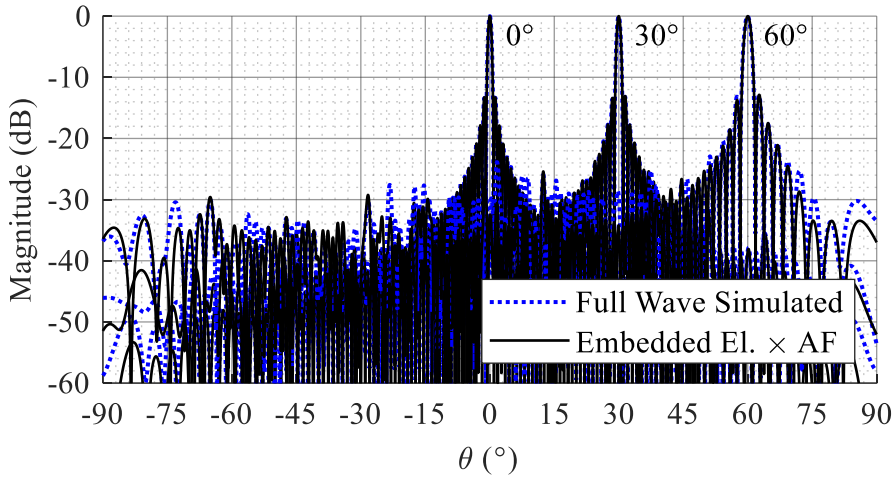

Figure 2.24 Normalized full wave simulated 128 element PAA pattern compared with [embedded element × AF] pattern at $f = 30$ GHz employing the optimum TDU architecture shown in Fig. 2.13.

pattern is obtained from one of the center elements of the full-wave simulated 128 element Vivaldi PAA when all other elements are terminated with 50Ω. Embedded element pattern reduces the peak magnitude of the pattern; however, scan angle is maintained with increased side lobe levels due to the quantization error lower than the 26 dB level as specified. This shows the applicability of the proposed TDU architecture design in presence of mutual couplings. Figs. 2.23 and 2.24 compares the [embedded element × modeled AF] pattern with the pattern obtained from the full wave simulation to investigate the potential effects of edge elements. The simulated patterns are presented at 10 GHz (Fig. 2.23) and 30 GHz (Fig. 2.24) for scan angles of 0°, 30°, and 60°. The comparison shows excellent agreement where pointing errors are less than 0.1° and increased side lobe levels due to the quantization error lower than the 26 dB. Full wave simulations clearly show that excellent steering performance can be achieved by using the excitations from the optimal TDU architecture generated in Section V. A fully functioning hardware implementation though may suffer from some non-idealities as described end of Section 2.3 and is considered in Chapter 3.

2.7 Linear PAA TDU-A Optimization Conclusions

A systematic method for optimizing the time delay architecture of phased antenna arrays is introduced in this chapter to guarantee the desired phase error requirement while minimizing power, complexity, and cost. The method utilizes integer linear programming with an objective function, constraints, and weightings to determine the optimal architecture. The method is demonstrated with three modeled example PAAs: an 8 element linear PAA, a 128 element linear PAA, and a 256×256 element PAA. An optimal architecture is found for each example that minimized the TDU and bit count while achieving the RMS phase error performance requirement. The array factor plots are generated to demonstrate the achievable performance of each case. Full wave simulation of the 128 element linear array constructed with Vivaldi antennas shows excellent steering and grating lobe levels due to the quantization error from the optimal TDU architecture excitations. The presented formulation does not readily accommodate TDU architectures of arbitrary 2D PAAs because the RF-fanout is not unique in such 2D antenna arrays. Chapters 3 and 5 aim to address this arbitrary lattice and expand the concept to a more generalized algorithm that will also consider the phase errors exhibited by the practical implementations of the TDUs. Additionally, the demonstrated work in this manuscript is simulation based as a fully functioning hardware implementation would require a significant effort and detail design. However, Chapter 3 addresses the practical implementations of an RF-fanout and TDUs and analyzes the phase non-idealities associated with them.

Chapter 3: Ultra-Wideband Phased Antenna Array Time Delay Unit Architecture Optimization in Presence of Component Non-Idealities[2]

Fig. 3.1 demonstrates a TDU circuit consisting of n bits which can switch between a reference and a delay state. As in Chapter 2, an amplifier is typically included to compensate for the loss incurred by the bits. Ultra-wideband (UWB) phased antenna array designers are often required to distribute the time delay to multiple division levels within the RF-fanout due to space constraints at the element level [4]; thereby creating a TDU architecture (TDU-A). Fig. 3.2 shows an exemplary (but also the optimal as discussed in Section 3.2) TDU-A for an $M = 16$ element linear PAA with $D = 4$ division levels. $L = 2$ TDU layers are distributed between the $d = 1$ division level (TDU_1) and the $d = 4$ division level (TDU_2) of the RF-fanout. This TDU-A is one configuration out of many possible variations. The number of variants grows exponentially as the number of elements increases. In Chapter 2, it is demonstrated that there exists an optimal TDU-A which can be found by a system architect using ILP. However, despite its comprehensiveness, the optimization model introduced focuses on ideal implementations of feed networks such as with the assumptions of perfectly matched and isolated power dividers with ideal transmission lines. This also seems to be the approach taken in the existing literature. Even though different approaches for designing TDU-As are presented [1,4-5], literature does not provide a consideration of the impact of non-ideal responses of the circuit components that form the TDU-A in its practical implementation. In practice, the designs of the circuit components within a TDU-A are typically carried out independently by different engineers in a way to meet a set of requirements imposed

[2]Portions of this chapter have been previously published in IEEE Open Journal of Antenna and Propagation [59] by the author and have been reproduced here under the CC-BY-NC-ND creative commons license.

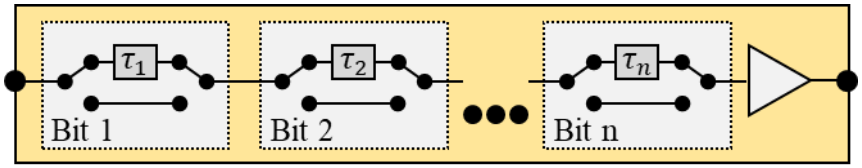

Figure 3.1 A TDU block diagram with n bits, each with τ_n of delay capability.

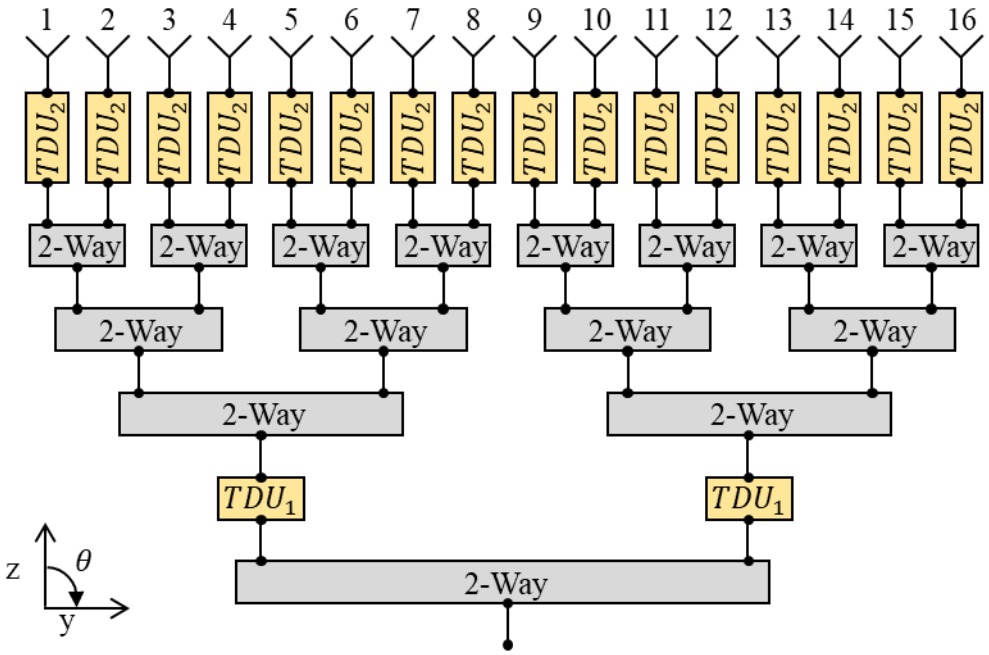

Figure 3.2 An example TDU architecture for a 16 element PAA (which is also the optimal for the PAA and its requirements considered in this chapter).

by the TDU-A system architect. Although these requirements can be strict, they are far from being ideal (e.g., return loss (RL) >15 dB vs RL >∞ across the UWB). The major circuit components in the TDU-A shown in Fig. 3.2 are the 2-way power dividers, TDUs, and antennas. The non-idealities in the network responses of these components and their frequency dependent variation lead to time delay errors. Therefore, it is of interest to account for these non-idealities in the optimization model of [13]. If these errors are left unnacounted for, radiation pattern degredations

that cannot be resolved with PAA calibration occur due to the unavailibility of required delay lengths within TDUs. This is espcially pronounced at the wider scan angles as shown in Fig. 3.2.

This chapter offers three major contributions to this dissertation. The first is the transfer equation derivation through signal flow diagram of key componts within the physical TDU-A implementation and relating the transfer equation into time domain in order to account for delay ripple when ports of the components are not terminated with idealistic perfectly matched impedances. The second is to incorporate these non-idealities (i.e. delay ripples) within the optimization model of [13] to obtain the best TDU-A. The final contribution is the first experimental demonstration of the TDU-A designed based on the optimization results and thereby closing the modeled to measured loop. Some non-idealities in the responses of the feed network components may be specific to the particular feed network implementation technology and associated with fabrication and/or component tolerances. On the other hand, there are three major prevelant time delay errors that are not limited to a particular implementation or component. This chapter focuses on these three major time delay errors that are associated with the frequency dependent phase ripples arising from the imperfections in 1) component VSWR, 2) power divider isolation and load mismatch, and 3) transmission line dispersion. The approach presented can be further extended by the designers to include the time delay errors that may come from a specific impelmentation technology and/or manufacturing tolerances.

To demonstrate the validity of the presented algorithm, a TDU-A is designed for an $M = 16$ element linear PAA consisting of Vivaldi antenna elements operating from 5 GHz to 30 GHz. By using fixed length delay lines to represent the TDU states within the TDU-A, three feed networks and PAAs are designed and fabricated to investigate the performance of radiation patterns steered towards 0°, 25°, and 50° scan angles. It is important to note that, although this

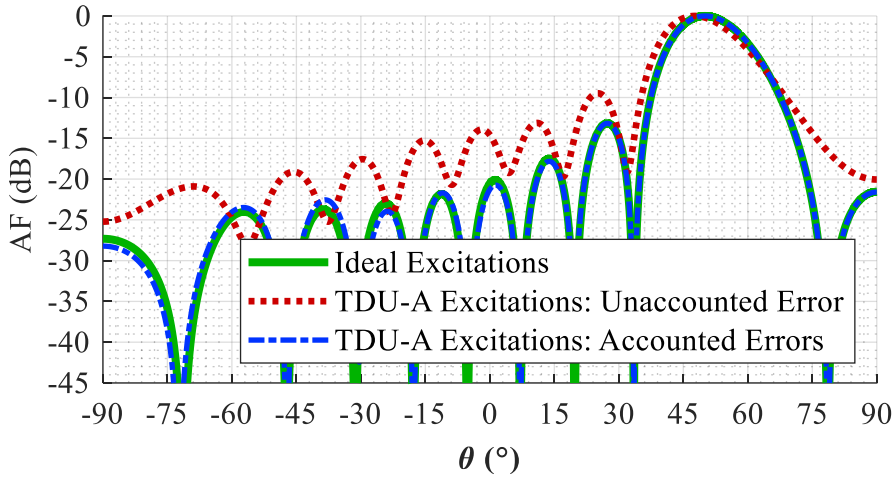

Figure 3.3 Effect of time delay errors from component non-idealities for the TDU-A shown in Fig. 3.2 at $f_c = 17.5$ GHz in the array factor (AF) patterns with ideal excitations and excitations from the TDU-A when optimized with the time delay errors accounted or not.

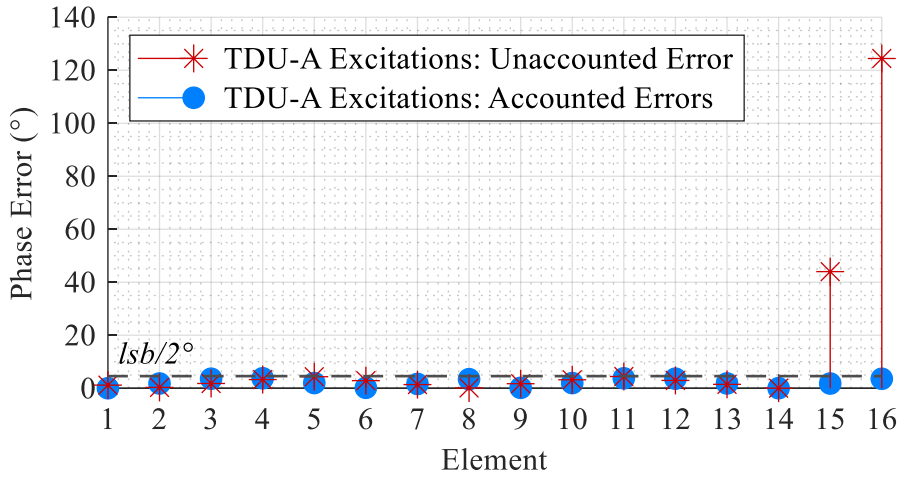

Figure 3.4 Effect of time delay errors from component non-idealities for the TDU-A shown in Fig. 3.2 at $f_c = 17.5$ GHz in the absolute value of the phase error across antenna elements.

dissertation considers stationary beam steering for the ease of implementation, the optimizaton method is applicable to electrically steered PAAs that incorporate controled TDU devices.

3.1 Time Delay Errors in Linear PAAs

Time delay error terms stem from the non-idealities of the components within the feed

network that is designed to implement the TDU-A for practical use. These errors must be modeled and included in the total delay requirement of the TDU-A before proceeding with the optimization. Chapter 2 determined the delay range and resolution of a TDU-A only by the geometry of a uniform plane wave intersecting with the PAA which results in a progressive phase across the array [4]. Different than this, there are three pervasive time delay error terms considered in this chapter that stem from non-ideality of the TDU-A components: delay variation by phase ripple due to divider isolation and load mismatch (τ_{div}), delay variation by phase ripple due to VSWR (τ_{VSWR}), and dispersion in the transmission lines (τ_{disp}). Many of the components in a TDU-A, such as the TDU itself, cannot be designed prior to architecting the TDU-A. The requirement imposed by the system architect establishes the worst-case performance acceptable for each component. Consequently, the TDU-A is designed without *a priori* knowledge of performance across frequency. Hence, TDU-A design must assume the worst-case delay error that can arise from the components.

Sections 3.2.1-3 address each time delay error term individually. As a primer, their performance effect is demonstrated in Figs. 3.3 and 3.4. The array factor (AF) patterns in Fig. 3.3 are generated by three separate phase excitations to a $M = 16$ element PAA at $f_c = 17.5$ GHz (i.e., center frequency of the 5 GHz – 30 GHz operation band). The PAA exhibits an element spacing $e_p = 0.5$ cm which is half wavelength at $f_{max} = 30$ GHz. Its beam is steered towards the maximum desired scan angle of $\theta_{max} = 50°$. The architecture shown in Fig. 3.2 was designed with the optimization method in Chapter 2 for the case when time delay errors are unaccounted or accounted as detailed in Section 3.2.5. It is observed that the radiation pattern generated by the TDU-A optimized without acounting the time delay errors of the feed network components shows degraded sidelobe levels when compared to the patterns generated by the ideal excitations and by

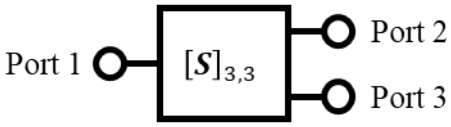

Figure 3.5 3-port S-parameter block.

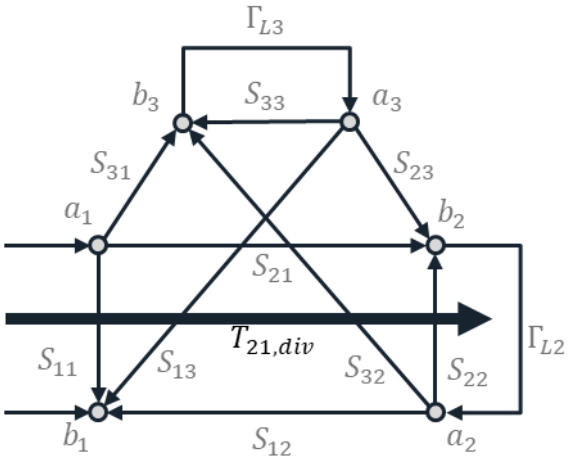

Figure 3.6 Signal flow graph representation of Fig. 3.5 when ports 2 and 3 are terminated with loads.

the TDU-A optimized with accounting the time delay errors. The degraded side lobe levels (SLLs) are caused by the lack of delay range required to compensate for the delay errors generated by the TDU-A components. In both cases, a bit search is conducted that aims to minimize the delay error between the TDU bit selected and the ideal phase at each element (see Appendix A). However, as shown in Fig. 3.4, the phase error at the 15th and 16th elements of the PAA, when compared to an ideal progressive phase excitation, falls significantly outside the quantized error bound ($lsb/2° = 4.5°$) when the TDU-A is optimized without accouting for the component delay errors. This occurs because the required delay to steer the 15th and 16th elements is simply not available by the TDU-A and selecting different states cannot overcome this fundamental deficiency. Conversely, when the TDU-A is optimized by accounting the component delay errors, the architecture is capable of

fully generating the desired time delays and the phase distribution errors fall below the desired quantization error. The quantized error bound results from the *lsb* which is found through the optimization in Section 3.1.5.

3.1.1 Divider Isolation and Load Mismatch

Imperfect divider isolation and load mismatch introduces frequency dependent phase ripple to the signal through path. A divider is a 3-port network as shown in Figs. 3.5 and 3.6. Based on Mason's rule [48] and the signal flow diagram in Fig. 3.6, the transmission from port 1 to port 2 is

$$T_{21,div} = \frac{S_{21}^D - S_{21}^D S_{33}^D \Gamma_{L3} + S_{31}^D \Gamma_{L3} S_{23}^D}{1 - (S_{22}^D \Gamma_{L2} + S_{33}^D \Gamma_{L3} + S_{23}^D \Gamma_{L2} S_{32}^D \Gamma_{L3}) + S_{22}^D S_{33}^D \Gamma_{L2} \Gamma_{L3}} \tag{3.1}$$

where S_{ij}^D are the complex S-parameters of the divider, Γ_{L2} and Γ_{L3} are the load reflection coefficients at ports 2 and 3, respectively. Note that when all loads are perfectly matched, $T_{21,div} = S_{21}^D$. From (1), $T_{21,div}$ is clearly dependent on Γ_{L2}, Γ_{L3} and isolations (i.e. S_{23}^D and S_{32}^D). The phase delay error at a frequency f is

$$\phi_{21,div}(f) = \angle(T_{21,div}) - \angle(S_{21}^D). \tag{3.2}$$

This phase delay error (in degrees) is typically less than 360° for a well-matched divider and can be converted into time to obtain the time delay error due to the isolation and load mismatch as

$$\tau_{21,div} = \frac{-\phi_{21,div}}{f\ 360}. \tag{3.3}$$

Equations (3.2) and (3.3) show that when $\tau_{21,div}$ is a negative number, the signal takes less time to propagate from port 1 to port 2 than the baseline S_{21}^D, whereas a positive number corresponds to a signal that takes more time. Positive value is the primary concern leading to a lack of TDU range since a negative delay error will still fall within the range of the TDU-A optimized without regarding component non-idealities. Therefore, the single worst-case delay error for all frequencies

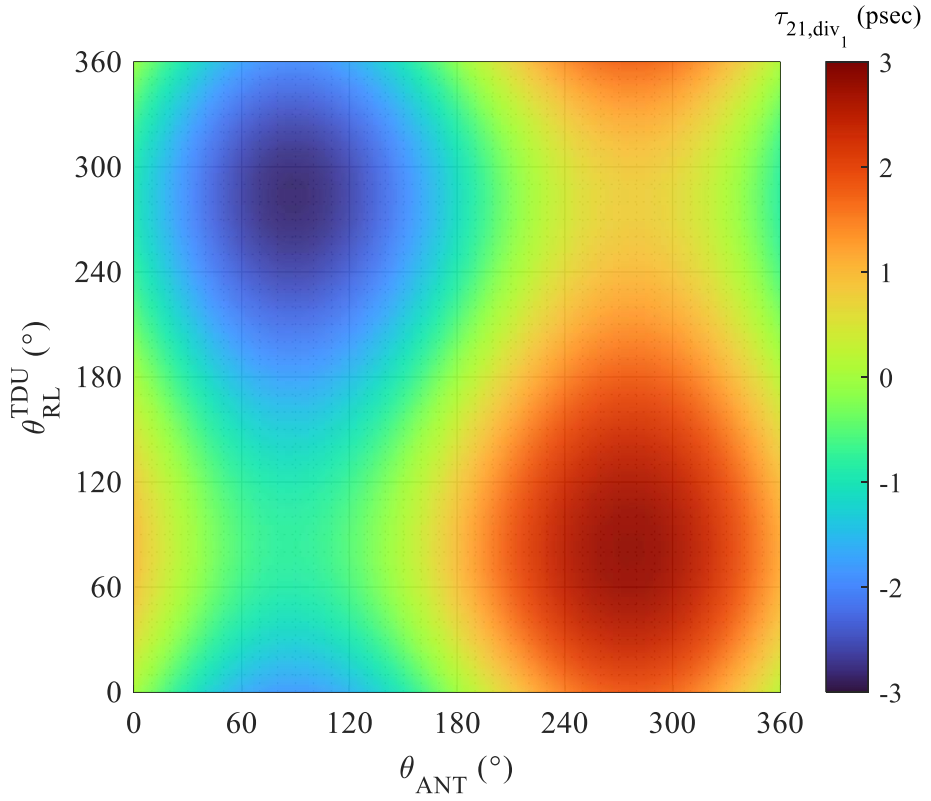

Figure 3.7 Time delay variation at 5 GHz when the divider is terminated with $\Gamma_{L2} = \Gamma_{L3} = 0.178\, e^{-j\theta_{RL}^{TDU}}$ and $\angle\Gamma_{L2}$ and $\angle\Gamma_{L3}$ are swept independently.

which must be accommodated in the TDU-A is

$$\tau_{e,div} = \max\left(\tau_{21,div}(f)\right). \tag{3.4}$$

Using (3.1)–(3.4), we proceed with calculating the time delay error from the divider to be designed for the $M = 16$ element PAA. The design requirements that will be imposed on the reciprocal divider are RL ≥ 10 dB (i.e., $S_{11}^{D},\ S_{22}^{D},\ S_{33}^{D} \leq 0.316e^{-j\theta_{RL}^{D}}$), isolation (ISO) ≥ 15 dB (i.e., $S_{32}^{D} \leq 0.178\, e^{-j\theta_{ISO}^{D}}$), and insertion loss (IL) ≤ 1 dB (i.e., $S_{21}^{D},\ S_{31}^{D} \leq 0.631e^{-j\theta_{IL}^{D}}$). Based on the RF fan-out shown in Fig. 3.2, the output ports of the dividers can be loaded in three different scenarios, by: 1) TDUs with an imposed requirement of RL ≥ 15 dB (i.e., $S_{11}^{TDU} \leq 0.178\, e^{-j\theta_{RL}^{TDU}}$), 2) input ports of the subsequent power dividers, or 3) antenna elements which are to be designed with a

$VSWR \leq 3:1$ requirement, implying $S_{11}^{ANT} \leq 0.5\, e^{-j\theta_{ANT}}$. The delay values for each of the three load cases are calculated independently using equations (3.1)–(3.4). For each case, the loads are swept independently from 0° to 360° in 5° steps while the magnitudes are held constant at the worst-case value. The S-parameter amplitudes of the divider are taken as worst-case values and the phases (i.e. θ_{RL}^{D}, θ_{ISO}^{D}, θ_{IL}^{D}) are modeled as ideal. Among these S-parameters, the most dominant factor in (3.1) is the stand-alone S_{21}^{D} term in numerator due to not being multiplied with a load reflection coefficient, however $\angle S_{21}^{D}$ is strictly bounded in the divider design (e.g. ~90° for a standard single stage Wilkinson power divider). Sweeping phases of the other S-parameters in (3.2) does not provide new information since they are multiplied with load reflection coefficients that are already being swept in phase. Fig. 3.7 depicts the result of the sweep for the first power divider termination scenario when the ports 2 and 3 are connected to TDUs at 5 GHz, implying $\Gamma_{L2} = \Gamma_{L3} = S_{11}^{TDU} = 0.178\, e^{-j\theta_{RL}^{TDU}}$. The maximum delay happens at 5 GHz as expected from (3.3) and leads to $\tau_{e,div_1} = 2.8$ psec. This is due to the fact that the consideration of (3.2) as in Fig. 3.7 is frequency independent until the last step where the phase values get converted into time domain using (3.3) to generate the y-axis of Fig. 3.7. Hence, the largest error is observed at the lowest frequency.

The phase sweeps of load reflection coefficients lead to worst case errors of $\tau_{e,div_2} = 5.1$ psec, and $\tau_{e,div_3} = 8.2$ psec when the output ports are connected to power dividers (scenario 2, $\Gamma_{L2} = \Gamma_{L3} = S_{11}^{D} = 0.316e^{-j\theta_{RL}^{D}}$) and antenna elements (scenario 3, $\Gamma_{L2} = \Gamma_{L3} = S_{11}^{ANT} = 0.5\, e^{-j\theta_{ANT}}$), respectively.

3.1.2 TDU VSWR

Non-ideal components such as TDUs introduce frequency dependent phase ripple on the through path due to the finiteness of their VSWR. A generic 2-port S-parameter network as shown

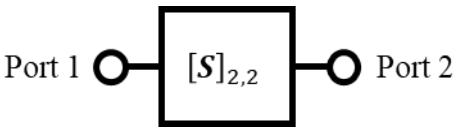

Figure 3.8 2-port S-parameter block.

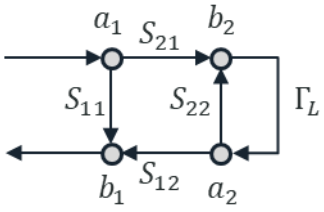

Figure 3.9 Signal flow graph representation of Fig. 3.8 when port 2 is terminated with a load.

in Fig. 3.8 can be used to model these components. From the signal flow diagram shown in Fig. 3.9, using the Mason's rule [48], the transmission from port 1 to port 2 can be determined as

$$T_{21,VSWR} = \frac{S_{21}^{TDU}}{1 - S_{22}^{TDU}\Gamma_L} \tag{3.5}$$

where S_{ij} are the complex S-parameters and Γ_L is the load impedance at port 2. As was the case for the divider, the deviation from the baseline phase can be calculated as

$$\phi_{21,VSWR} = \angle T_{21,VSWR} - \angle(S_{21}^{TDU}) = -\angle(1 - S_{22}^{TDU}\Gamma_L) \tag{3.6}$$

which shows that the only dependence is on the return loss specification of the TDU and the load which it is connected to. This is converted to time to obtain the delay error as

$$\tau_{21,VSWR} = \frac{-\phi_{VSWR}}{f\ 360}. \tag{3.7}$$

Since positive value of $\tau_{21,div}$ is the main concern as explained in previous section, the worst-case delay error that must be accommodated by the TDU-A is

$$\tau_{e,VSWR} = \max\left(\tau_{21,VSWR}(f)\right). \tag{3.8}$$

Using (3.5)–(3.8), we proceed to calculate the time delay error for the $M = 16$ element PAA. The

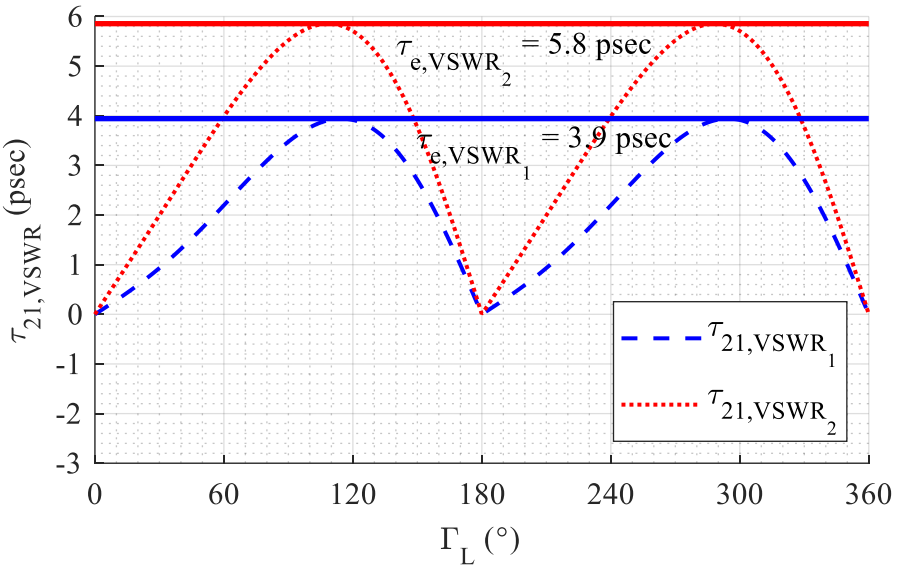

Figure 3.10 Time delay variation of TDU at 5 GHz when terminated with $\Gamma_L = S_{11}^D = 0.316\, e^{-j\theta_{RL}}$ (VSWR$_1$) and $\Gamma_L = S_{11}^{ANT} = 0.5\, e^{-j\theta_{ANT}}$ (VSWR$_2$)

TDU ($S_{22}^{TDU} \leq 0.178\, e^{-j\theta_{RL}^{TDU}}$) has two possible load terminations: 1) power divider with an imposed requirement of RL ≥ 10 dB (i.e., $S_{11}^D \leq 0.316 e^{-j\theta_{RL}}$) and 2) antenna elements which are to be designed with a $VSWR \leq 3{:}1$ requirement, implying $S_{11}^{ANT} \leq 0.5\, e^{-j\theta_{ANT}}$. Sweeping the phase possibilities independently across the frequency range in (3.5)–(3.8), we find the worst-case time delay errors as $\tau_{e,VSWR_1} = 3.9$ psec and $\tau_{e,VSWR_2} = 5.9$ psec as shown in Fig. 3.10.

3.1.3 Microstrip Line Dispersion

The time delay error caused by dispersion is due to the change in the effective dielectric constant over frequency and the length of microstrip line in the RF-fanout and TDU-A. Reference [49] provides a method for calculating dispersion of the microstrip line. Following this method for the selected printed circuit board (PCB) substrate (see Section 3.3) provides that the effective dielectric constant, ϵ_{eff}, over the frequency range from 5 GHz to 30 GHz increases monotonically concave up from 3.26 to 3.31, respectively. Hence, the time delay variation over frequency is found

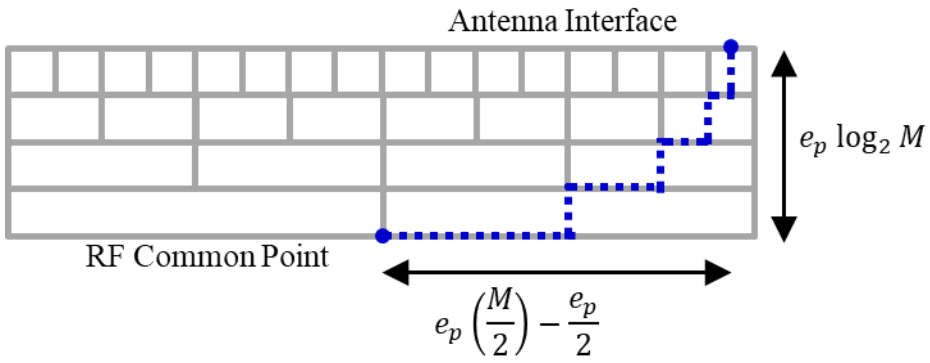

Figure 3.11 Illustration of the allowable area for the corporate feed network implementation pursued for the M=16 element PAA. The dashed path represents the reference distance to the antenna interface.

by calculating the total delay through the RF-fanout at the highest and lowest frequency due to the extremes of the effective dielectric constants. The total microstrip line length through the RF-fanout is due to the combination of three lengths associated with maximum time delay needed to scan the beam towards θ_{max} (d_{scan}), a reference time delay needed to provide a connection from RF common feed point to the antenna element at the edge of the PAA (d_{ref}), and time delay through the power dividers (d_{pd}). It should be noted that the TDUs for this demonstration are delay lines on the PCB. The maximum delay that must be provided by the TDU-A for the linear PAA is calculated based on element spacing and maximum scan angle as

$$d_{scan} = (M-1)\, e_p\, \sin(\theta_{max}) \tag{3.9}$$

where e_p is the element spacing. d_{ref} represents the length of transmission line from RF common port to an antenna element when all TDUs are set to a reference state of 0 (i.e., the array is pointing to boresight). This reference length can be approximated by assuming that the area required at each division level, as defined in [4], has a vertical length of e_p and a horizontal length that starts at e_p at the element level and doubles for each division level moving from the antenna to the RF common feed point. This is demonstrated in Fig. 3.11 where the boxes represent the area for each

division level of the RF-fanout and the dashed line is the reference path distance calculated as

$$d_{ref} = e_p\left(\log_2 M + {}^{M}/_{2} - {}^{1}/_{2}\right). \tag{3.10}$$

The length of the microstrip lines within the dividers depends on the design requirements and implementation choice. The 5 GHz to 30 GHz bandwidth requirement pursued in this chapter necessitates a three stage microstrip line Wilkinson power divider. Since each stage is quarter wavelengths at the center frequency of $f_c = 17.5$ GHz and there are $\log_2 M$ levels of these dividers, total length of the power dividers becomes

$$d_{pd} = 3(\log_2 M)\left(\frac{c}{4f_c}\right) \tag{3.11}$$

where c stands for speed of light. Sum of (3.9)–(3.11) provides the longest length of the microstrip line required as

$$d_{tot} = d_{scan} + d_{ref} + d_{pd}. \tag{3.12}$$

For the $M = 16$ element linear PAA and e_p = 5 mm (i.e. half wavelengths at 30 GHz), equations (3.9)–(3.12) provide d_{scan} = 5.75 cm, d_{ref}= 5.75 cm, d_{pd} = 5.14 cm, and d_{tot} = 16.63 cm. Hence, the effective length of the microstrip line becomes

$$d_{eff}(f) = d_{tot}\sqrt{\epsilon_{eff}(f)} \tag{3.13}$$

with maximum and minimum values attained at the edges of the operation band as $d_{eff} = [30.0, 30.3]$ cm. This distance is subsequently converted into time delay as

$$\tau_{eff}(f) = \frac{d_{eff}(f)}{c} \tag{3.14}$$

which leads to a delay of $\tau_{eff} = [1001, 1009]$ psec. The maximum variation in time delay across the bandwidth is therefore found as $\tau_{disp} = \tau_{eff}(f_{low}) - \tau_{eff}(f_{high}) = 8$ psec.

Table 3.1 Time delay errors

Error Variable	Interval (psec)	Number of Occurrences*	Variable Type
τ_{e,div_1}	± 2.8	1	Random
τ_{e,div_2}	± 5.1	2	Random
τ_{e,div_3}	± 8.2	1	Random
$\tau_{e,VSWR_1}$	± 3.9	1	Random
$\tau_{e,VSWR_2}$	± 5.9	1	Random
τ_{disp}	8	1	Known

* When tracing from the common point to an antenna

3.1.4 Total Delay Error

The total time delay error that must be utilized in optimization algorithm can simply be an additive combination of the worst-case situations determined in the previous section and summarized in Table 3.1. This will yield a total time delay error of 31 psec. However, this is an unlikely occurrence since the errors are a function of frequency and their exact values are not known *a priori*. As an alternative approach for approximating total time delay error, they are considered random and distributed uniformly between their respective $\pm\tau_e$ (i.e., a uniformly distributed probability density function (PDF)).

This assumption can be made because the performances of the individual components are bounded by the requirement, but the actual performance remains unknown until design is completed. Once the design is completed, the actual error may be located anywhere within the specified bound, justifying a uniform distribution assumption. As an example, the requirement for the antenna element discussed in this manuscript is $VSWR \leq 3{:}1$ as stated above; however, the exact value of S_{11}^{ANT} may be at any point within the 3:1 VSWR circle on the Smith Chart over frequency, for example a VSWR of 2:1 is achieved at 15 GHz at 50° scan based on simulations. If

two random variables are independent, then the PDF of their sum is equal to the convolution of their PDFs. Convolving the PDFs of the random variables in Table 3.1 the number of times each occur when tracing a path from the common point to an antenna result in a Gaussian distribution of random errors with a standard deviation of 13.4 psec. As compared to 25.9 psec (excluding dispersion), 13.4 psec is much smaller and can be used to avoid implementation of unnecessary longer states in the TDUs. There is a potential risk when using this approach that a situation may arise that once again the TDU-A does not have the delay range required to steer the beam at extreme angles. However, the probability has been lowered dramatically and it is preferred to use the least amount of delay possible to minimize loss and complexity in the RF-fanout. It is ultimately up to the architect to assess and determine how much time delay error to include in the TDU-A from the Gaussian distribution. We selected the standard deviation for this chapter. Unlike the others, the time delay error due to the dispersion is not random. It is additively combined with the other errors. Therefore, the total time delay error is found as $\tau_{error} = 13.4 + 8 = 21.4$ psec.

3.1.5 TDU-A of a PAA Including Delay Errors

In Chapter 2, it is demonstrated that the problem of optimizing the TDU-A of a linear PAA can be placed into the standard integer linear programming (ILP) form. Key steps of the process are summarized here to show how the time delay error calculated in the previous sections can be introduced into the optimization. Specifically, τ_{error} is added in equation (2.17), which denotes the maximum time delay needed from the first TDU layer TDU_1, as

$$\tau_{max_1} = \frac{h_{scan_1}}{c} + \tau_{error} \tag{3.15}$$

where h_{scan_1} is the scan distance (equation (2.16)) of TDU_1. Following the remainder of the method outlined in Section 2.3 the performance matrix $\boldsymbol{A}$ is filled out for each architecture variant

$$\boldsymbol{A} = [\boldsymbol{a}_{\phi e} \quad \boldsymbol{a}_{1_{msb}} \quad \boldsymbol{a}_{2_{msb}} \quad \boldsymbol{a}_{3_{msb}} \quad \boldsymbol{a}_{4_{msb}}] \tag{3.16}$$

where again $\boldsymbol{a}_{\phi e}$ is the quantization phase error for each architecture variant, and $\boldsymbol{a}_{d_{msb}}$ are the most significant bits (*msbs*) (i.e. the longest time delay bit) of the TDUs at each division level d for each architecture variant where $D = \log_2 M = 4$ is the total number of divisions. The optimization requires constraints for each vector in the $\boldsymbol{A}$ matrix. As explained in Chapter 2, the maximum root mean squared (RMS) quantized phase error is set to $\phi_{max} = 5°$ so the quantization of the TDU-A has a minimal effect on the side lobe levels. The maximum *msb* is calculated based on the area in each division level as shown in Fig. 3.11 (as explained in Section 2.3) by following the method outlined in [4] to find $\tau_{msb_1}^{max} = 376.8$ psec, $\tau_{msb_2}^{max} = 188.4$ psec, $\tau_{msb_3}^{max} = 94.2$ psec and $\tau_{msb_4}^{max} = 47.1$ psec. These values are placed into the constraint vector $\boldsymbol{b}$ as

$$\boldsymbol{b} = [\phi_{max} \quad \tau_{msb_1}^{max} \quad \tau_{msb_2}^{max} \quad \tau_{msb_3}^{max} \quad \tau_{msb_4}^{max}]^T. \tag{3.17}$$

The objective function $\boldsymbol{Kx}$ sets the goal of the optimization, which is to minimize the number of TDUs, the number of bits, and the quantization phase error for the TDU architecture. Hence, $\boldsymbol{Kx}$ can be expressed as

$$\boldsymbol{Kx} = [w_{TDU} \quad w_{bits} \quad w_{\phi}][\boldsymbol{\eta}_{TDU} \quad \boldsymbol{\eta}_{bits} \quad \boldsymbol{a}_{\phi_e}]^T \boldsymbol{x} \tag{3.18}$$

where w_{TDU}, w_{bits}, w_{ϕ} are the weights for the contributions of the TDU count, bit count, and phase error, respectively, $\boldsymbol{\eta}_{TDU}$ is a vector containing the number of TDUs for each architecture variant, $\boldsymbol{\eta}_{bits}$ is a vector containing the number of bits for each architecture variant, and $\boldsymbol{x}$ is a variable vector $\boldsymbol{x} = [x_1, x_2, \dots, x_V]^T$ with V being the total number of architecture variants. In this manuscript, the priority is set to minimize TDU count, which is followed by the bit count, and then the phase error with the weight selection of $[w_{TDU} \quad w_{bits} \quad w_{\phi}] = [1 \quad 0.1 \quad 0.001]$**.** The ILP form for expressing the objective function and constraints of the TDU-A problem is

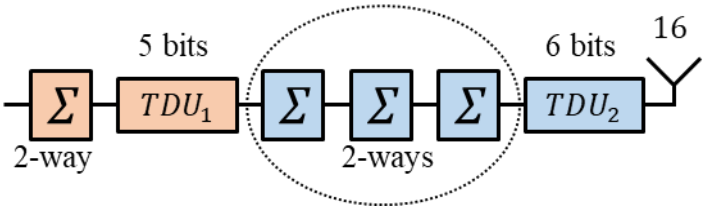

Figure 3.12 Optimized TDU architecture of the 16 element linear PAA where TDU_1 has 5 bits and $\tau_{lsb} = 4.4$ psec and TDU_2 has 6 bits and $\tau_{lsb} = 1.45$ psec.

$$\begin{aligned} &minimize && \boldsymbol{Kx} \\ &subject\ to && \boldsymbol{A}^T\boldsymbol{x} \leq \boldsymbol{b} \\ & && x_1 + x_2 + x_3 + \cdots + x_V = 1 \\ & && x_v = 0\ or\ 1\ \forall\ v = 1, \ldots, V \end{aligned} \tag{3.19}$$

where v is a particular TDU-A architecture variant and the summing constraint, $x_1 + x_2 + x_3 + \cdots + x_V = 1$, along with the integer constraint, $x_v = 0\ or\ 1\ \forall\ v = 1, \ldots, V$, ensures that the solution will be $x_o = 1$, where subscript o stands for the optimum variant, and all other variables are zero. The ILP was run produced the optimal TDU-A shown in Fig. 3.2 and expounded in Fig. 3.12 where TDU_1 has 5 bits with $\tau_{lsb} = 4.4$ psec and TDU_2 has 6 bits with $\tau_{lsb} = 1.45$ psec. Theother parameters found from optimization are $\phi_{max} = 4.52°$, $a_{1_{msb}} = 63.8$ psec, $a_{2_{msb}} = 0$ psec, $a_{3_{msb}} = 0$ psec, and $a_{3_{msb}} = 46.4$ psec.

3.2 Design and Fabrication of a Linear PAA

Three PAAs with static feed networks are pursued for the design, fabrication, and testing of the optimization method. The feed networks are designed for beam steering towards to 0°, 25°, and θ_{max} of 50°. The TDU states for steering the beam towards these scan angles are implemented with fixed length meandered microstrip delay lines (see Appendix A). Other design components are the RF connector transition, Wilkinson power dividers, and antennas. The printed circuit board substrate is Rogers 4003 ($\epsilon_r = 3.55$, $\tan\delta = 0.0027$ at 10 GHz) with $h = 0.203$ mm thickness. The microstrip delay lines were individually simulated with Keysight ADS Momentum to verify

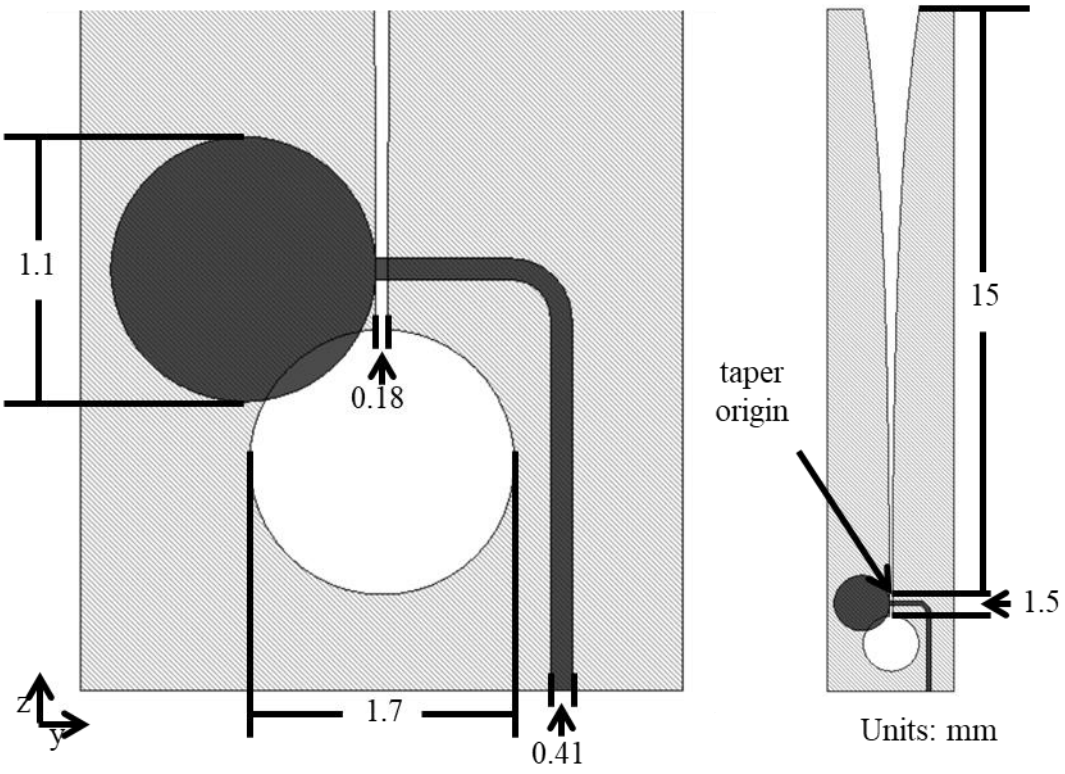

Figure 3.13 Antenna element geometry.

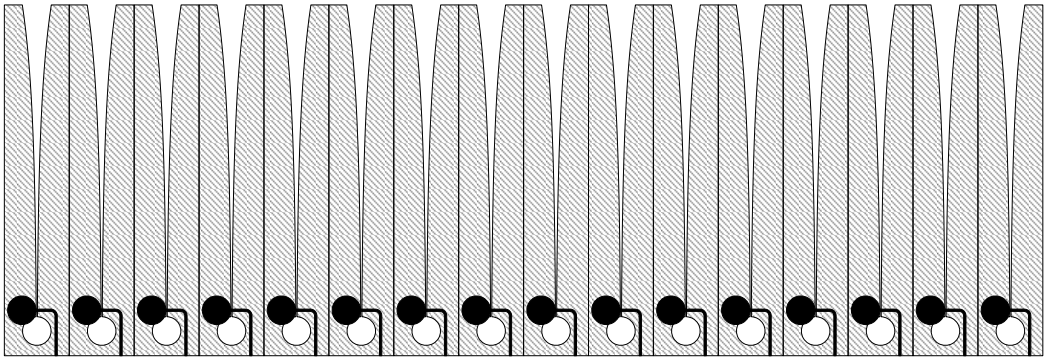

Figure 3.14 A 16 element array model with two terminated elements on both sides to reduce edge effects totaling 20 elements.

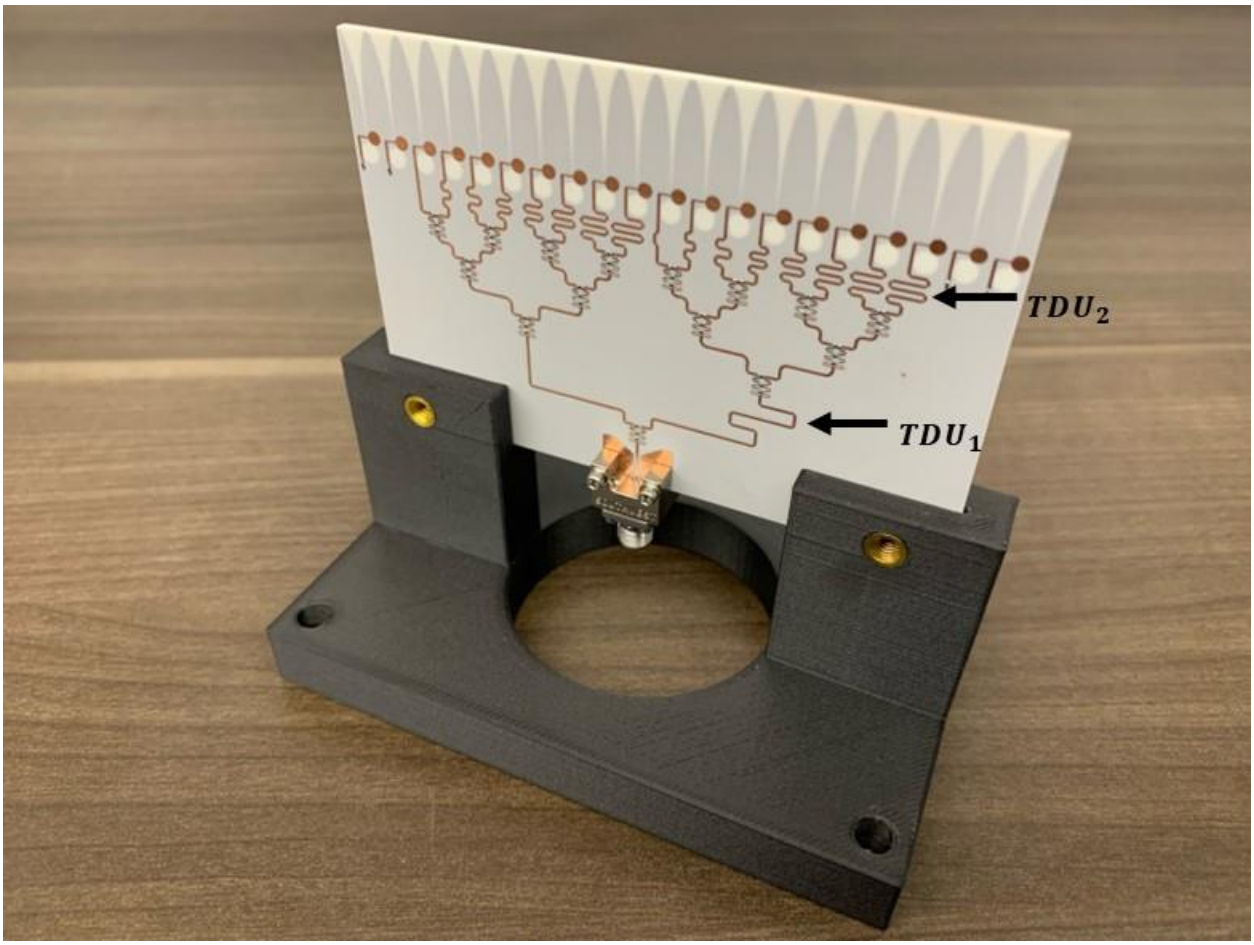

Figure 3.15 Fabricated 16 element linear PAA with feed network implemented for 50° beam steering.

that the required delay and return loss performances are achieved. The Vivaldi antenna was designed and simulated in Ansys Electronics Desktop HFSS to determine the parameters shown in Figs. 3.13 and 3.14. The 16 element PAA for the 50° scan angle is shown in Fig. 3.15 with arrows indicating the layers meandered lines as TDUs. Two additional antenna elements with 50 Ω resistive terminations are added on each side of the PAA to reduce the edge effects for a total of 20 elements. The PAAs are characterized in a far field anechoic chamber as seen in Fig. 3.16.

3.3 Experimental Verification of a Fabricated Linear PAA

Elevation plane radiation pattern measurements are taken from 5 to 30 GHz in 1 GHz steps

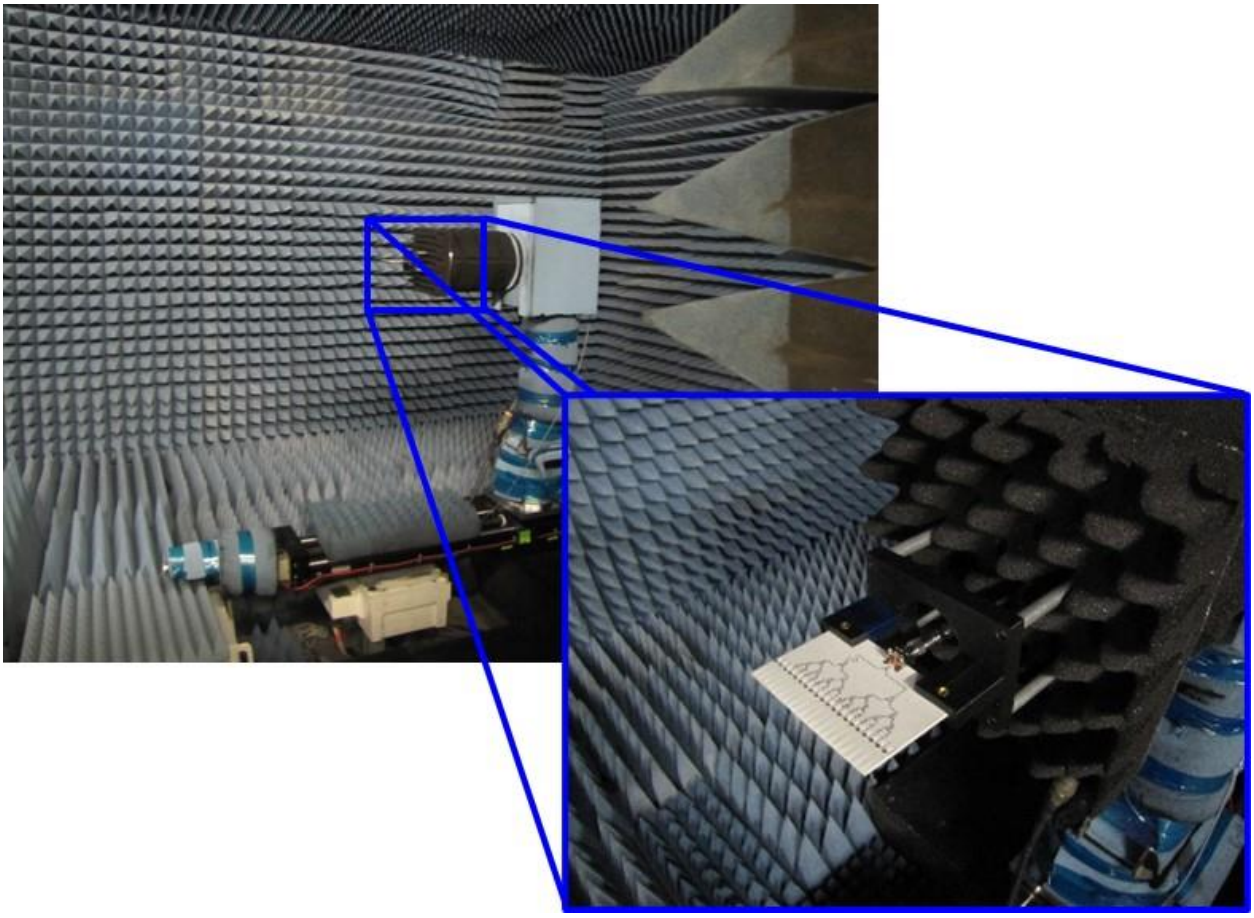

Figure 3.16 16 element PAA with feed network implemented for 0° beam steering during measurement inside an anechoic chamber.

as θ is varying from -90° to 90° in 0.5° step. These patterns are compared to the simulated radiation patterns obtained from PAA model. The model is multiplication of the array factor (AF) with the radiated electric field of the simulated Vivaldi antenna element. The AF is calculated using equations in [1]

$$AF(f_0) = \sum a_i \mathrm{e}^{jk\boldsymbol{r_i}\cdot\hat{\boldsymbol{r}}} \tag{3.20}$$

where $\boldsymbol{r_i}$ is the position vector of the i^{th} antenna element, $\hat{\boldsymbol{r}}$ is the unit vector in the direction of the observation point, $a_i = |a_i|e^{j\phi_{a_i}}$ is the complex weigh of the i^{th} antenna element and f_0 is the frequency at which the AF is being evaluated. For the following examples, we assume a uniform

amplitude distribution with $|a_i| = 1,\ \forall i$ which is approximately true for our hardware demonstration, and the unwrapped phase excitation of each element weighting (i.e., ϕ_{a_i}) is obtained from a search method. The search method begins by finding the ideal phase excitation required as

$$\boldsymbol{\phi_{a_i}} = -k_0 \boldsymbol{r_i} \sin(\theta_{steer}) \tag{3.21}$$

where ϕ_{a_i} is the ideal phase excitation at the i^{th} antenna element, $k_0 = 2\pi/\lambda_0$ is the wavenumber and λ_0 is the wavelength, and θ_{steer} is the desired beam steering direction in degrees. Then we find the ideal delay as

$$\boldsymbol{\tau_{a_i}} = \frac{-\boldsymbol{\phi_{a_i}}}{f_0\ 360}. \tag{3.22}$$

where $\boldsymbol{\tau_{a_i}}$ is the ideal time delay requred at the i^{th} antenna element. The TDUs of each path are configured to provide a total delay at each element to minimize the error between the ideal and the quantized bit selection (See Appendix A). Note that these delay settings are identical across the frequency band of operation (i.e., 5-30 GHz for our example) for a given θ_{steer} due to the UWB nature of the TDU-A. Once TDU settings are found from a frequency of choice, equations (3.20)–(3.22) can be worked backwards to plot AF at any desired frequency. The Vivaldi antenna element is simulated by feeding the 8th element of a 20-element array with all other elements terminated in 50 Ω in order to find the embedded element pattern within the presence of adjacent array elements [1]. The normalized elevation plane radiation patterns obtained from the PAA model without accounting for delay error (i.e., only follwing the method outlined in [47]) are presented in Figs. 3.17, 3.20, and 3.23 as a function of frequency. These pattens clearly show that the true time delay nature of the feed network succesfully ensures that the peak of the radiation pattern is maintained at the desired angle across the UWB frequency. As expected, it is also observed that the beamwidth

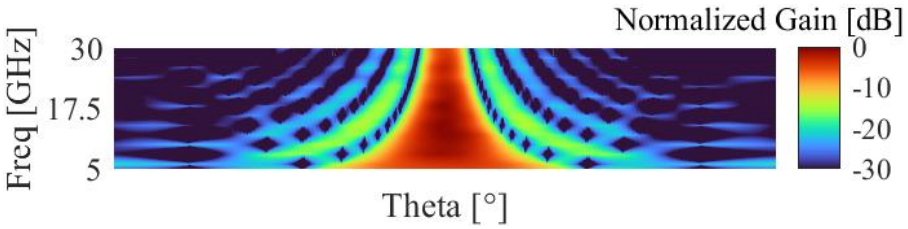

Figure 3.17 Normalized array pattern vs. scan angle and frequency for the TDU-A defined in Fig. 3.12 from model without including delay error steered to 0°.

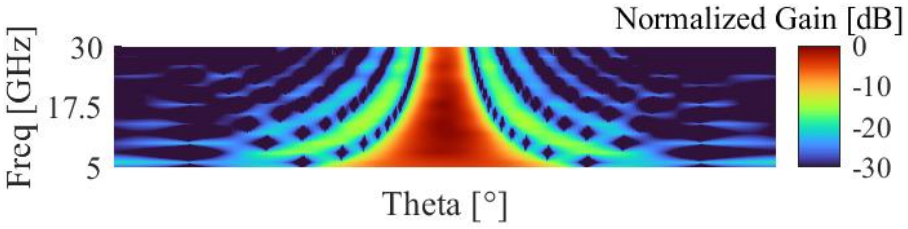

Figure 3.18 Normalized array pattern vs. scan angle and frequency for the TDU-A defined in Fig. 3.12 from model when including delay error steered to 0°.

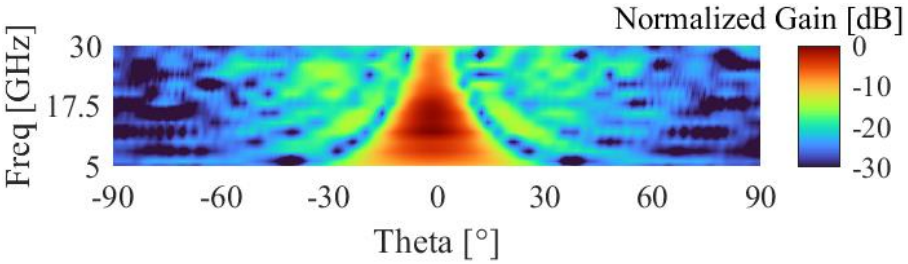

Figure 3.19 Normalized array pattern vs. scan angle and frequency for the TDU-A defined in Fig. 3.12 measured patterns from hardware steering to 0°.

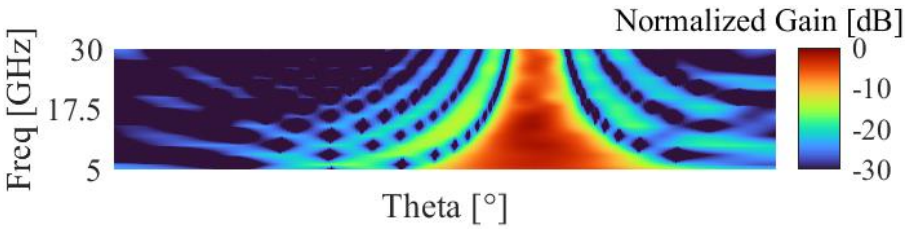

Figure 3.20 Normalized array pattern vs. scan angle and frequency for the TDU-A defined in Fig. 3.12 from model without including delay error steered to 25°.

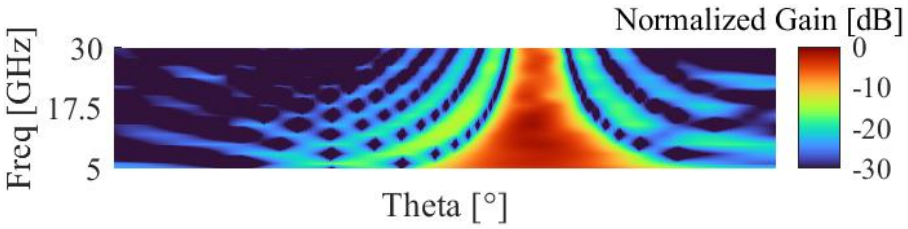

Figure 3.21 Normalized array pattern vs. scan angle and frequency for the TDU-A defined in Fig. 3.12 from model when including delay error steered to 25°.

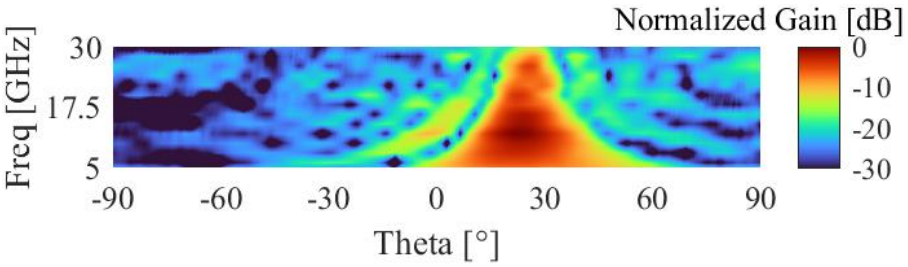

Figure 3.22 Normalized array pattern vs. scan angle and frequency for the TDU-A defined in Fig. 3.12 measured patterns from hardware steering to 25°.

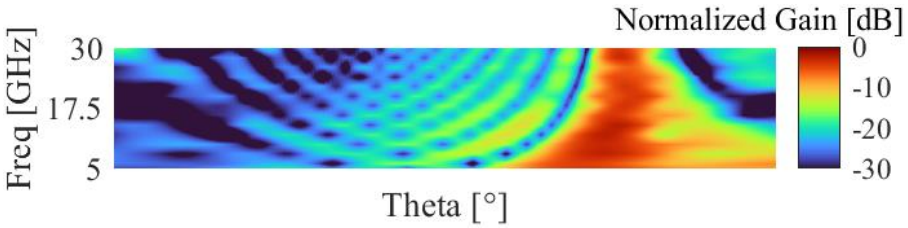

Figure 3.23 Normalized array pattern vs. scan angle and frequency for the TDU-A defined in Fig. 3.12 from model without including delay error steered to 50°.

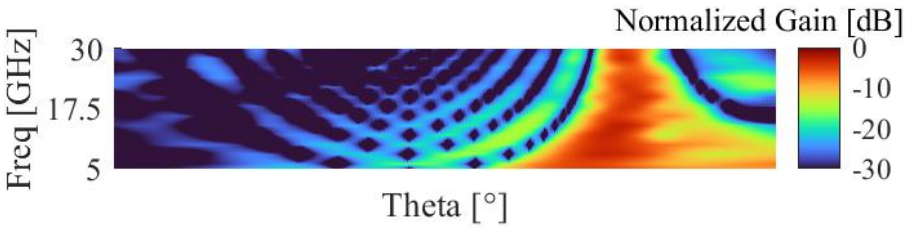

Figure 3.24 Normalized array pattern vs. scan angle and frequency for the TDU-A defined in Fig. 3.12 from model when including delay error steered to 50°.

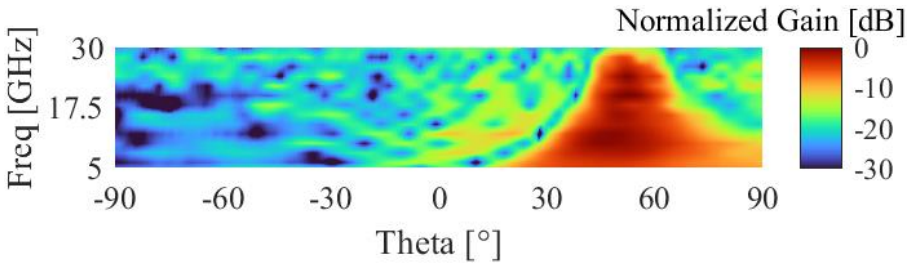

Figure 3.25 Normalized array pattern vs. scan angle and frequency for the TDU-A defined in Fig. 3.12 measured patterns from hardware steering to 50°.

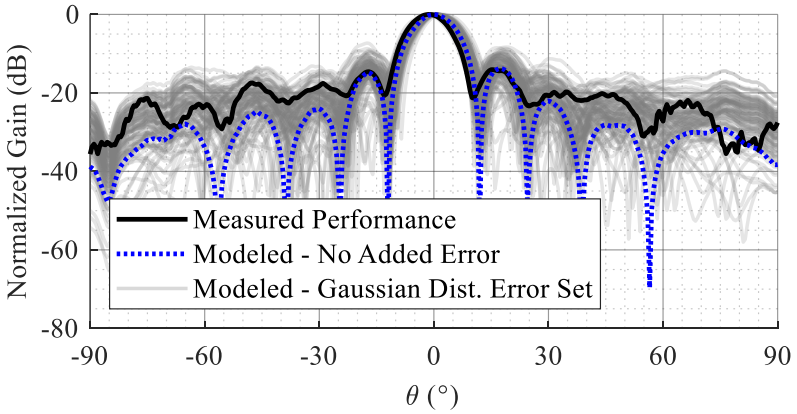

Figure 3.26 Comparison of 18 GHz measurement (bold plots) vs 100 iterations of modeled performance (light gray plots) within the family of expected delay errors in the RF-fanout steered to 0°.

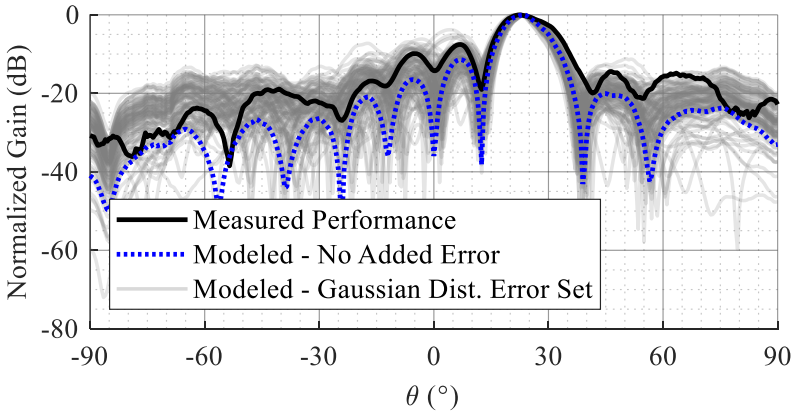

Figure 3.27 Comparison of 18 GHz measurement (bold plots) vs 100 iterations of modeled performance (light gray plots) within the family of expected delay errors in the RF-fanout steered to 25°.

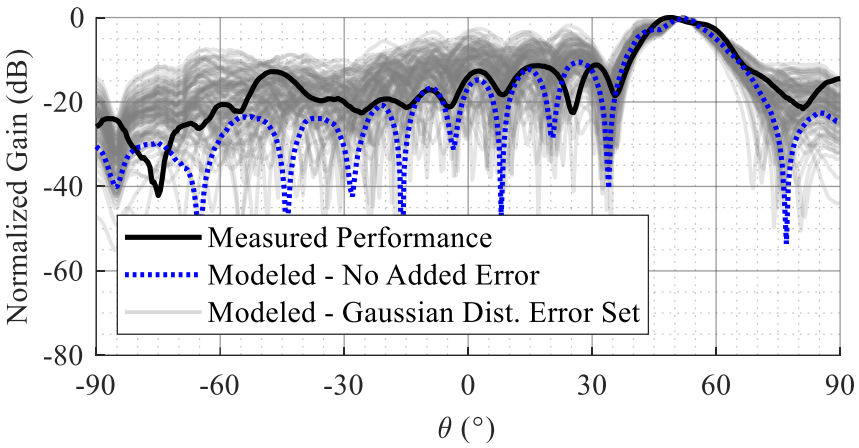

Figure 3.28 Comparison of 18 GHz measurement (bold plots) vs 100 iterations of modeled performance (light gray plots) within the family of expected delay errors in the RF-fanout steered to 50°.

of the radiation pattern decreases with increasing frequency. However, side-lobe degredation at extreme steer angles can be observed in Fig. 3.23 when the array is steered to 50°. The normalized elevation plane radiation patterns obtained from the PAA model with delay errors accounted are presented in Figs. 3.18, 3.21, and 3.24 as a function of frequency. The same characteristics are observed as before, however now the side lobe degredation at extreme steers is no longer present, as expected. The measured normalized radiation patterns from the fabricated PAAs are shown in Figs. 3.19, 3.22, and 3.25. The frequency dependent steering direction and beamwidth characteristics of the measured radiation pattern agrees well with those obtained from the PAA model and the mainbeam beamwidths are nearly identical. On the other hand, the SLL performance is degraded due to the individual components of the TDU-A (i.e., TDUs and dividers) as well as the antenna array being designed independent of each other, since the TDU-A is designed prior to the individual component design, and then stitched together in a final design as well as the loss in the divider network not included in the modeled simulation. The smearing of the measured pattern (i.e., shifts in the side lobe location and amplitude compared to simulation), occurs due to the time

delay errors discussed in Section 3.2 of this dissertation which may be calibrated. The cause of the smearing is illustrated in Figs. 3.26, 3.27, and 3.28 at 18 GHz, approximately the center of the design bandwidth, by comparing the measured results with two sets of PAA models: 1) a pattern with no random error distributed throughout the array (i.e., "Modeled – No Added Error" in Figs. 3.26, 3.27, and 3.28), and 2) a set of 100 array patterns with random errors distributed as a Gaussian PDF across the array elements as defined in Section II. D (i.e., "Modeled – Gaussian Dist. Error Set" in Figs. 3.26, 3.27, and 3.28). The worst case SLL performance is shown in Fig. 3.27 at ~8° which is due to the random stacking of delay errors peaking at 18 GHz and a scan of 25°; however, the performance falls within the set of performance with random errors distributed as predicted. The amplitude variation across the 16-way divider and TDUs was simulated and is approximately ± 0.3 dB at 18 GHz which was determined to be of negligible contribution to the side lobe level performance degradation. An exhaustive set of figures over the entire 5-30 GHz would be impractical in this dissertation, so 18 GHz was chosen as a reperesentation; however, these figures were generated and verified at many other frequencies spaning the entirety of the bandwidth but left out for brevity. Figs. 3.26, 3.27, and 3.28 shows that the measured performance lies within the set of 100 modeled patterns with error distribution showing correlation to predicted performance in Section 3.2. Therefore, the TDU-A has the necessary range to be adjusted and achieve approximately the modeled performance through calibration which is routine for these arrays [19,50-54].

3.4 Linear PAA TDU-A Optimization in Presence of Non-Idealities Conclusions

An approach for including practical time delay errors in the optimization of a UWB PAA feed network to ensure sufficient time delay range at wide scan angles has been introduced and modeled. Specifically, the effects of time delay errors due to frequency dependent variations in

VSWR, divider isolation and load mismatch, and dispersion were calculated and included in the optimization algorithm to determine a robust TDU-A. The efficacy of the method outlined in this manuscript is implemented and verified experimentally by three 16 element linear PAA test articles with an optimized TDU-A operating from 5 GHz to 30 GHz with beams steered towards 0°, 25°, and 50°. The components were designed independently to emulate a representative architecture design, where component characteristics across frequency are not necessarily known *a priori*. Simulated and measured performance demonstrate UWB operation with stable patterns.

Chapter 4: Calibration of Ultra-Wideband Phased Antenna Arrays Fed with Optimized Time Delay Unit Architecture Implementations

Although the discussion in Chapter 2 goes through a comprehensive set of modeling details, time delay errors stemming from practical realization of the feed network is omitted from the discussion. Practical implementations exhibit non-idealities in feed network components such as finiteness of impedance matching, frequency dependent variation in network transfer coefficients, and transmission line dispersion as shown in Chapter 3. Such time delay errors are introduced into the model so that the designed TDU-A exhibit additional – but no more than necessary – delay lengths to compensate the accumulated errors through a time delay calibration procedure.

This chapter demonstrates that the TDU-A optimized by accounting the time delay errors of the non-ideal components within the feed network can be calibrated to obtain the desired radiation pattern from UWB PAAs. Specifically, the 16-element linear PAA in Chapter 3 is considered as a case study for 5-30 GHz operation. Optimal TDU-A is determined for the desired ±50° scan range as shown in Chapter 3 and a feed network is designed for 25° scan with stationary delay lines (but with varying with discrete delay lengths to mimic a realistic reconfigurable implementation). The feed network is full wave simulated to obtain the PAA phase excitations. The operation is repeated for a calibrated feed network to demonstrate side lobe level (SLL) performance of the PAA remains within optimization constraints.

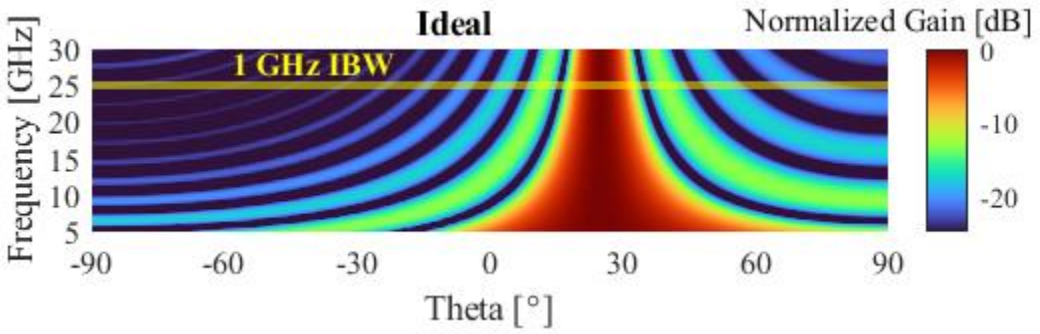

Figure 4.1 Array factor vs frequency of a 16 element array with ideal excitations.

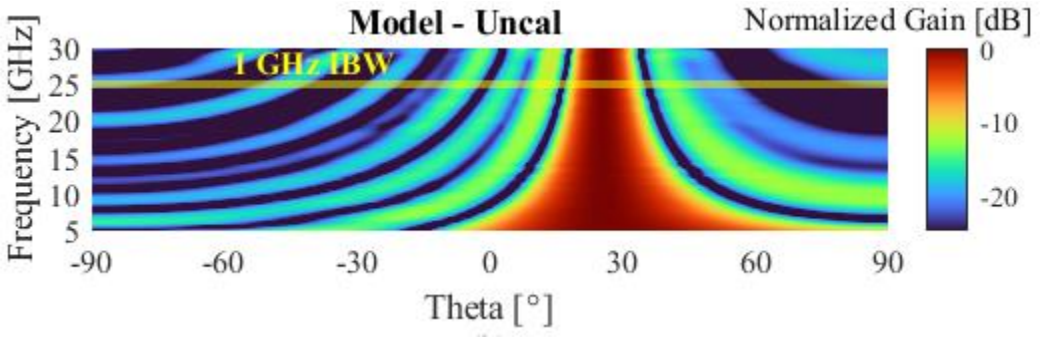

Figure 4.2 Array factor vs frequency of a 16 element array with uncalibrated EM TDU-A simulated excitations.

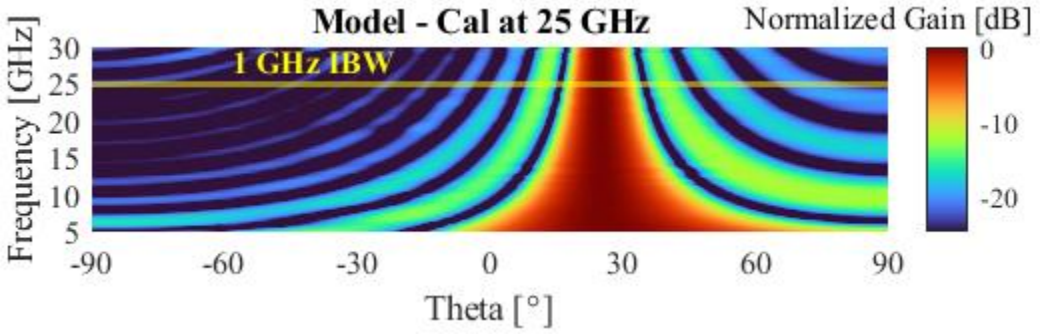

Figure 4.3 Array factor vs frequency of a 16 element array with calibrated EM TDU-A simulated excitations at 25 GHz with a 1 GHz IBW.

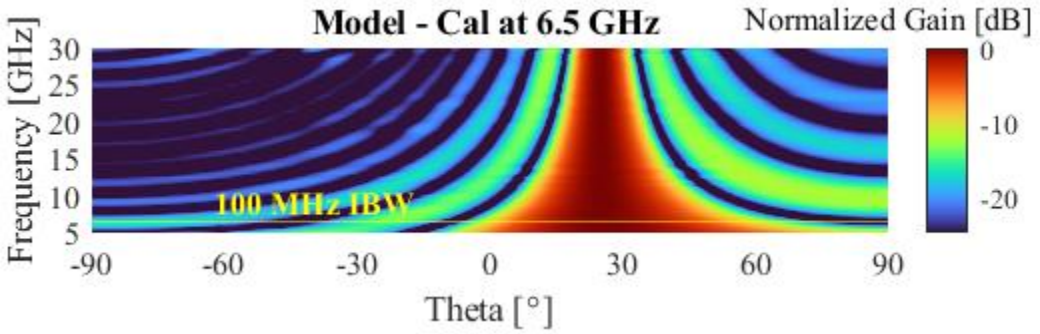

Figure 4.4 Array factor vs frequency of a 16 element array with calibrated EM TDU-A simulated excitations at 6.5 GHz with a 100 MHz IBW.

4.1 Time Delay Unit Architecture Optimization

The PAA is composed of Vivaldi antenna elements in Ansys HFSS as in Chapter 3. For the TDU-A design, the performance matrix of the optimization concatenates the performance variables as $\boldsymbol{A} = [\boldsymbol{a}_{\phi e} \quad \boldsymbol{a}_{1_{msb}} \quad \boldsymbol{a}_{2_{msb}} \quad \boldsymbol{a}_{3_{msb}} \quad \boldsymbol{a}_{4_{msb}}]$ with each variable defined in Chapter 3. The maximum RMS phase error is set to $\phi_{max} = 5°$ to ensure acceptable SLL performance. The maximum most significant bit (msb) is calculated by following the method outlined in [4] to find $\tau_{msb_1}^{max} = 376.8$ psec, $\tau_{msb_2}^{max} = 188.4$ psec, $\tau_{msb_3}^{max} = 94.2$ psec and $\tau_{msb_4}^{max} = 47.1$ psec. These values are placed into the constraint vector, $\boldsymbol{b}$. The objective function $\boldsymbol{Kx}$ sets the goal of the optimization, which is to minimize the number of TDUs, the number of bits, and the quantization phase error for the TDU architecture as shown in Chapters 2 and 3. The ILP algorithm generates the optimal TDU-A shown in Fig. 3.1 where TDU_1 has 5 bits with least significant bit (lsb) $\tau_{lsb} =$ 4.0 psec and TDU_2 has 6 bits with $\tau_{lsb} = 1.5$ psec. The other parameters found from optimization are $a_{\phi_e} = 4.52°$, $a_{1_{msb}} = 63.8$ psec, $a_{2_{msb}} = 0$ psec, $a_{3_{msb}} = 0$ psec, and $a_{3_{msb}} = 46.4$ psec.

4.2 Simulated Results

As an example, a static feed network for the PAA was designed for 25° angle with

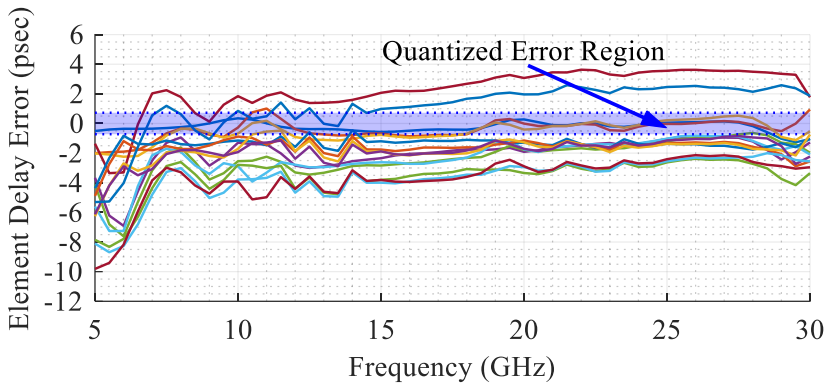

Figure 4.5 Distribution of delay error of the EM simulated TDU-A excitations for each element when compared to an ideal excitation before calibration.

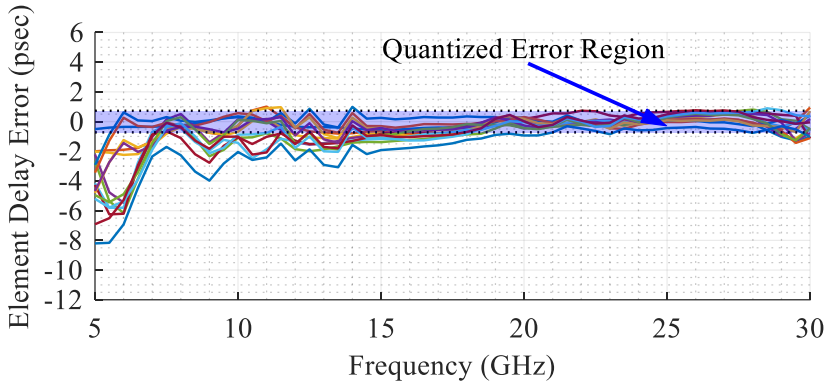

Figure 4.6 Distribution of delay error of the EM simulated TDU-A excitations for each element when compared to an ideal excitation after calibration at 25 GHz with a 1 GHz IBW.

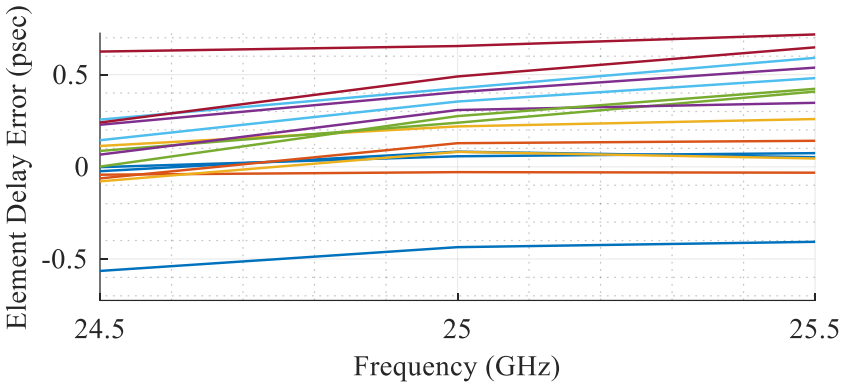

Figure 4.7 Distribution of delay error of the EM simulated TDU-A excitations for each element when compared to an ideal excitation after calibration at 25 GHz zoomed into the calibration window.

microstrip lines on a Rogers 4003 board ($\epsilon_r = 3.55$, $\tan\sigma = 0.002$) using ADS Momentum. The array factor (AF) pattern with ideal element phase excitations to steer the antenna beam to $25°$ is shown in Fig. 4.1 across frequency. Due to the non-idealities of the designed board (such as frequency response of the power dividers), small but notable phase errors are introduced and distributed across the feed network when the TDU-A is realized with microstrip lines. These errors lead to antenna element excitation delays that fall outside the bounds of the quantized error $\pm lsb/2$ (See Chapter 3). The uncalibrated error distribution of the practical RF-fanout and delay elements across every element with the simulated load impedance of the Vivaldi antenna is shown in Fig. 4.5 where each line is the time delay delta between the achieved delay and the ideal delay to steer the beam toward $25°$. Fig. 4.5 shows the spread of delay error fall far outside the quantized error region which leads to degraded SLL performance as shown in Fig. 4.2. The calibration process aims to improve the performance of the delay spread over an instantaneous bandwidth (IBW) within the operational bandwidth (OBW) of the array. As an example, we first take our IBW to be a 1 GHz window and demonstrate calibration centered at 25 GHz (i.e., 24.5-25.5 GHz). A 1 GHz window was selected arbitrarily but is on the order of typical high resolution radar systems [5]. Correction is added to each element feed by increasing or decreasing TDU_2 in Fig. 3.12 by increments of the *lsb* until the center of the 1 GHz IBW is within the quantized error region. This is illustrated in Figs. 4.6 and 4.7 where each element error has been shifted until all errors lie within the calibration window (24.5-25.5 GHz and $\pm lsb/2$). The resulting AF of the calibrated 16 element linear PAA is show in Fig. 4.3 where the side lobe level performance from 24.5 to 25.5 GHz has been dramatically improved such that differences are imperceptible above -26 dB as shown in Fig. 4.3 as expected based on the TDU-A having an RMS quantized error of $5°$. It is worth noting that although the calibration IBW is 1 GHz, the error distribution stays within the

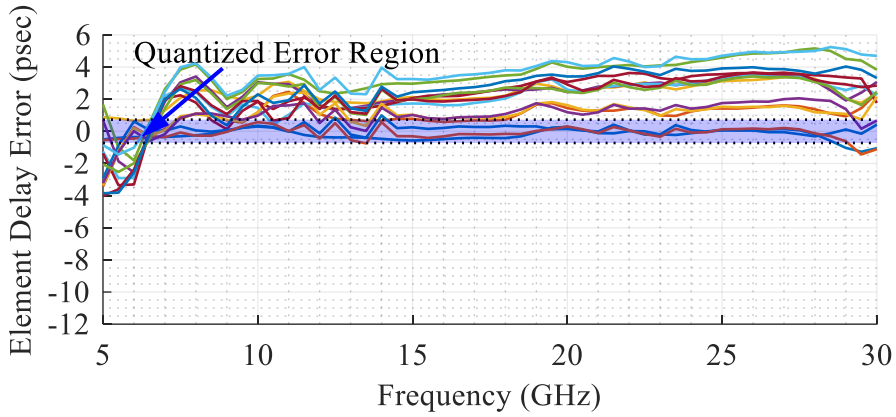

Figure 4.8 Distribution of delay error of the EM simulated TDU-A excitations for each element when compared to an ideal excitation after calibration at 6.5 GHz with a 100 MHz IBW.

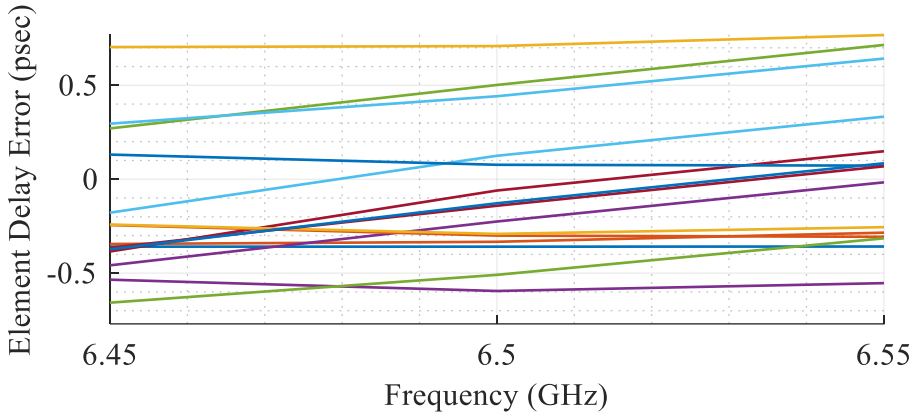

Figure 4.9 Distribution of delay error of the EM simulated TDU-A excitations for each element when compared to an ideal excitation after calibration at 6.5 GHz zoomed into the calibration window.

required quantization window from ~21 GHz to ~28.5 GHz. This means the same calibrated TDU-A configuration settings can be used for a 1 GHz sliding window for this entire frequency range. This is confirmed by comparing the ideal AF pattern of Figs. 4.1 and 4.3 from 21-28.5 GHz where sidelobe degradation are minimal. If, however, we attempt to calibrate at the lower frequencies in this example (i.e., frequencies below 12 GHz), the VSWR ripple dominates, and calibration becomes impossible using this method over such a high percentage bandwidth. Therefore, the IBW

must be decreased to continue employing this method of calibration. Figs. 4.8 and 4.9 demonstrates calibration at 6.5 GHz with a 100 MHz IBW with a corresponding AF plot in Fig. 4.4. It can be observed that the sidelobe performance matches the ideal well beyond the 100 MHz IBW. This is because although we are falling outside the quantized error region of the $lsb/2$ in terms of time, the phase error is smaller at lower frequency and the phase is what impacts the array pattern. For example, the $lsb/2$ quantized error of our example is 0.7 psec which is required so that the RMS phase error at 30 GHz is less than $5°$. Our first calibration example is at 25 GHz which has an RMS phase error of $\phi_e = (lsb/2\sqrt{3})(30 \times 10^9)(360) = 3.8°$. Our second calibration example at 6.5 GHz has an RMS phase error of $\phi_e = (lsb/2\sqrt{3})(6.5 \times 10^9)(360) = 0.98°$ which is significantly lower than the required $5°$. Therefore, relaxation in the LSB precision over frequency can lead to better calibration performance. There are many calibration methods demonstrated in the literature and it is up to the systems architect to determine which best fits the specific applications needs [19,50-54]; however, the aim of this work is to demonstrate that the TDU-A has the required range to calibrate and not a robust method for implementing calibration.

4.3 Calibration Conclusion

A demonstration for calibrating the practical implementation of an optimized 16 element PAA TDU-A has been presented. Deleterious effects caused by non-idealities led to phase excitations outside the quantized error region which degraded side lobe level performance. Through calibration of the TDU-A and RF-fanout, acceptable performance was achieved and demonstrated at $25°$ scan and 25 GHz with an IBW of 1 GHz.

Chapter 5: A General Method for Optimizing Time Delay Unit Architectures of Rectangular Phased Antenna Arrays

The equations provided in Chapter 2 are for 1D PAAs exhibiting power of two total element numbers. They are not readily applicable to 2D PAAs except in the case that the 2D PAA exhibits total element numbers that is a power for two over a square grid. The extension of Chapter 2 into 2D PAAs with elements distributed over a rectangular grid is not trivial and this chapter aims to address this shortcoming. Specifically, this chapter considers the optimization of the TDU-A variants for general rectangular PAAs defined with M elements in the x-direction and N elements the y-direction where M and N are integers that are not necessarily a power of two. Figs. 5.1 and 5.2 demonstrates two TDU-A variants for an $M \times N = 10 \times 6$ element PAA as an example. Sections 5.2-4 demonstrate the development of the optimization problem through the consideration of the 10×6 element PAA shown in Figs. 5.1. Section 5.5 presents a more compelling 256×120 element PAA example to validate the proposed method. In each case, it is shown that the number of TDUs is minimized while achieving the desired performance criteria.

5.1 TDU Architecture Variants of an Arbitrary 2D Rectangular PAA

Optimizing the TDU-A of the PAA begins by defining the relationship between each TDU-A variant and the number of TDUs and bits. This relationship is shown in Chapter 2 for a 1D linear PAA, however the method is not readily extendable to 2D PAAs. This section proposes a general method to represent the TDU-A variants. We define $[\boldsymbol{\Psi}]$ and $[\boldsymbol{T}]$ to track the number of branches and TDUs at each division level of the RF fanout, respectively, and $[\boldsymbol{B}]$ to track the number of bits on each TDU layer. For the 2D PAA, the power division happens differently in *x*- and *y*-

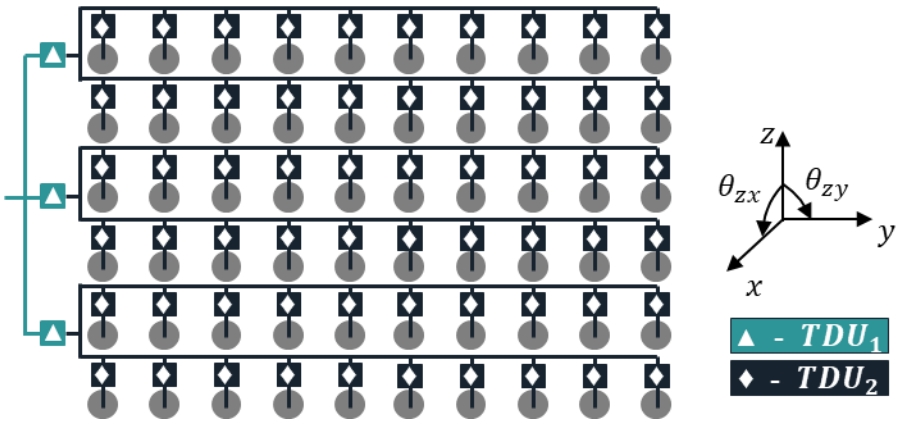

Figure 5.1 Demonstrating the TDU-A for a 10×6 PAA graphically for configuration vector $\boldsymbol{\Lambda}(2,2,4,5,7)$ or $[\boldsymbol{\Upsilon}]_{v=1177,:}$.

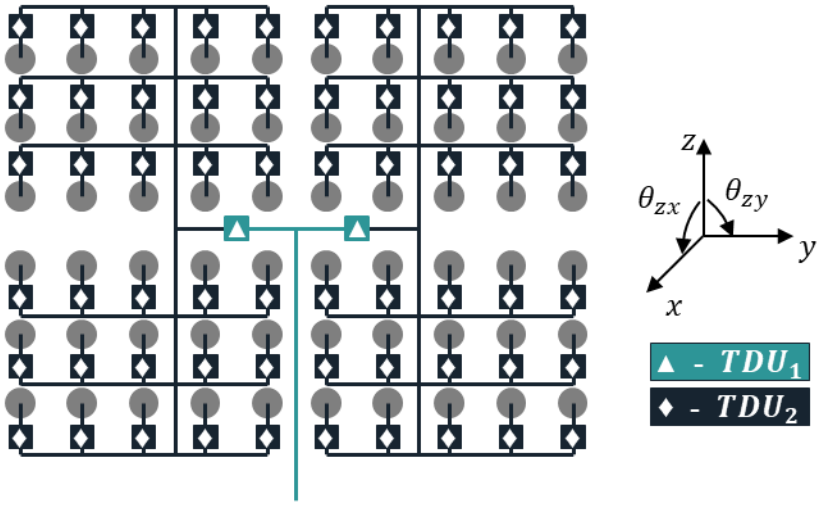

Figure 5.2 Demonstrating the TDU-A for a 10×6 PAA graphically for configuration vector $\boldsymbol{\Lambda}(1,1,5,4,7)$ or $[\boldsymbol{\Upsilon}]_{v=250,:}$.

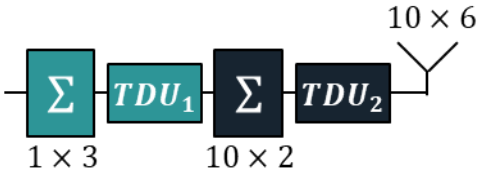

Figure 5.3 TDU-A schematic corresponding to Fig. 5.1.

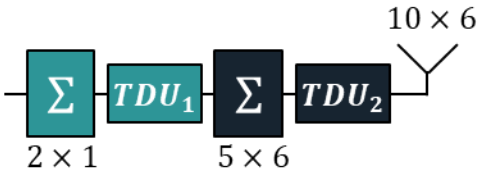

Figure 5.4 TDU-A schematic corresponding to Fig. 5.2.

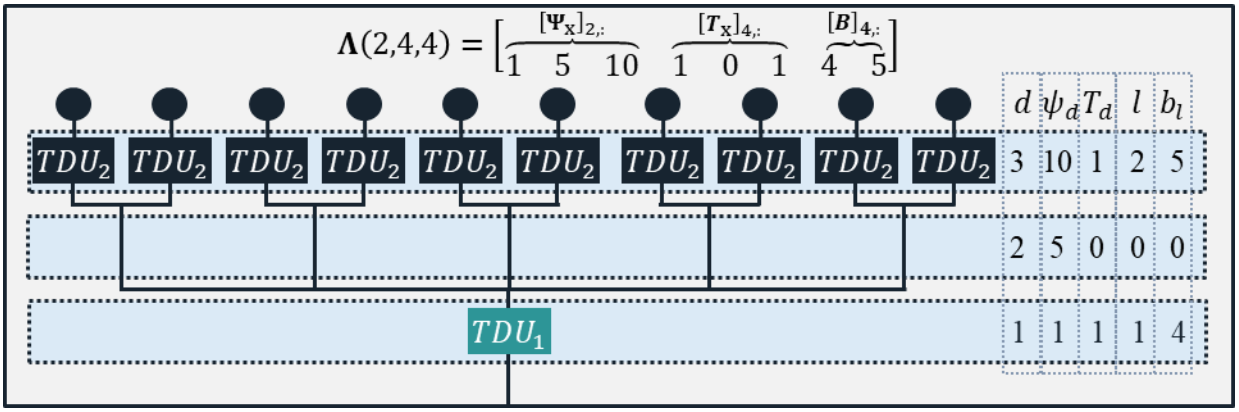

Figure 5.5 Architecture variant examples for a $D_x = 3$ division level 10 element PAA with a 5-way divider followed by a 2-way divider with a 4 bit TDU layer in $d = 1$ and 5 bit TDU layer in $d = 3$ with no TDUs in $d = 2$.

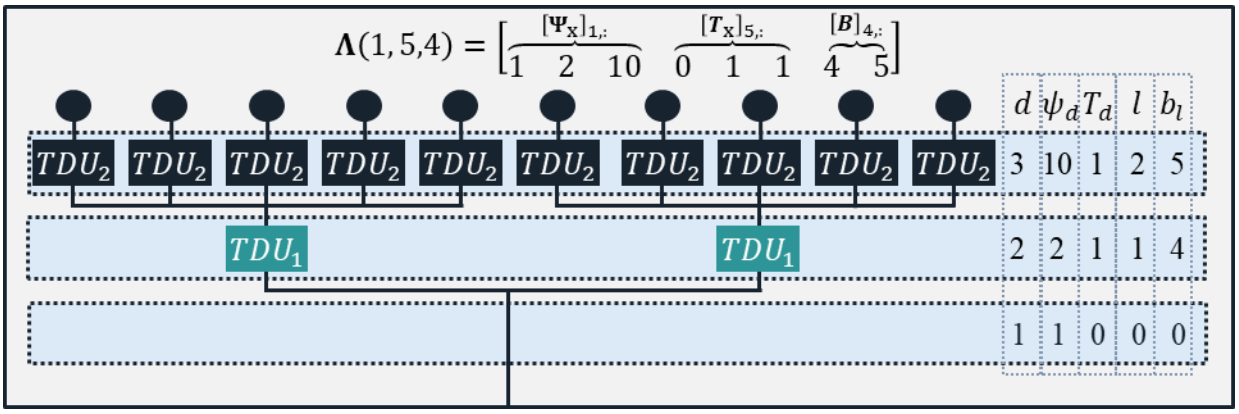

Figure 5.6 Architecture variant examples for a $D_x = 3$ division level 10 element PAA with a 2-way divider followed by a 5-way divider with a 4 bit TDU layer in $d = 2$ and 5 bit TDU layer in $d = 3$ with no TDU in $d = 1$.

dimensions depending on M and N. Hence, $[\boldsymbol{\Psi}]$ and $[\boldsymbol{T}]$ matrices will be different for power division along the two dimensions. On the other hand, the matrices in one dimension are not dependent on the matrices in the other dimension and are therefore separable. To that end, we will carry an illustration of the x-dimension of Figs. 5.1 and 5.2 in Fig. 5.5 and 5.6 through Sections 5.2.1-3 and then combine the results with the y-dimension matrices to yield the TDU-A configuration vector, $\boldsymbol{\Lambda}$ in Section II.D. The notation used throughout this chapter for matrix indexing is $[\boldsymbol{A}]_{i,j}$ where i and j are the row and column indices. A colon in either indexing position is used to represent all entries in that dimension (i.e., $[\boldsymbol{M}]_{i,:}$ is the i^{th} row vector of $[\boldsymbol{M}]$).

5.1.1 Setting Up the $[\boldsymbol{\Psi}]$ Matrices

The $[\boldsymbol{\Psi}]$ matrix tracks the number of branches at each division level within the RF-fanout, which was not required or addressed in Chapter 2. The formulation shown in Chapter 2 can only handle linear arrays that are powers of two. Therefore, no variations in the division configuration exist between architecture variants. To make a general optimization algorithm, element values with multiple unique division levels must be handled. To illustrate the limitation of Chapter 2, a linear PAA with 8 elements will require 3 division levels of identical 2-way dividers in the RF-fanout and can readily be handled by the formulated method. However, given a linear PAA with 12 elements, the RF-fanout requires two 2-ways and one 3-way and the order in which these dividers are configured (i.e., 2-way followed by 2-way followed by 3-way, or 2-way followed by 3-way followed by 2-way) will change the TDU-A performance depending on which division level the TDUs are located which cannot be optimized using Chapter 2. To address this need, we begin by generating a vector that represents the number of divisions at each stage of the RF-fanout by finding the prime factorizations of M and N and call this $\boldsymbol{m}$ and $\boldsymbol{n}$, respectively, such that

$$\boldsymbol{m} = factor(M) \tag{5.1a}$$

$$\boldsymbol{n} = factor(N) \tag{5.1b}$$

where $factor(x)$ generates a prime factorization vector of a scalar x. In the 10×6 PAA, the vectors are $\boldsymbol{m} = [2 \quad 5]$ and $\boldsymbol{n} = [2 \quad 3]$ which implies in the x-dimension there is a 2-way followed by a 5-way (i.e., the RF-fanout in Fig. 5.6) and in the y-dimension, there is a 2-way followed by a 3-way. However, there are multiple permutations of the divider configurations which must be considered during optimization. For example, in the x-dimension the 5-way could come first followed by the 2-way (i.e., the RF-fanout in Fig. 5.5) which changes the TDU-A performance. While optimizing the array, any potential permutations of dividers in the x- and y-dimensions must be considered so we define an operator $P(\boldsymbol{x})_v$ which represents the vth unique permutation of a vector $\boldsymbol{x}$**.** The 10×6 element PAA example has a total of $V_{\Psi_x} = V_{\Psi_y} = 2$ unique permutation variants in the x- and y- dimensions which are $P(\boldsymbol{m})_1 = [2 \quad 5]$, $P(\boldsymbol{m})_2 = [5 \quad 2]$, $P(\boldsymbol{n})_1 = [2 \quad 3]$, and $P(\boldsymbol{n})_2 = [3 \quad 2]$. Finally, to track the number of branches on each division level, we must generate the cumulative product of each unique permutation, such that the $[\boldsymbol{\Psi}]$ matrix is

$$[\boldsymbol{\Psi}] = \begin{bmatrix} 1 & C\left(P(\boldsymbol{x})_{v\Psi=1}\right) \\ \vdots & \vdots \\ 1 & C\left(P(\boldsymbol{x})_{v\Psi=V\Psi}\right) \end{bmatrix} \tag{5.2}$$

where the notation $C(\boldsymbol{x})$ denotes the cumulative product of a vector $\boldsymbol{x}$. Note the column of 1's which represents the common point of the RF-fanout for each variant. Returning to our 10×6 element PAA demonstration, we find the $[\boldsymbol{\Psi}]$ matrices in the x- and y-dimensions as

$$[\boldsymbol{\Psi}_x] = \begin{bmatrix} 1 & 2 & 10 \\ 1 & 5 & 10 \end{bmatrix} \; [\boldsymbol{\Psi}_y] = \begin{bmatrix} 1 & 2 & 6 \\ 1 & 3 & 6 \end{bmatrix}$$

where each row shows the number of branches, ψ_d, at each level of division, d, and there are $D_x = 3$ division levels in $[\boldsymbol{\Psi}_{\mathrm{x}}]$ and $D_y = 3$ division levels in $[\boldsymbol{\Psi}_{\mathrm{y}}]$ as seen by the number of columns in

the $[\boldsymbol{\Psi}]$ matrices. Fig. 5.6 demonstrates the first row of $\boldsymbol{\Psi}_x$ (i.e., $[\boldsymbol{\Psi}_x]_{1,:}$) where $d = 1$ is the common point so there is one branch (i.e., $\psi_1 = 1$) followed by $d = 2$ with a 2-way that generates two branches (i.e., $\psi_2 = 2$) and finally at $d = 3$ there are two 5-ways for a total of 10 branches (i.e., $\psi_3 = 10$). Fig. 5.5 demonstrates the second row of $\boldsymbol{\Psi}_x$ (i.e., $[\boldsymbol{\Psi}_x]_{2,:}$) where $\psi_1 = 1$, $\psi_2 = 5$, and $\psi_3 = 10$.

5.1.2 Setting Up the $[\boldsymbol{T}]$ Matrices

Next, we define $[\boldsymbol{T}]$ to track all potential TDU placements in the 2D PAA RF-fanout. As stated in Chapter 2 each division level can have no TDUs (i.e., $T_d = 0$), a single layer of TDUs (i.e., $T_d = 1$) or cascaded layers of TDUs (i.e., $T_d = 2, 3, \ldots L$) where L denotes the total number of TDU layers that will be employed within the RF-fanout. A layer of TDUs, TDU_l ($l = 1, .., L$), consists of ψ_d identical TDUs placed at each branch in the division level of an RF-fanout. Placement of these TDU layers create different architecture variants. To illustrate this, we return to the example in Fig. 2 which shows two unique architecture variants for the x-dimension 10-element PAA with $D = 3$ when $L = 2$ TDU layers are employed. In Fig. 5.6, TDU_1 is placed on $d = 2$ level and TDU_2 is placed on $d = 3$ level. Placement in Fig. 5.6 implies $T_1 = 0$, $T_2 = 1$, and $T_3 = 1$. In Fig. 5.5, TDU_1 and TDU_2 are on $d = 1$ and $d = 3$ levels, so that $T_1 = 1$, $T_2 = 0$, and $T_3 = 1$. The total number of architecture variants due to the placement of TDU layers within division levels of the RF-fanout (V_T) is shown in [17] as

$$V_T = \frac{(L+1)^{\overline{(D-1)}}}{(D-1)!} \tag{5.3}$$

where L is the total number of TDU layers in the RF-chain and the notation $x^{\bar{n}}$ denotes a rising factorial where $x^{\bar{n}} = x(x+1) \ldots (x+n-1)$. For Fig. 5.2, $L = 2$ and $D = 3$ lead to $V_T = 6$. Equation (5.3) grows exponentially with number of layers and division level. In each row of the

$\boldsymbol{T}$ matrix, the sum of the columns is L since this defines the total number of TDU layers. This can be seen in Figs. 5.5 and 5.6 where in both cases $T_1 + T_2 + T_3 = 2$. Therefore, $\boldsymbol{T}$ is a matrix with V_T rows and D columns containing every combination of rows whose summation adds to L or

$$\sum_{d=1}^{D} [\boldsymbol{T}]_{v_T,d} = L, \quad v_{\mathrm{T}} = 1, 2, \ldots V_{\mathrm{T}}. \tag{5.4}$$

The 10×6 PAA has $D_x = D_y = 3$, $L = 2$, $V_{T_{\mathrm{x}}} = V_{T_{\mathrm{y}}} = 6$, and

$$[\boldsymbol{T}_x] = \left[\boldsymbol{T}_y\right] = \begin{bmatrix} 2 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 2 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 & 2 \end{bmatrix}^T$$

where each row after transposing is a variant of the TDU configurations in the RF-fanout (i.e., v_{T_x} and v_{T_y}). Fig. 5.6 demonstrates the fifth row of $[\boldsymbol{T}_x]$ (i.e., $[\boldsymbol{T}_x]_{5,:}$), and Fig. 5.5 demonstrates $[\boldsymbol{T}_x]_{4,:}$.

5.1.3 Setting Up the $[\boldsymbol{B}]$ Matrices

The final matrix we must define is $[\boldsymbol{B}]$ which tracks the number of bits employed at each TDU layer. Following the method in Chapter 2, the parameter b_l $(l = 1, .., L)$ represents the number of bits used in implementing the TDU on the l^{th} layer (i.e., TDU_l). Since minimizing the bit count is important, flexibility in bit counts should be provided during optimization. To do so, we set $b_l \in [b_{min}, b_{max}]$ where b_{min} and b_{max} represent the minimum and maximum number of bits allowed in the architecture, respectively. Consequently, the number of architecture variants due to the allowable bits in the TDUs becomes

$$V_B = (b_{max} - b_{min} + 1)^L . \tag{5.5}$$

The $[\boldsymbol{B}]$ matrix has V_B rows to contain every combination bit count for each TDU layer and has L total columns. For simplicity, let us set $b_{max} = 6$ and $b_{min} = 4$ for the 10×6 element PAA example such that $V_B = 9$ and

$$[\boldsymbol{B}] = \begin{bmatrix} 4 & 5 & 6 & 4 & 5 & 6 & 4 & 5 & 6 \\ 4 & 4 & 4 & 5 & 5 & 5 & 6 & 6 & 6 \end{bmatrix}^T$$

where each row after transposing is a variant of the TDU bit configurations in the RF-fanout (i.e., v_B). Architectures shown in Fig. 5.5 and 5.6 demonstrates the fourth row of $[\boldsymbol{B}]$ (i.e., $[\boldsymbol{B}]_{4,:}$).

5.1.4 Creating the TDU-A Configuration Vector $\boldsymbol{\Lambda}$ and Variant Matrix, $[\boldsymbol{\Upsilon}]$

The matrices generated in Sections 5.2.1-3 must be placed into a format that is easily digestible by the ILP in Section IV, called the variant matrix. In Algorithm 2.1, the variant matrix was generated by cycling through many potential $[\boldsymbol{T}]$ and $[\boldsymbol{B}]$ matrices while only accepting architectures that meet certain criteria into the variant matrix. This process is computationally expensive, especially in extremely large arrays. Since Chapter 2 only focuses on linear arrays with element counts which are powers of two, there are significantly fewer potential variations, and therefore significantly less iterations when generating the variant matrix compared to following the same method for a 2D array. As an illustration, assume a linear PAA with $b_{min} = 4$ and $b_{max} = 5$ and $L = 2$ layers of TDUs. An 8-element PAA requires 109 cycles through Algorithm 2.1 to generate the $V = 24$ acceptable TDU-A variants, an acceptance rate of 22%. However, a 128 element PAA requires 8749 cycles through Algorithm 2.1 to generate the 113 acceptable TDU-A variants, which is an acceptance rate of 1.3%. Therefore, given constant bit range and TDU layer requirements, a larger number of elements will yield significantly larger cycles and lower acceptance rates than lower element counts. However, larger arrays require additional layers and larger bit ranges to find the optimal TDU-A. Changing $b_{min} = 2$ and $b_{max} = 6$ with $L = 3$ for the 128 element linear PAA yields 10,501 acceptable TDU-A variants of 2,048,00 cycles through Algorithm 2.1. Expanding this to a 2D array exacerbates the issue. A 128×64 element PAA with $b_{min} = 2$ and $b_{max} = 6$ with $L = 3$ yields 588,000 acceptable TDU-A variants of ~8.4 billion cycles which does not include the added complexity of the $[\boldsymbol{\Psi}]$ matrix since 128 and 64 are

powers of two which was selected intentionally since Algorithm 2.1 cannot accommodate RF-fanouts with multiple unique divisions. Therefore, a more efficient algorithm is required to generate the variant matrix of these significantly more complex general 2D PAAs. We begin by generating a configuration vector, $\mathbf{\Lambda}$. All unique TDU-As for an $M \times N$ PAA can be configured by concatenating single rows selected from the $[\boldsymbol{\Psi}]$, $[\boldsymbol{T}]$, and $[\boldsymbol{B}]$ matrices to form the configuration vector as

$$\mathbf{\Lambda}\left(v_{\Psi_x}, v_{\Psi_y}, v_{T_x}, v_{T_y}, v_B\right) = \left[[\boldsymbol{\Psi}_{\mathrm{x}}]_{v_{\Psi_x},:}\ \left[\boldsymbol{\Psi}_{\mathrm{y}}\right]_{v_{\Psi_y},:}\ [\boldsymbol{T}_{\mathrm{x}}]_{v_{T_x},:}\ \left[\boldsymbol{T}_{\mathrm{y}}\right]_{v_{T_y},:}\ [\boldsymbol{B}]_{v_B,:}\right]. \tag{5.6}$$

To demonstrate, we return to the 10 element linear PAA in Figs. 5.5 and 5.6 and create the TDU-A configuration vector for the architecture in Fig. 5.6 as

$$\mathbf{\Lambda}(1,5,4) = \left[\overbrace{1\ 2\ 10}^{[\boldsymbol{\Psi}_{\mathrm{x}}]_{1,:}}\ \overbrace{0\ 1\ 1}^{[\mathbf{T}_{\mathrm{x}}]_{5,:}}\ \overbrace{4\ 5}^{[\mathbf{B}]_{4,:}}\right]$$

and the TDU-A configuration vector for Fig. 5.5 as

$$\mathbf{\Lambda}(2,4,4) = \left[\overbrace{1\ 5\ 10}^{[\boldsymbol{\Psi}_{\mathrm{x}}]_{2,:}}\ \overbrace{1\ 0\ 1}^{[\mathbf{T}_{\mathrm{x}}]_{4,:}}\ \overbrace{4\ 5}^{[\mathbf{B}]_{4,:}}\right].$$

Note that we are only showing the x-dimension in Figs. 5.5 and 5.6 and therefore $\left[\boldsymbol{\Psi}_y\right]$ and $\left[\mathbf{T}_y\right]$ were eliminated from $\mathbf{\Lambda}(1,5,4)$ and $\mathbf{\Lambda}(2,4,4)$ above to demonstrate how $\mathbf{\Lambda}$ corresponds to a realized architecture. Finally, we are able to demonstrate a 2D configuration vector by returning to our 10×6 PAA example and selecting two configuration vectors

$$\mathbf{\Lambda}(1,1,5,4,7) = \left[\overbrace{1\ 2\ 10}^{[\boldsymbol{\Psi}_{\mathrm{x}}]_{1,:}}\ \overbrace{1\ 2\ 6}^{[\boldsymbol{\Psi}_{\mathrm{y}}]_{1,:}}\ \overbrace{0\ 1\ 1}^{[\mathbf{T}_{\mathrm{x}}]_{5,:}}\ \overbrace{1\ 0\ 1}^{[\mathbf{T}_{\mathrm{y}}]_{4,:}}\ \overbrace{4\ 6}^{[\mathbf{B}]_{7,:}}\right]$$

$$\mathbf{\Lambda}(2,2,4,5,7) = \left[\overbrace{1\ 5\ 10}^{[\boldsymbol{\Psi}_{\mathrm{x}}]_{2,:}}\ \overbrace{1\ 3\ 6}^{[\boldsymbol{\Psi}_{\mathrm{y}}]_{2,:}}\ \overbrace{1\ 0\ 1}^{[\mathbf{T}_{\mathrm{x}}]_{4,:}}\ \overbrace{0\ 1\ 1}^{[\mathbf{T}_{\mathrm{y}}]_{5,:}}\ \overbrace{4\ 6}^{[\mathbf{B}]_{7,:}}\right]$$

which are demonstrated by the TDU-A variants shown in Figs. 5.1 and 5.2. Each divider in Figs. 5.3 and 5.4 are configured as $X \times Y$ dividers where X is the number of divisions in the x-dimension

and Y is the number of divisions in the y-dimension. In Fig. 5.2, there is a 2×1 way divider before TDU_1 and a 5×6 way divider before TDU_2 shown schematically in Fig. 5.4. In Fig. 5.1 there is a 1×3 way divider before TDU_1 and a 10×2 way divider before TDU_2 shown schematically in Fig. 5.3. The total number of TDU-A variants, V, is found by considering every row configuration of the $[\boldsymbol{\Psi}]$, $[\boldsymbol{T}]$, and $[\boldsymbol{B}]$ matrices in $\boldsymbol{\Lambda}$ so that

$$V_{\Upsilon} = V_{\Psi_x} V_{\Psi_y} V_{\mathrm{T}_x} V_{\mathrm{T}_y} V_B. \tag{5.7}$$

There are $V_{\Upsilon} = 2 \times 2 \times 6 \times 6 \times 9 = 1296$ TDU-A variants in our 10×6 element PAA example. The configuration vector is transformed to a variant matrix, $\boldsymbol{\Upsilon}$, using Algorithm 5.1 shown below to be used later in the optimization. Following Algorithm 5.1, we find that $[\boldsymbol{\Upsilon}]_{v_{\Upsilon}=1177,:}$ and $[\boldsymbol{\Upsilon}]_{v_{\Upsilon}=250,:}$ are the rows of $[\boldsymbol{\Upsilon}]$ that produces the configuration vector shown in Figs. 5.1 and 5.2, respectively.

Algorithm 5.1 Generation of Variant Matrix

$v = v_{\Psi_x} = v_{\Psi_y} = v_{T_x} = v_{T_y} = v_T = 0;$
for $v_{\Psi_x} \leq V_{\Psi_x}$; for $v_{\Psi_y} \leq V_{\Psi_y}$;
  for $v_{\mathrm{T}_x} \leq V_{\mathrm{T}_x}$; for $v_{\mathrm{T}_y} \leq V_{\mathrm{T}_y}$;
    for $v_B \leq V_{\mathbf{T}_x}$
      $[\boldsymbol{\Upsilon}](v_{\Upsilon}, :) = \boldsymbol{\Lambda}\left(v_{\Psi_x}, v_{\Psi_y}, v_{T_x}, v_{T_y}, v_B\right)$
      $v_{\Upsilon} = v_{\Upsilon} + 1;$
end; end; end; end; end;

5.1.5 Calculating TDU and Bit Count

Each TDU-A variant, $v_{\Upsilon,}$ for an $M \times N$ PAA requires a certain number of TDUs and bits which can be calculated using the information found in the configuration vector, $\boldsymbol{\Lambda}$. The number of TDUs and bits in $[\boldsymbol{\Upsilon}]_{v_{\Upsilon}=250,:}$ of our 10×6 PAA in Fig. 5.2 can be found by observation. There is a 2×1 way divider before TDU_1 leading to 2 TDUs on $l = 1$, each with 4 bits for a total of 8 bits. Following the 2×1 way divider there is a 5×6 way divider before TDU_2 leading to 60 TDUs on $l = 2$, each with 6 bits for a total of 360 bits. So, the total number of TDUs is 62 and the

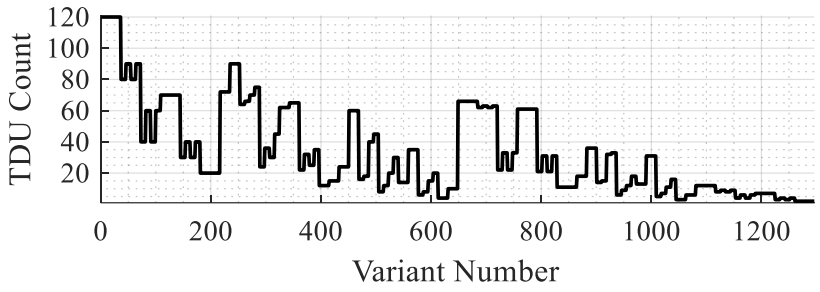

Figure 5.7 TDU count vs variant number of the 10×6 element PAA.

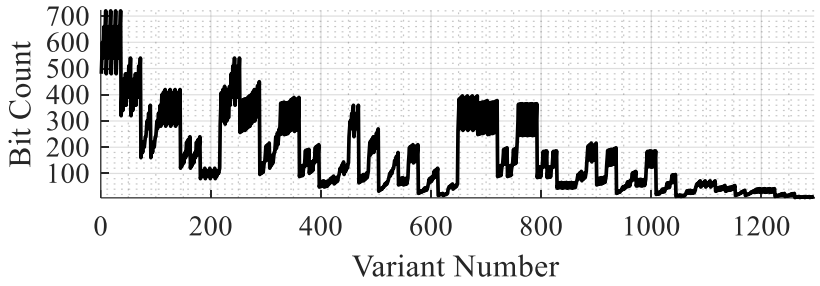

Figure 5.8 Bit count vs variant number of the 10×6 element PAA.

total number of bits is 368. Through this exercise, we can see that the total number of TDUs for each variant, v, is found by

$$\boldsymbol{\eta}_{TDU}(v_{\Upsilon}) = \sum_{l=1}^{L} [\boldsymbol{\Psi}_{\mathrm{x}}]_{v_{\boldsymbol{\Psi}_{\mathbf{X}}, d_{x_l}}} [\boldsymbol{\Psi}_{\mathrm{y}}]_{v_{\boldsymbol{\Psi}_{\mathbf{Y}}, d_{y_l}}}, \qquad v_{\Upsilon} = 1, \ldots, V_{\Upsilon} \tag{5.8}$$

where d_{l_x} and d_{l_y} are the division levels with the location of TDU layer l in the x- and y-dimensions, respectively. Our 10×6 element PAA example in Fig. 5.2 yields $\boldsymbol{\eta}_{TDU}(250) = [\boldsymbol{\Psi}_{\mathrm{x}}]_{1,2}[\boldsymbol{\Psi}_{\mathrm{y}}]_{2,1} + [\boldsymbol{\Psi}_{\mathrm{x}}]_{1,3}[\boldsymbol{\Psi}_{\mathrm{y}}]_{2,3} = 2 \times 1 + 6 \times 10 = 62$ TDUs, equating what we found in observation. Fig. 5.7 shows the relationship between the TDU count and variant number, v_{Υ}, for the 10×6 element PAA. Similarly, the total number of bits for each TDU-A variant is

$$\boldsymbol{\eta}_{bit}(v_{\Upsilon}) = \sum_{l=1}^{L} [\boldsymbol{\Psi}_{\mathrm{x}}]_{v_{\Psi_{\mathrm{x}}},d_{x_l}} [\boldsymbol{\Psi}_{\mathrm{y}}]_{v_{\Psi_{\mathrm{y}}},d_{y_l}} [\boldsymbol{B}]_{v_{\mathrm{B}},l}\,, v_{\Upsilon} = 1,2,\dots,V_{\Upsilon}. \tag{5.9}$$

Our 10×6 element PAA example in Fig. 5.2 yields $\boldsymbol{\eta}_{bits}(250) = [\boldsymbol{\Psi}_{\mathrm{x}}]_{1,2}\left[\boldsymbol{\Psi}_{\mathrm{y}}\right]_{2,1} [\boldsymbol{B}]_{2,1} + [\boldsymbol{\Psi}_{\mathrm{x}}]_{1,3}\left[\boldsymbol{\Psi}_{\mathrm{y}}\right]_{2,3} [\boldsymbol{B}]_{2,2} = 2 \times 1 \times 4 + 6 \times 10 \times 6 = 368$ bits, equating what we found by observation. Fig. 5.8 shows the relationship between the bit count and variant number, v_{Υ}, for the 10×6 element PAA.

5.2 Architecture Variants Performance Matrix of a General Rectangular PAA

The performance matrix $[\boldsymbol{A}]$ is the coefficient matrix in the optimization and is weighted against performance constraints. The construction of the $[\boldsymbol{A}]$ matrix is a concatenation of vectors that track performance vs TDU-A variant. It is up to the TDU-A architect to determine which performance criteria must be constrained during optimization. For simplicity and brevity, in this section the construction of the $[\boldsymbol{A}]$ matrix is demonstrated with the 10×6 element PAA example by tracking a single performance vector: the quantization phase error, $\boldsymbol{a}_{\phi_e}$, of each vector. Other constraints, such as physical size of the most significant bit (*msb*), may be included in the $[\boldsymbol{A}]$ matrix as shown in Chapter 2. The $[\boldsymbol{A}]$ matrix for the 10×6 element PAA example takes the form

$$[\boldsymbol{A}] = \left[\boldsymbol{a}_{\phi_e}\right]. \tag{5.10}$$

The $\boldsymbol{a}_{\phi_e}$ vector was thoroughly investigated in Chapter 2, however there are key modifications required to the multi-layer TDU derivations to handle the generalities this manuscript introduces: specifically, the addition of 1) a second dimension, 2) arbitrary divisions (i.e., not only 2-way dividers), and 3) arbitrary scan in the x- and y-dimensions. These modifications correspond to equations (2.14)-(2.16). First, equation (2.14), which tracks the number of subarrays or elements being compensated by a TDU layer, must be modified to handle the arbitrary divisions by using the $[\boldsymbol{\Psi}]$ columns of the $[\boldsymbol{\Upsilon}]$ matrix in both the x- and y-dimensions which becomes

$$M_l = M_{l-1} / \left([\boldsymbol{\Psi}_x]_{v,d_{x_l}} / [\boldsymbol{\Psi}_x]_{v,d_{x_{l-1}}} \right) \tag{5.11a}$$

$$N_l = N_{l-1} / \left([\boldsymbol{\Psi}_y]_{v,d_{y_l}} / [\boldsymbol{\Psi}_y]_{v,d_{y_{l-1}}} \right) \tag{5.11b}$$

where d_l is the division level where TDU_l is located, $M_0 = M$, $N_0 = N$, and $[\boldsymbol{\Psi}_x]_{v,d_0} = 1$. Equation (2.15) calculates the distance compensated by a TDU layer and must be similarly modified as

$$h_{x_l} = M_{l-1}\, e_p \left(1 - \frac{1}{[\boldsymbol{\Psi}_x]_{v,d_{x_l}} / [\boldsymbol{\Psi}_x]_{v,d_{x_{l-1}}}} \right) \tag{5.12a}$$

$$h_{y_l} = N_{l-1}\, e_p \left(1 - \frac{1}{[\boldsymbol{\Psi}_y]_{v,d_{y_l}} / [\boldsymbol{\Psi}_y]_{v,d_{y_{l-1}}}} \right). \tag{5.12b}$$

Returning to Fig. 5.2 to illustrate equations (5.11) and (5.12), the element spacing is $e_p = \lambda_{min}/2$, so in the x-dimension $d_{x_1} = 2$ and $d_{x_2} = 5$ leading to $M_0 = 10$, $M_1 = 5$, $M_2 = 1$, $h_{x_1} = 5\lambda_{min}/2$ and $h_{x_2} = 2\lambda_{min}$ and in the y-dimension $d_{y_1} = 1$ and $d_{x_2} = 3$ leading to $N_0 = 6$, $N_1 = 6$, $N_2 = 1$, $h_{y_1} = 0$ and $h_{y_2} = 5\lambda_{min}/2$. Finally, equation (2.16) calculates the scan distance and must be modified as

$$h_{scan_l} = \sqrt{{h_{x_l}}^2 + {h_{y_l}}^2}\, \sin(\theta_{max}) \tag{5.13}$$

where θ_{max} is the max scan angle from the z-axis (i.e., normal to the array) taken on the cardinal plane. Given a unique maximum scan in the x- and y-dimensions, θ_{max} is found as

$$\theta_{max} = \cos^{-1}(\cos(\theta_{zx_{max}}) \cos(\theta_{zy_{max}}) \tag{5.14}$$

where $\theta_{zx_{max}}$ and $\theta_{zy_{max}}$ are the max scan angle taken from the z-axis toward the x-axis and y-axis, respectively. For our 10×6 element PAA example, we take $\theta_{zx_{max}} = 60°$ and $\theta_{zy_{max}} = 30°$ and find that $\theta_{max} = 64.34°$. The scan distances for the architecture in Fig. 5.2 are then $h_{scan_1} =$

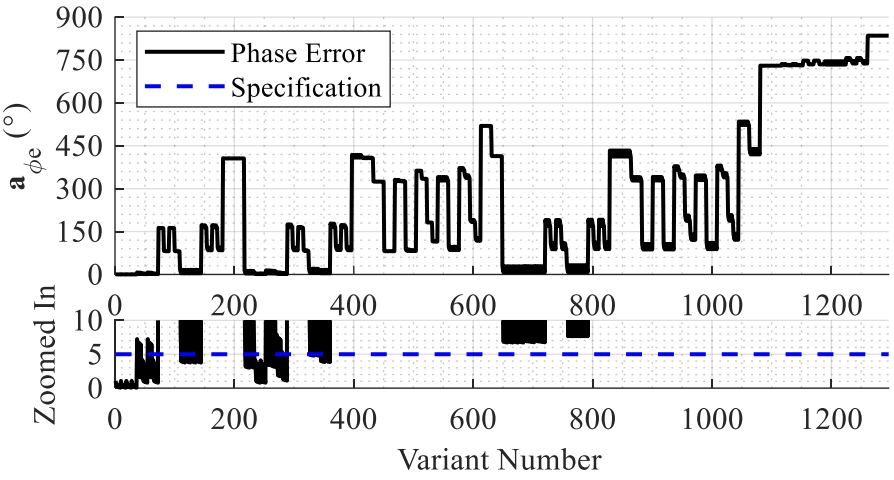

Figure 5.9 Demonstration of the non-linear relationship between RMS phase error and the variant number for the 10×6 element PAA.

2.3 cm and $h_{scan_1} = 2.9$ cm. Beyond these, equations (2.17)-(2.21) may be used in Chapter 2 to calculate the phase error, $\phi_{e,deg}$, of each TDU-A variant, v_{Υ}, to form the $\boldsymbol{a}_{\phi_e}$ vector. We demonstrate in Fig. 5.9 how the performance vector $\boldsymbol{a}_{\phi_e}$ varies vs. TDU-A variant for our 10×6 element PAA example.

5.3 Setting Up the Integer Linear Programming Problem for a General Rectangular PAA

Standard ILP algorithms cannot be used in the general case as in [17] since there are potentially more than a single optimal variant due to the allowance of multiple unique divisions and 2-dimensions of the PAA. Similar to ILP, the aim is to solve

$$\begin{aligned} &minimize && \boldsymbol{K}\boldsymbol{x} \\ &subject\ to && [\boldsymbol{A}]^T\boldsymbol{x} \leq \boldsymbol{b} \\ & && x_1 + x_2 + x_3 + \cdots + x_{V_{\Upsilon}} = 1 \\ & && x_{v_{\Upsilon}} = 0\ or\ 1\ \forall\ v_{\Upsilon} = 1, \ldots, V_{\Upsilon} \end{aligned} \tag{5.15}$$

where $\boldsymbol{x}$ is a variable vector $\boldsymbol{x} = \left[x_1, x_2, \ldots, x_{V_{\Upsilon}}\right]^T$ and the summing constraint, $x_1 + x_2 + x_3 + \cdots + x_{V_{\Upsilon}} = 1$, along with the integer constraint, $x_{v_{\Upsilon}} = 0\ or\ 1\ \forall\ v = 1, \ldots, V_{\Upsilon}$, ensures that the solution will be $x_o = 1$, where subscript o stands for the optimum variant, and all other variables

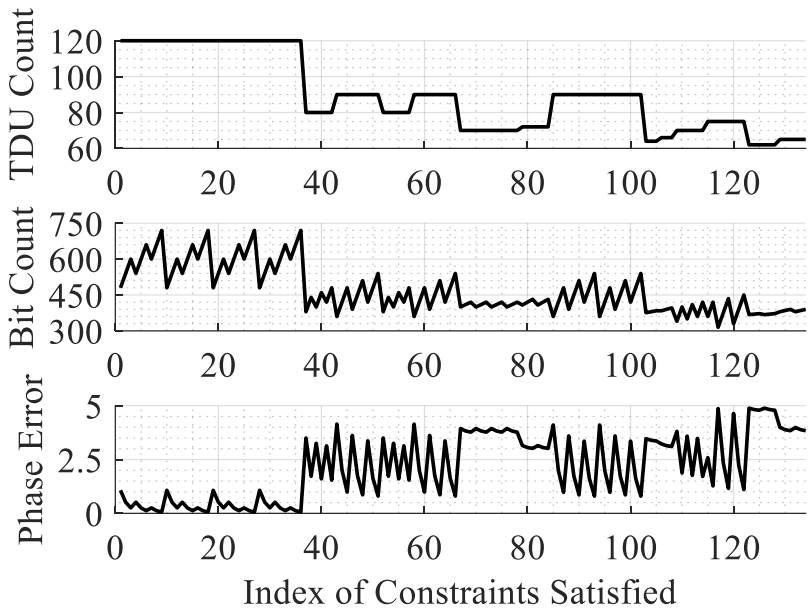

Figure 5.10 TDU count, bit count, and RMS phase error vs index of variants that satisfy the constraints for the 10 × 6 PAA example.

are zero. $[\boldsymbol{A}]$ is the performance matrix as defined in Section 5.3. The vector $\boldsymbol{b}$ contains the constraints for the performance matrix. In this manuscript $\boldsymbol{b}$ is the maximum root mean squared (RMS) quantized phase error. As in Chapter 2, the maximum RMS quantized phase error is set to $\phi_{max} = 5°$ to minimize quantized side lobe levels. This value is placed into the constraint vector $\boldsymbol{b}$ as

$$\boldsymbol{b} = [\phi_{max}]^T. \tag{5.16}$$

$\boldsymbol{Kx}$ sets the objective function of the ILP, which is to minimize the number of TDUs, the number of bits, and the RMS quantization phase error for the TDU-A. Therefore, $\boldsymbol{Kx}$ can be expressed as

$$\boldsymbol{Kx} = [w_{TDU} \quad w_{bits} \quad w_{\phi}][\boldsymbol{\eta}_{TDU} \quad \boldsymbol{\eta}_{bits} \quad \boldsymbol{a}_{\phi_e}]^T \boldsymbol{x} \tag{5.17}$$

where w_{TDU}, w_{bits}, w_{ϕ} are the weights for the contributions of the TDU count, bit count, and phase error, respectively, $\boldsymbol{\eta}_{TDU}$ and $\boldsymbol{\eta}_{bits}$ are vectors containing the number of TDUs and bits for each TDU-A variant as developed in Section 5.2.5. In this chapter, the weighting vector is

$[w_{TDU} \quad w_{bits} \quad w_{\phi}] = [1 \quad 0.01 \quad 0.001]$ to prioritize minimizing TDU count, then the bit count, and lastly the quantized phase error to benefit size, weight, and power by having a less overall number of components. However, it is ultimately decided by the system architect what the priority in optimization will be. Since ILP algorithms cannot be used, a new approach for locating the optimal TDU-A variants is employed consisting of two steps: 1) finding the variants that meet the constraints, and 2) finding the variants that minimize the objective function. In our implementation, first step is completed by using the MATLAB function find() to locate all $\boldsymbol{x}$ variables which satisfy the constraints in equation (10). Second step again employs the find() function to locate the $\boldsymbol{x}$ variables that minimize the objective function of those $\boldsymbol{x}$ variables that satisfied the constraints from first step. There are two optimal solutions found for the 10×6 PAA with corresponding configuration vectors $\boldsymbol{\Lambda}(1, 1,5,4,7)$ and $\boldsymbol{\Lambda}(1, 2,5,4,7)$ where the first is shown in Fig. 2 with TDU_1 has 4 bits with $\tau_{lsb} = 5.0$ psec, TDU_2 has 6 bits with $\tau_{lsb} = 1.57$ psec, and $\phi_{max} = 4.88°$. The difference between the two optimal solutions is how the 6-way divider in the y-dimension of Fig. 5.2 is configured. In the first configuration vector, the 2-way comes before the 3-way, whereas the second configuration vector has the 3-way before the 2-way. Both solutions yield the same performance with the same number of TDUs and bits, however they will be physically laid out differently, providing the architect with options during board layout. Fig. 5.10 shows that there are 134 TDU-A variants of the 1296 available (i.e., 10.3%) that meet the performance constraints and TDU count varies from ~60 to 120 total TDUs and the bit count varies from ~300 to 750 bits which demonstrates the TDU and control line savings through the optimization method. A full derivation example of the $\boldsymbol{A}$ and $\boldsymbol{K}$ matrices is demonstrated in Appendix C for variant 250. A different weighting vector of $[0.1 \quad 1 \quad 0.001]$ yields $\phi_{max} = 4.87°$, 75 TDUs, and 315 bits by heavily minimizing bits over others. On the other hand, a

Figure 5.11 TDU-A variant 8318050 of the 256×120 element PAA where TDU_1 has 3 bits and $\tau_{lsb} = 431.7$ psec, TDU_2 has 6 bits and $\tau_{lsb} = 22.7$ psec, and TDU_3 has 6 bits and $\tau_{lsb} = 1.6$ psec.

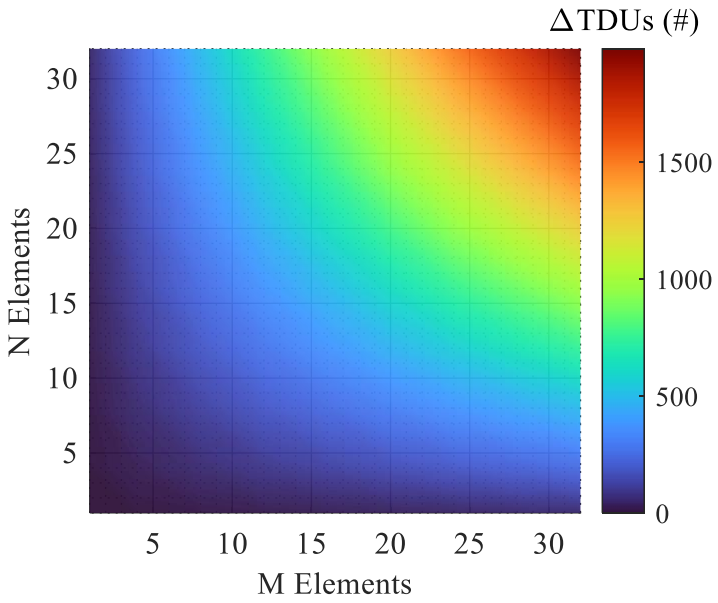

Figure 5.12 Variation in TDU count as the number of M and N elements vary from 1 to 32.

weighting vector of $[0.1 \quad 0.01 \quad 1]$ yields $\phi_{max} = 1.76°$, 70 TDUs, and 410 bits by prioritizing the phase error. The effectiveness increases exponentially with the array size as demonstrated in Fig. 5.12. For example, the TDU savings would approach to 2000 and 500 for 32×32 and 16×16 arrays, respectively, when 3 TDU layers with $\phi_{max} = 5°$ is requested.

5.4 Application to Large Rectangular PAAs

As an example, in this section we consider an $M \times N = 256 \times 120$ element PAA with $\theta_{zx_{max}} = 60°$ and $\theta_{zy_{max}} = 30°$, $f_{max} = 30$ GHz, and $e_p = \lambda_{min}/2$. We set $L = 3$, $b_{min} = 2$ and

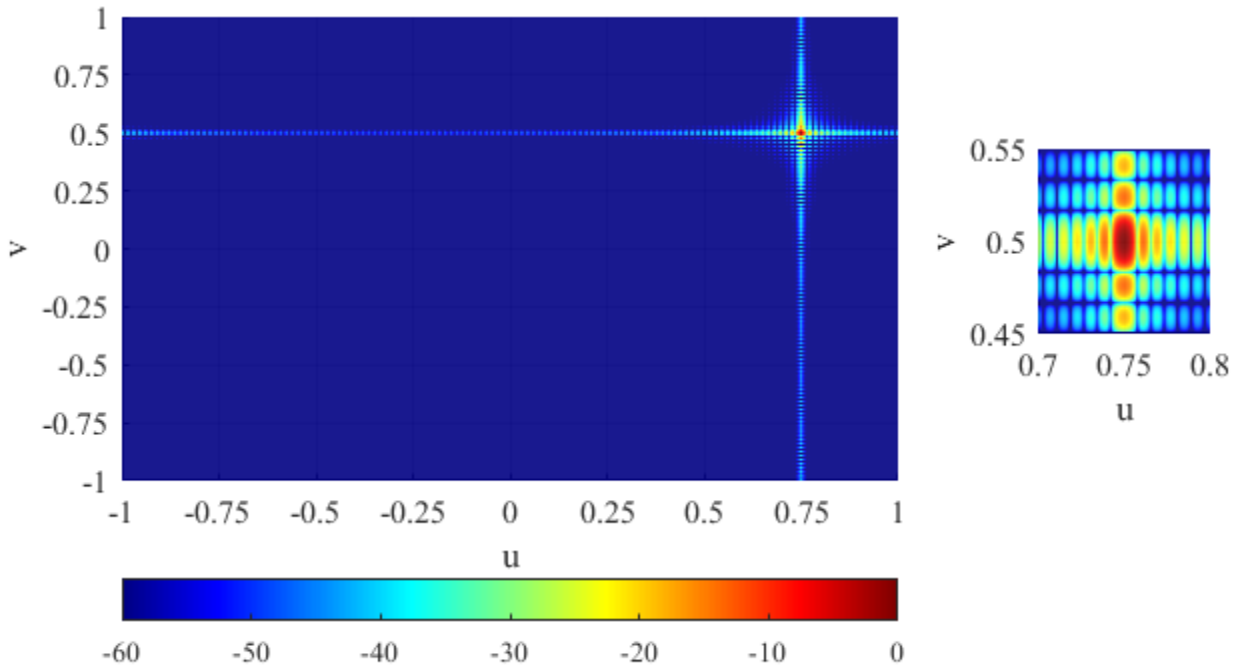

Figure 5.13 AF of 256×120 PAA scanned to $\theta_{zx_{max}} = 60°$ and $\theta_{zy_{max}} = 30°$ with excitations that are ideal.

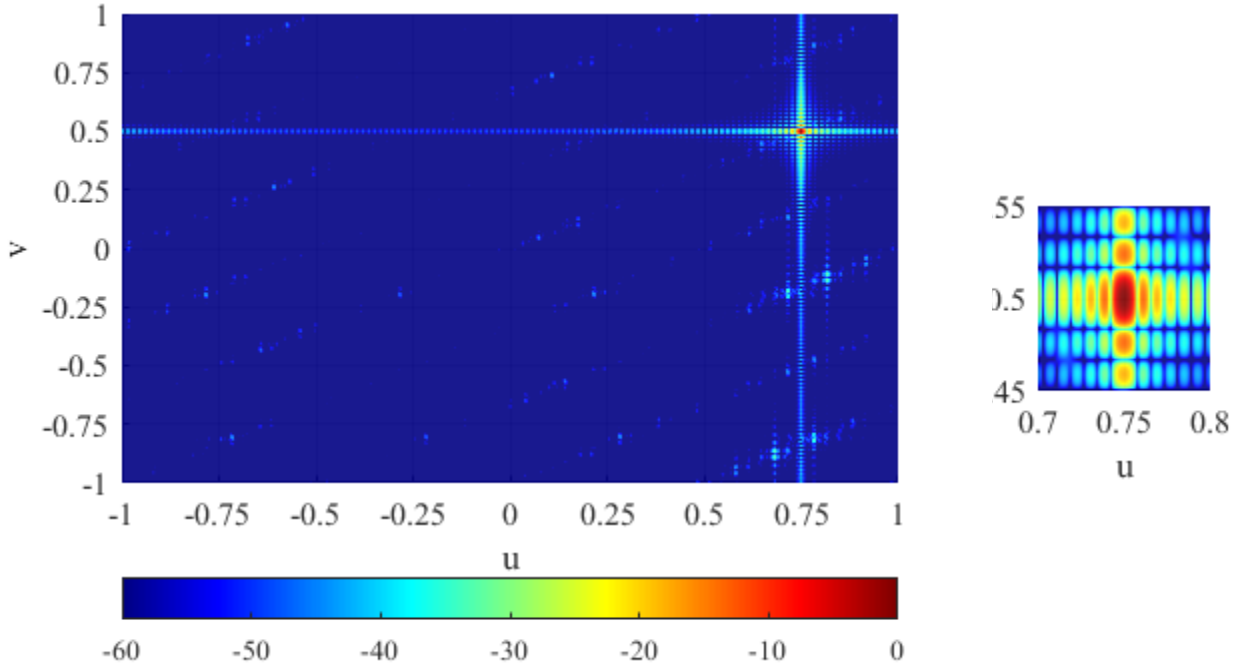

Figure 5.14 AF of 256×120 PAA scanned to $\theta_{zx_{max}} = 60°$ and $\theta_{zy_{max}} = 30°$ with excitations that are generated by the TDU architecture in Fig. 5.11.

and a total of $V_{\Upsilon} = 23{,}100{,}000$ TDU-A variants to be considered. The optimization was placed $b_{max} = 6$. The phase error in this example is again set as $\phi_{max} = 5°$. Given the size of the array allowable bit range, we find that $V_{\Psi_x} = 1$, $V_{\Psi_y} = 20$, $V_{\mathrm{T}_x} = 165$, $V_{\mathrm{T}_y} = 56$, $V_B = 125$ leading to into standard form and the ILP was run. Eliminating the architectures that do not meet the maximum allowable RMS phase error criteria leaves 179,011 of 23,100,000 (i.e., ~0.8%) TDU-A variants. Of the 179,011 TDU-A variants, the TDU count ranges from 32,008 to 92,160, which is a delta of 60,152 TDUs. The optimal architecture is found to be variant 8,318,050 which is shown in Fig. 5.11 and has an RMS phase error of $\boldsymbol{a}_{\phi_e}(8{,}318{,}050) = 4.90°$ with a total of 32,008 TDUs. An iterative approach such as demonstrated in [4] or suggested in [5] may lead to a solution that meets RMS phase error performance, however the resulting TDU-A would most likely not minimize the number of TDUs and bits as the odds are 1:179,011 which demonstrates the power of the optimization approach. To compare the performance of the ideal delay settings and the modeled discretized TDU-A, Figs. 5.13 and 5.14 shows the AF at $\theta_{zx_{max}} = 60°$ and $\theta_{zy_{max}} = 30°$ (i.e., $\theta = 64.3°, \phi = 33.7°$) scan angle in the u-v plane where $u = \sin(\theta)\cos(\phi)$ and $v = \sin(\theta)\sin(\phi)$. Fig. 5.13 presents the AF of the 256×120 element PAA with ideal elemental delay settings and Fig. 5.14 presents the AF of the 256×120 element PAA with elemental delay settings configured by the optimal TDU-A shown in Fig. 5.11 (see Appendix A). It can be observed in Fig. 5.14 that the TDU-A had the necessary range to steer to the maximum extent of $u = 0.75$, $v = 0.5$. The error at each element is bounded between $\pm lsb/2$ which leads to side lobe degradation below -26 dB as expected due to our RMS error constraint of $\leq 5°$ [1].

5.5 Conclusion of General Rectangular PAA TDU-A Optimization

A systematic method for optimizing the time delay unit architecture of general 2D rectangular phased antenna arrays is introduced to guarantee the desired phase error requirement

while minimizing power, complexity, and cost. As in Chapter 2, the problem is cast into the standard form of integer linear programming to locate the optimal architecture which targets minimizing the total TDU and bit count while achieving the desired performance while requiring a new algorithm to solve. The $\boldsymbol{T}$, $\boldsymbol{\Psi}$, and $\boldsymbol{B}$ matrices are developed to track the number of TDUs, branches, and bits for each architecture variants, and key modifications to Chapter 2 are demonstrated to enable the construction of the performance matrix $\boldsymbol{A}$ to accommodate general 2D rectangular PAAs. The optimization method is illustrated through two modeled examples: a 10×6 element rectangular PAA and a 256×120 element PAA. The development of the 10×6 element rectangular problem is carried throughout to demonstrate configuring each matrix and placing the problem into standard ILP form. An optimal architecture for each example case is found which minimizes the number of TDUs and bits while achieving the desired RMS phase error performance requirement.

Chapter 6: Concluding Remarks

In this dissertation, a rigorous method for locating the optimal hierarchical time delay unit architecture (TDU-A) of ultra-wideband (UWB) phased antenna array (PAA)s is demonstrated. The optimum TDU-A is found by utilizing an objective function which aims to minimize TDU and bit count while achieving acceptable performance and also being manufacturable. Minimizing TDU and bit count leads to lower system power, cost, and complexity. The problem is cast into standard integer linear programming (ILP) form with the necessary objective function and constraints. ILP can easily handle the linear case with single division types (e.g., all 2-ways in the RF-division); however, unique division levels of general 2D antenna arrays lead to multiple optimal solutions yielding a problem that is ill-posed for ILP. In this case, a secondary algorithm is presented which efficiently handles redundant optimal solutions. Demonstrations are carried out for both linear and rectangular PAAs showing the utility of the methods to minimize TDU count and bit count while achieving performance and size constraints. This dissertation also investigates various delay error effects during the development of a practical TDU-A solutions and demonstrates how to account for these errors early when architecting a system. If left unaccounted, these errors can wreak havoc on system performance, so it is essential these are budgeted in the design early on. Finally, a fabricated example is demonstrated which shows excellent correlation to simulation and it is shown that the array is calibratable by carrying out that exercise. Specifically, this dissertation makes the following accomplishments:

- An optimal architecture is found for an 8 element linear PAA, a 128 element linear PAA, and a 256×256 element PAA TDU-A which reduced the TDU count as high

as 20% compared to previous iterative methods while achieving the RMS phase error performance requirement.

- A full wave simulation of a 128 element linear array constructed with Vivaldi antennas shows steering capability from $-50°$ to $+50°$ and side lobe level perturbation due to the quantization from the optimal TDU architecture excitations less than -26 dBm.
- The effects of time delay errors due to frequency dependent variations in VSWR, divider isolation and load mismatch, and dispersion were calculated and included in the optimization algorithm to find a TDU-A with additional 21.4 psec to ensure enough TDU range when steering to extreme angles (i.e., $50°$ at 30 GHz).
- An experimental verification of three 16 element linear PAA test articles with an optimized TDU-A operating from 5 GHz to 30 GHz with beams steered towards 0°, 25°, and 50° were in family with modeled results that assume a gaussian distribution of calculated errors.
- Two calibration examples of an optimized 16 element PAA TDU-A at $25°$ scan and 25 GHz with an IBW of 1 GHz demonstrated the optimal TDU-A variants ability to be calculated by switching *lsb*s of each branch until the error is bounded at the center frequency of the IBW within the quantization region.
- A large array PAA example with 256×120 elements which shows that optimization can provide significant savings in TDU when compared to the traditional iterative design approaches as the usable TDU-A variants with an RMS phase error less than $5°$ have TDU counts that vary from 32,008 to 92,160.

There is room for future development in this research area in multiple ways. The first is by further expanding the algorithm to include more abstract array types. The majority of PAAs are

linear or rectangular and therefore are covered by the methods presented within this dissertation, however there are additional PAA types which are not covered, such as PAAs with triangular lattices and conformal PAAs. There is also opportunity to expand the algorithm generated herein to be more general by accepting elemental positions and specified mechanical constraints to generate optimal TDU-A solutions for these more complicated PAA constructions. Within this dissertation, cost is considered a secondary benefit by lowering the TDU and bit count. If desired, the cost could be directly included within the optimization algorithm such that the objective function is to minimize cost of a TDU-A. An interesting topic worth exploring is to find opportunities to utilize TDU-A configurations to generate beam patterns with certain characteristics that may be exploited for increased security. There is current research being pursued in altering the pattern of antennas by small adjustments in the fabricated characteristics to generate unique "RF fingerprints" of the pattern for security purposes [57-58]. By extension, an array may synthesize pattern variations to generate finite fingerprints to increase security. Additionally, the amplitude weightings of the elements are largely ignored in this discussion. There is an analogous discussion of hierarchical distribution for the amplitude weighting across the array to both calibrate for amplitude errors and generate altered patterns such employing techniques such as Taylor weightings. Once this is accomplished, the next step would be to include amplitude errors due to time delay units in the optimization distributing the amplitude weightings, and to include the delay errors due to the amplitude weighting components into the optimization of the TDU-A.

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Appendix A: Array Factor with TDU Configured Excitations

This appendix provides practical steps to assist the reader in configuring a TDU-A to steer a PAA to a desired location. The process is thoroughly demonstrated for a linear PAA followed by a brief walkthrough of a more complex rectangular PAA. We begin by returning to the formulation of the array factor (AF) equation from Chapter 3. The AF is calculated using equations in [1]

$$AF = \sum a_i \mathrm{e}^{jk_0 r_i \cdot \hat{r}} \qquad (A.1)$$

where $\boldsymbol{r_i}$ is the position vector of the i^{th} antenna element (referenced to the origin), $\hat{\boldsymbol{r}}$ is the unit vector in the direction of the observation point, $a_i = |a_i| e^{j\phi_{a_i}}$ is the complex weight of the i^{th} antenna element, $k_0 = 2\pi/\lambda_0$, $\lambda_0 = c/f_0$, c is the speed of light, and f_0 is the frequency at which the AF is being evaluated. In this appendix, we assume a uniform amplitude distribution with $|a_i| = 1, \forall i$, and the unwrapped phase excitation of each element weighting (i.e., ϕ_{a_i}) is obtained from a search method given a TDU-A. The search method begins by finding the ideal phase excitation required as

$$\phi_{\boldsymbol{a_i}} = -k_0 r_i \sin(\theta_{steer}) \qquad (A.2)$$

where ϕ_{a_i} is the ideal phase excitation at the i^{th} antenna element, $k_0 = 2\pi/\lambda_0$ is the wavenumber and λ_0 is the wavelength, and θ_{steer} is the desired beam steering direction in degrees. Then we find the ideal delay as

$$\tau_{a_i} = \frac{-\phi_{a_i}}{f_0\, 360}. \qquad (A.3)$$

Table A.1 TDU bit states for the TDU-A in Fig. 3.12.

TDU_1 5 bits							TDU_2 6 bits (States 1-32)								TDU_2 6 bits (States 33-64)							
State	1	2	3	4	5	delay (Psec)	State	1	2	3	4	5	6	delay (Psec)	State	1	2	3	4	5	6	delay (Psec)
1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	33	1	0	0	0	0	0	46.4
2	0	0	0	0	1	4.4	2	0	0	0	0	0	1	1.45	34	1	0	0	0	0	1	47.85
3	0	0	0	1	0	8.8	3	0	0	0	0	1	0	2.9	35	1	0	0	0	1	0	49.3
4	0	0	0	1	1	13.2	4	0	0	0	0	1	1	4.35	36	1	0	0	0	1	1	50.75
5	0	0	1	0	0	17.6	5	0	0	0	1	0	0	5.8	37	1	0	0	1	0	0	52.2
6	0	0	1	0	1	22	6	0	0	0	1	0	1	7.25	38	1	0	0	1	0	1	53.65
7	0	0	1	1	0	26.4	7	0	0	0	1	1	0	8.7	39	1	0	0	1	1	0	55.1
8	0	0	1	1	1	30.8	8	0	0	0	1	1	1	10.15	40	1	0	0	1	1	1	56.55
9	0	1	0	0	0	35.2	9	0	0	1	0	0	0	11.6	41	1	0	1	0	0	0	58
10	0	1	0	0	1	39.6	10	0	0	1	0	0	1	13.05	42	1	0	1	0	0	1	59.45
11	0	1	0	1	0	44	11	0	0	1	0	1	0	14.5	43	1	0	1	0	1	0	60.9
12	0	1	0	1	1	48.4	12	0	0	1	0	1	1	15.95	44	1	0	1	0	1	1	62.35
13	0	1	1	0	0	52.8	13	0	0	1	1	0	0	17.4	45	1	0	1	1	0	0	63.8
14	0	1	1	0	1	57.2	14	0	0	1	1	0	1	18.85	46	1	0	1	1	0	1	65.25
15	0	1	1	1	0	61.6	15	0	0	1	1	1	0	20.3	47	1	0	1	1	1	0	66.7
16	0	1	1	1	1	66	16	0	0	1	1	1	1	21.75	48	1	0	1	1	1	1	68.15
17	1	0	0	0	0	70.4	17	0	1	0	0	0	0	23.2	49	1	1	0	0	0	0	69.6
18	1	0	0	0	1	74.8	18	0	1	0	0	0	1	24.65	50	1	1	0	0	0	1	71.05
19	1	0	0	1	0	79.2	19	0	1	0	0	1	0	26.1	51	1	1	0	0	1	0	72.5
20	1	0	0	1	1	83.6	20	0	1	0	0	1	1	27.55	52	1	1	0	0	1	1	73.95
21	1	0	1	0	0	88	21	0	1	0	1	0	0	29	53	1	1	0	1	0	0	75.4
22	1	0	1	0	1	92.4	22	0	1	0	1	0	1	30.45	54	1	1	0	1	0	1	76.85
23	1	0	1	1	0	96.8	23	0	1	0	1	1	0	31.9	55	1	1	0	1	1	0	78.3
24	1	0	1	1	1	101.2	24	0	1	0	1	1	1	33.35	56	1	1	0	1	1	1	79.75
25	1	1	0	0	0	105.6	25	0	1	1	0	0	0	34.8	57	1	1	1	0	0	0	81.2
26	1	1	0	0	1	110	26	0	1	1	0	0	1	36.25	58	1	1	1	0	0	1	82.65
27	1	1	0	1	0	114.4	27	0	1	1	0	1	0	37.7	59	1	1	1	0	1	0	84.1
28	1	1	0	1	1	118.8	28	0	1	1	0	1	1	39.15	60	1	1	1	0	1	1	85.55
29	1	1	1	0	0	123.2	29	0	1	1	1	0	0	40.6	61	1	1	1	1	0	0	87
30	1	1	1	0	1	127.6	30	0	1	1	1	0	1	42.05	62	1	1	1	1	0	1	88.45
31	1	1	1	1	0	132	31	0	1	1	1	1	0	43.5	63	1	1	1	1	1	0	89.9
32	1	1	1	1	1	136.4	32	0	1	1	1	1	1	44.95	64	1	1	1	1	1	1	91.35

where τ_{a_i} is the ideal time delay requred at the i^{th} antenna element. Note that the target of the TDU-A configuration is to provide the delay slope across the elements of the PAA generated by equation (A.3) and not necessarily the absolute value of τ_{a_i}. To that end, the goal when configuring

Table A.2 Failed configuring the TDU-A of an example 16 element linear PAA since element 9 has a quantized error that is outside the $\tau_{lsb}/2 = 0.725$ psec boundary.

Element # (i)	r_i	ϕ_{a_i}	τ_{a_i}	TDU_{1_i}	TDU_{2_i}	τ_{quant_i}	$\bar{\tau}_{quant_i}$	$\bar{\tau}_{quant_i} - \tau_{a_i}$
1	0.000	0.00	0.00	0	0.00	0.00	0.00	**0.00**
2	0.005	38.04	7.04		7.25	7.25	7.25	**0.21**
3	0.010	76.07	14.09		14.50	14.50	14.50	**0.41**
4	0.015	114.11	21.13		21.75	21.75	21.75	**0.62**
5	0.020	152.14	28.17		27.55	27.55	27.55	**-0.62**
6	0.025	190.18	35.22		34.80	34.80	34.80	**-0.42**
7	0.030	228.21	42.26		42.05	42.05	42.05	**-0.21**
8	0.035	266.25	49.31		47.85	47.85	47.85	**-1.46**
9	0.040	304.29	56.35	57.2	0.00	57.20	57.20	**0.85**
10	0.045	342.32	63.39		5.80	63.00	63.00	**-0.39**
11	0.050	380.36	70.44		13.05	70.25	70.25	**-0.19**
12	0.055	418.39	77.48		20.30	77.50	77.50	**0.02**
13	0.060	456.43	84.52		27.55	84.75	84.75	**0.23**
14	0.065	494.46	91.57		34.80	92.00	92.00	**0.43**
15	0.070	532.50	98.61		42.05	99.25	99.25	**0.64**
16	0.075	570.53	105.65		47.85	105.05	105.05	**-0.60**

the TDUs in the TDU-A is to minimize the delta between τ_{a_i} and the sum of the TDU layers for each element normalized to the first element. This delta is the called quantized error and must be bounded by $\pm\tau_{lsb_l}$.

The following example demonstrates how the TDU-A is configured for a 16 element linear PAA. Returning to Fig. 3.12, we have a two layered TDU-A where there is a 2-way followed by TDU_1 which has 5 bits with $\tau_{lsb_1} = 4.4$ psec, then there are three 2-way dividers before TDU_2 which has 6 bits with $\tau_{lsb_2} = 1.45$ psec. The bit states for the TDUs on each layer is shown in Table A.1. The pitch of the arrayed antenna elements is half the wavelength at the max frequency of 30 GHz, or 0.005 m, which provides r_i for each of the elements as shown in the second column of Table A.2. If we aim to configure the TDU-A to steer the antenna pattern to 25° at 15 GHz, we

follow equations (A.2) and (A.3) to find ϕ_{a_i} and τ_{a_i} for each element as shown in Table A.2. The τ_{a_i} column represents the target delay slope for our TDU-A configuration. We may now begin configuring the TDU-A by starting with TDU layer 1 and selecting the bit states from TDU_1 in Table A.1 for each TDU that provides the smallest error when compared to the lowest τ_{a_i} value covered by each TDU on layer 1. For our example, there are two TDUs on layer 1. The first TDU services elements 1-8 and the lowest delay value is $\tau_{a_1} = 0$ psec. So, we choose bit state 1 of TDU_1 in Table A.1 for the first TDU on layer 1 which provides $TDU_{1_{1:8}} = 0$ psec and a quantized error of 0 psec which is within the $\pm\tau_{lsb_1}/2 = \pm 2.2$ psec bound as required.. The second TDU on layer 1 services elements 9-16 and the lowest delay value is $\tau_{a_9} = 56.35$ psec. So, we select bit state 14 of TDU_1 in Table A.1 so that $TDU_{1_{9:16}} = 57.2$ psec which produces a quantized error of $57.2 - 56.38 = 0.85$ psec which is within the $\pm\tau_{lsb_1}/2 = \pm 2.2$ psec bound as required. Next, we move on to TDU layer 2, where there are 16 total TDUs. Since there are no additional layers, the total configured delay of the TDU-A for each element is $\tau_{quant_i} = TDU_{1_i} + TDU_{2_i}$. The goal is to ensure that the slope of τ_{quant_i} is as close to τ_{a_i} as possible since the slope represents the progressive delay at each element which determines the direction the beam is pointed. To compare the slope, we normalize τ_{quant_i} to the first element as $\bar{\tau}_{quant_i} = \tau_{quant_i} - \tau_{quant_1}$. The normalized configured delay for each element must be bounded by half the lsb of the final TDU layer. In our example case there are $L = 2$ layers, so the error must satisfy $-\tau_{lsb_2}/2 \leq \bar{\tau}_{quant_i} - \tau_{a_i} \leq \tau_{lsb_2}/2$. Starting with element 1, $\tau_{a_1} = 0$ psec, so we choose bit state 1 of TDU_2 in Table A.1 for the first TDU on layer 2 (i.e., TDU_{2_1}) which provides $TDU_{2_1} = 0$ psec and $\bar{\tau}_{quant_i} = 0$ which satisfies the requirement $-\tau_{lsb_2}/2 \leq \bar{\tau}_{quant_1} - \tau_{a_1} \leq \tau_{lsb_2}/2$ since $\tau_{lsb_2}/2 = 0.725$ psec and $\bar{\tau}_{quant_1} - \tau_{a_1} = 0$. Next, we look at element 2, with $\tau_{a_2} = 7.04$ psec. We choose bit state 6 of TDU_2 in Table

Table A.3 Passed configuring the TDU-A of an example 16 element linear PAA by increasing all TDU_2 settings by one *lsb* of 1.45 psec except for TDU_{2_9}.

Element # (i)	r_i	ϕ_{a_i}	τ_{a_i}	TDU_{1_i}	TDU_{2_i}	τ_{quant_i}	$\bar{\tau}_{quant_i}$	$\bar{\tau}_{quant_i} - \tau_{a_i}$
1	0.000	0.00	0.00	0	1.45	1.45	0.00	**0.00**
2	0.005	38.04	7.04		8.70	8.70	7.25	**0.21**
3	0.010	76.07	14.09		15.95	15.95	14.50	**0.41**
4	0.015	114.11	21.13		23.20	23.20	21.75	**0.62**
5	0.020	152.14	28.17		29.00	29.00	27.55	**-0.62**
6	0.025	190.18	35.22		36.25	36.25	34.80	**-0.42**
7	0.030	228.21	42.26		43.50	43.50	42.05	**-0.21**
8	0.035	266.25	49.31		50.75	50.75	49.30	**-0.01**
9	0.040	304.29	56.35	57.2	0.00	57.20	55.75	**-0.60**
10	0.045	342.32	63.39		7.25	64.45	63.00	**-0.39**
11	0.050	380.36	70.44		14.50	71.70	70.25	**-0.19**
12	0.055	418.39	77.48		21.75	78.95	77.50	**0.02**
13	0.060	456.43	84.52		29.00	86.20	84.75	**0.23**
14	0.065	494.46	91.57		36.25	93.45	92.00	**0.43**
15	0.070	532.50	98.61		43.50	100.70	99.25	**0.64**
16	0.075	570.53	105.65		49.30	106.50	105.05	**-0.60**

A. 1 which provides $TDU_{2_2} = 7.25$ psec and produces $\bar{\tau}_{quant_2} - \tau_{a_2} = 7.25 - 7.04 = 0.21 <$ 0.725 psec as required. This exercise is carried out for each element and results in the TDU setting shown in Table A.2. However, this leads to an error that is outside the $\pm\,\tau_{lsb_2}/2 = \pm 0.725$ psec requirement in element 9. This is because $\bar{\tau}_{quant_9} - \tau_{a_9} > \tau_{lsb_2}/2$ (i.e., $57.2 - 56.35 = 0.85 >$ 0.725) which is a problem because TDU_2 at element 9 is set to 0 and TDU values cannot go negative as required to bring $\bar{\tau}_{quant_9} - \tau_{a_9}$ within the $\pm\tau_{lsb_2}/2 = \pm 0.725$ boundary (i.e., a single negative lsb would bring the error within the boundary; $57.2 - 1.45 - 56.35 = -0.6$). Therefore, the TDU-A configuration in Table A.2 fails to achieve the necessary performance. To mitigate this issue, we take advantage of the fact that the goal is to achieve a delay slope across the array equal to that of τ_{a_i} row of Table A.2. We therefore increase the value of the TDU_2 bit setting for element

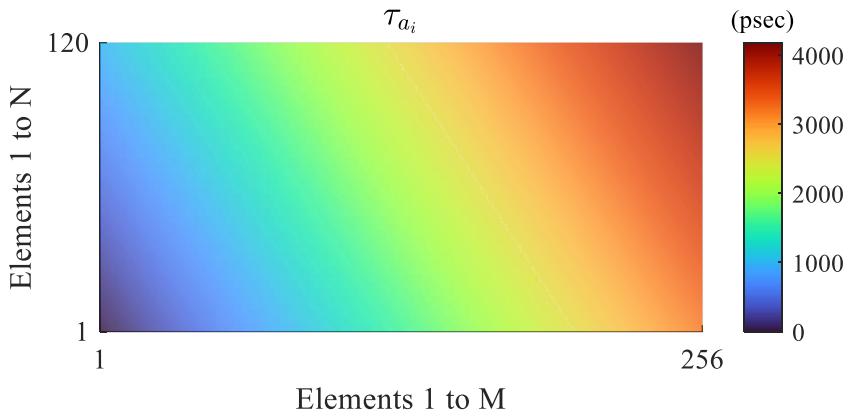

Figure A.1 Ideal delay settings for each element of a 256×120 element PAA steered to $\theta_{zx} = 60°$ and $\theta_{zy} = 30°$.

1 by a single bit so that the bit state of TDU_{2_1} is changed from 1 to 2 such that $TDU_{2_1} = 1.45$ psec. Then, the process for finding the setting of each TDU_{2_i} is repeated to minimize the $\bar{\tau}_{quant_i} - \tau_{a_i}$error. The result of this is shown in Table A.3 which shows that $-\tau_{lsb_2}/2 \leq \bar{\tau}_{quant_i} - \tau_{a_i} \leq \tau_{lsb_2}/2$ is satisfied so that this TDU-A configuration meets the appropriate conditions. If this was still not passing, we would increase element 1 an additional bit on TDU layer 2 and repeat the process until all elements satisfy the bounded quantized error condition. Note that by design our TDU-A has the range to handle this adding of delay, this is why we carry quantization error from the previous layer when architecting the TDU-A (See Section 2.2).

The process of configuring the TDU-A to achieve a steer to a specified angle at a specified frequency can be set up in an algorithm rather than being completed by hand and can accommodate much larger arrays with complex TDU-A networks. For example, returning to the architecture shown in Fig. 5.11 for the 256×120 element PAA with element spacing of $\lambda/2$ at $f_{max} = 30$ GHz, we will produce the TDU-A configuration settings which produced the AF plot shown in Fig 5.14. We start by using equations (A.2) and (A.3) to find the ideal phase setting at each element

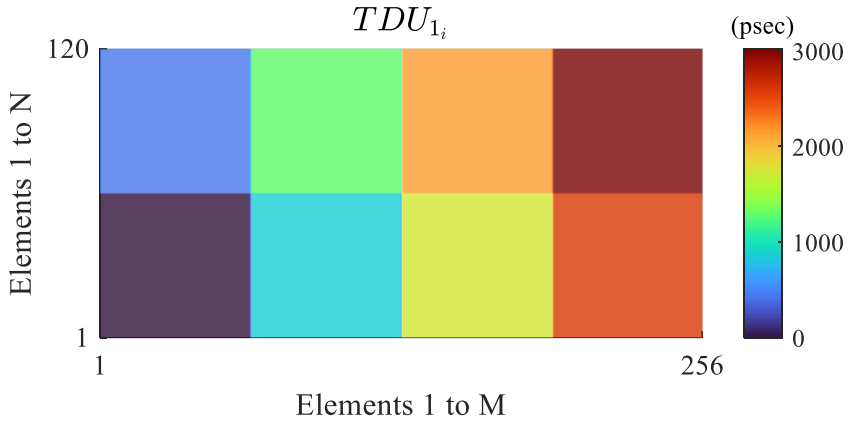

Figure A.2 TDU settings for layer 1 of the architecture in Fig. 5.11 for a 256×120 element PAA steered to $\theta_{zx} = 60°$ and $\theta_{zy} = 30°$.

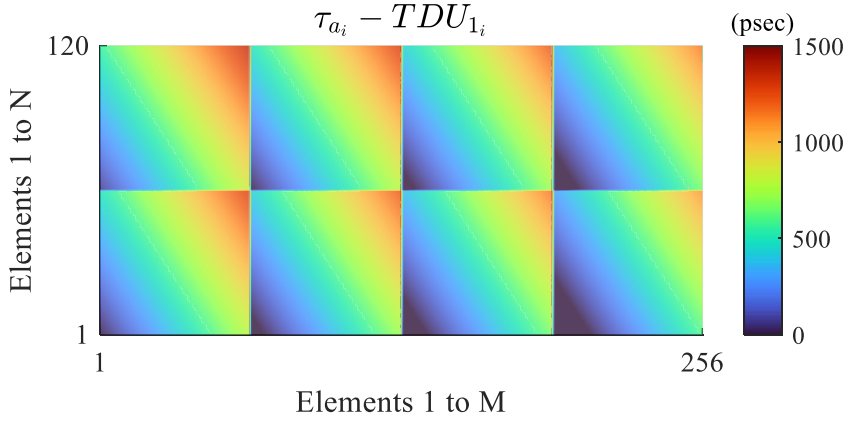

Figure A.3 Delay delta to be made up for by the remaining TDU layers after layer 1 in the architecture in Fig. 5.11 for a 256×120 element PAA steered to $\theta_{zx} = 60°$ and $\theta_{zy} = 30°$.

as shown in Fig. A.1 which represents the delay gradient across the PAA to steer to $\theta_{zx} = 60°$ and $\theta_{zy} = 30°$. Next, we follow the method shown above to configure the TDU-A by beginning at TDU layer 1. Each TDU_{1_i} is configured by selecting the bit states that provides the smallest delta when compared to the lowest τ_{a_i} value covered by each TDU on layer 1. Again, this ensures the quantized error at the lowest delay setting remains within the $\pm\tau_{lsb_1}$ boundary. The setting for

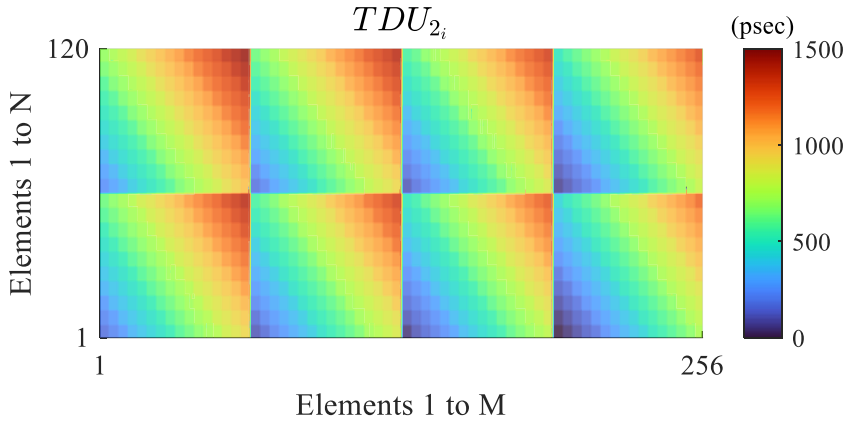

Figure A.4 TDU settings for layer 2 of the architecture in Fig. 5.11 for a 256×120 element PAA steered to $\theta_{zx} = 60°$ and $\theta_{zy} = 30°$.

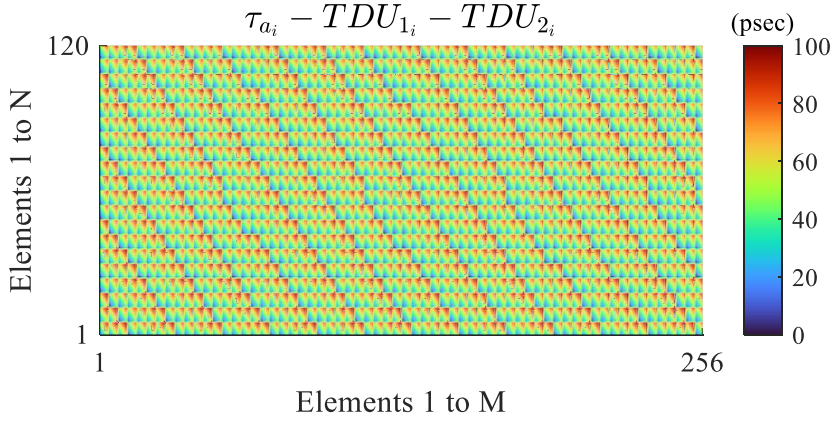

Figure A.5 Delay delta to be made up for by the remaining TDU layers after layer 2 in the architecture in Fig. 5.11 for a 256×120 element PAA steered to $\theta_{zx} = 60°$ and $\theta_{zy} = 30°$.

each TDU_{1_i} is shown in Fig. A.2. There are 8 TDU_{1_i} setting blocks as expected by the architecture shown in Fig. 5.11 since there is a 2-way in the y-dimension and a 4-way in the x-dimension before TDU layer 1. By taking the settings shown in Fig. A.1 and subtracting Fig. A.2, we are left with the required phase gradient to be accommodated by TDU layers 2 and 3, which is shown in Fig. A.3. The next step is to find the TDU_{2_i} bit state configurations by selecting the bit states that provide the smallest delta when compared to the lowest $\tau_{a_i} - TDU_{1_i}$ value in Fig. A.3 covered by

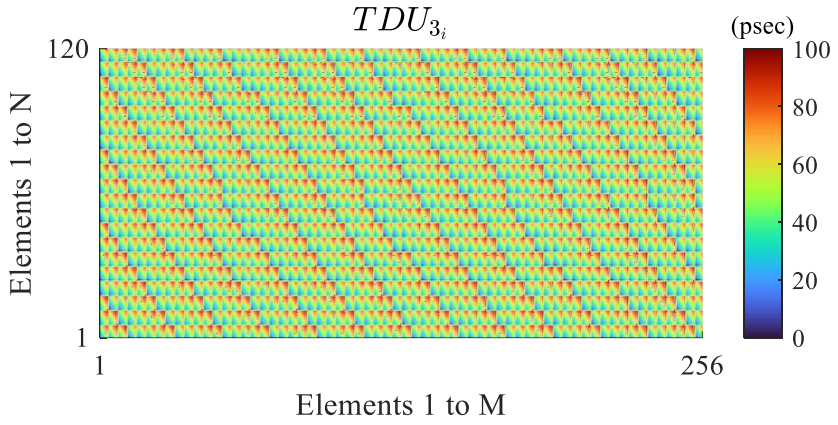

Figure A.6 TDU settings for layer 3 of the architecture in Fig. 5.11 for a 256×120 element PAA steered to $\theta_{zx} = 60°$ and $\theta_{zy} = 30°$.

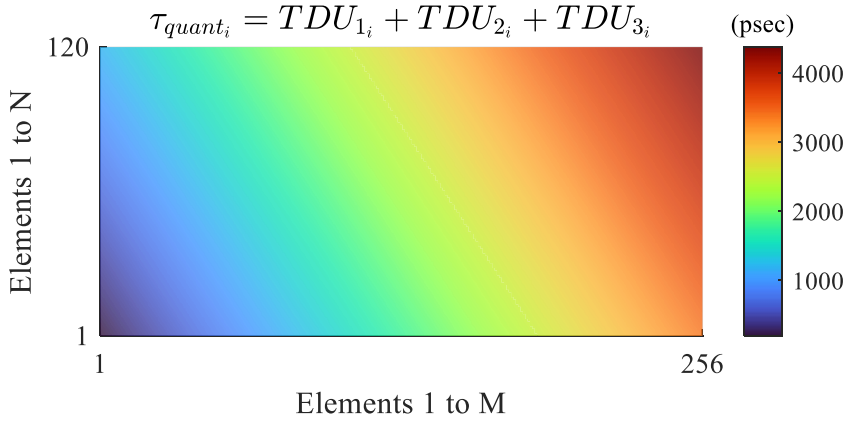

Figure A.7 Discretized total delay distribution for the TDU configuration of the architecture in Fig. 5.11 for a 256×120 element PAA steered to $\theta_{zx} = 60°$ and $\theta_{zy} = 30°$.

each TDU_{2_i}. This process is carried out and the result is shown in Fig. A.4 where there are 192 TDU setting blocks shown within the TDU_{1_i} setting blocks as expected due to the 16-way divider in the x-dimension and 12-way divider in the y-dimension after TDU_1 and before TDU_2. By taking the settings shown in Fig. A.3 and subtracting the gradient in Fig. A.4, we are left with the required delay gradient to be accommodated by TDU layer 3 shown in Fig. A.5. The final configuration step is to find the TDU_{3_i} settings by selecting bit states that provide the smallest delta when

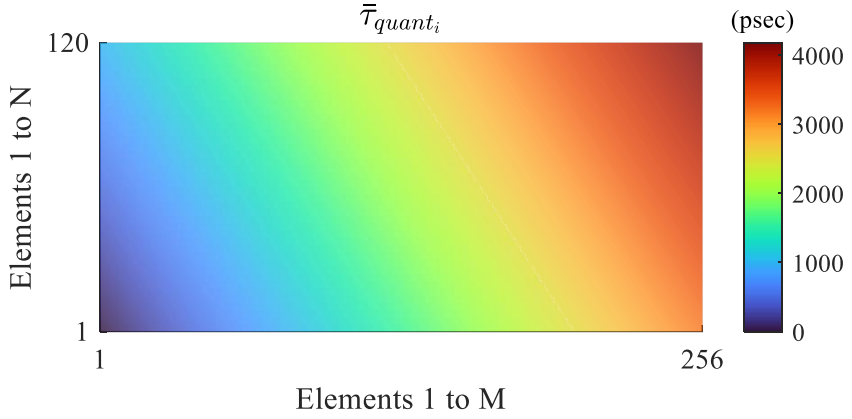

Figure A.8 Normalized discretized total delay distribution for the TDU configuration of the architecture in Fig. 5.11 for a 256×120 element PAA steered to $\theta_{zx} = 60°$ and $\theta_{zy} = 30°$.

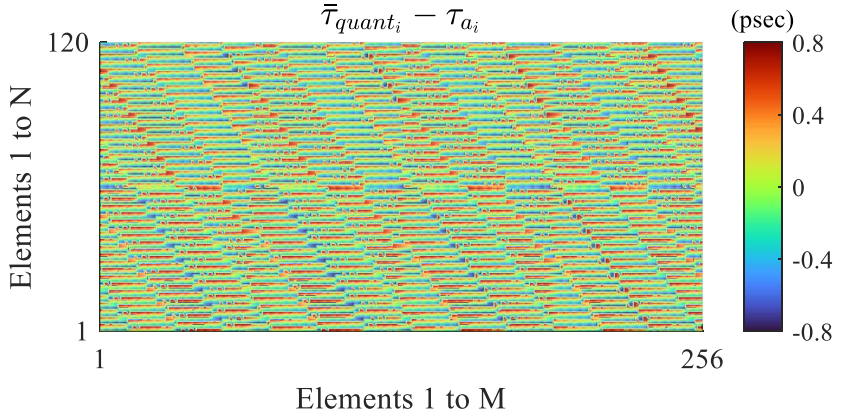

Figure A.9 Quantized delay error distribution for the TDU configurations of the architecture in Fig. 5.11 for a 256×120 element PAA steered to $\theta_{zx} = 60°$ and $\theta_{zy} = 30°$. Note that all element quantized error falls between ± 0.8 psec which satisfies the bounding $\pm\tau_{lsb_2}/2$ criteria.

compared to the lowest $\tau_{a_i} - TDU_{1_i} - TDU_{2_i}$ value in Fig. A.5 covered by each TDU on layer 3. This process is carried out and the result is shown in Fig. A.6 where there are 40 TDU settings shown within the TDU_{2_i} settings blocks as expected due to the 16-way divider in the x-dimension and 12-way divider in the y-dimension. At this point we have the TDU-A configuration settings for each TDU layer. Now, we must check the total error to ensure that it is bounded within $\pm\tau_{lsb_3}/2 = \pm 0.8$ psec. The first step is to find τ_{quant_i} for each element by summing the settings

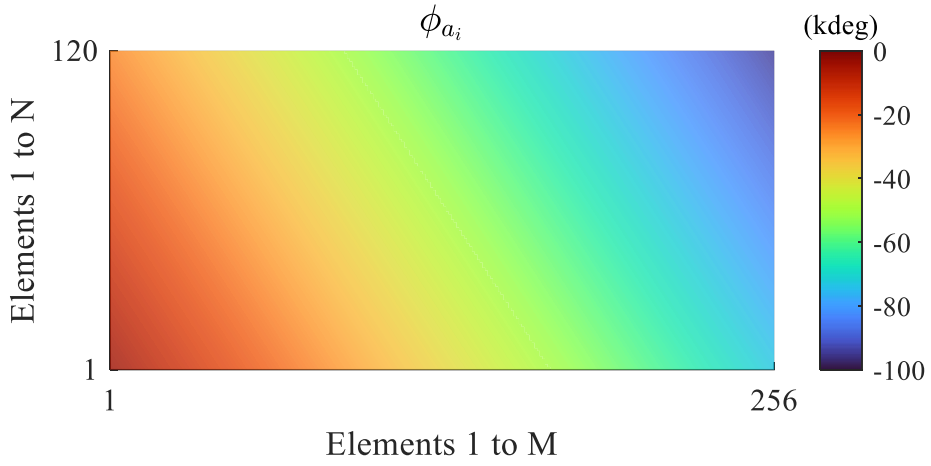

Figure A.10 Phase distribution for the TDU configurations of the architecture in Fig. 5.11 for a 256×120 element PAA steered to $\theta_{zx} = 60°$ and $\theta_{zy} = 30°$ at $f = 30$ GHz.

shown in Figs. A2, A4, and A6 which is shown in Fig. A7. As in the case for our linear example, we must normalize to the lowest value to find $\bar{\tau}_{quant_i}$ as shown in Fig. A.8. Secondly, we find the quantization error of each element which is shown in Fig. A.9 where it can be observed that each error is bounded by $\pm\tau_{lsb_3}/2 = \pm 0.8$ which means the TDU-A passes. The final step before we can plot the AF shown in Fig. 5.14 is to convert the τ_{quant_i} values into phase at the $f = 30$ GHz using the reverse of equation (A.3) as

$$\phi_{a_i} = -\tau_{quant_i} f_0 \, 360 \qquad (A.4)$$

which yields the phase excitations for each element shown in Fig. A.10 and together with equation (A.1) produces the AF shown in Fig. 5.14.

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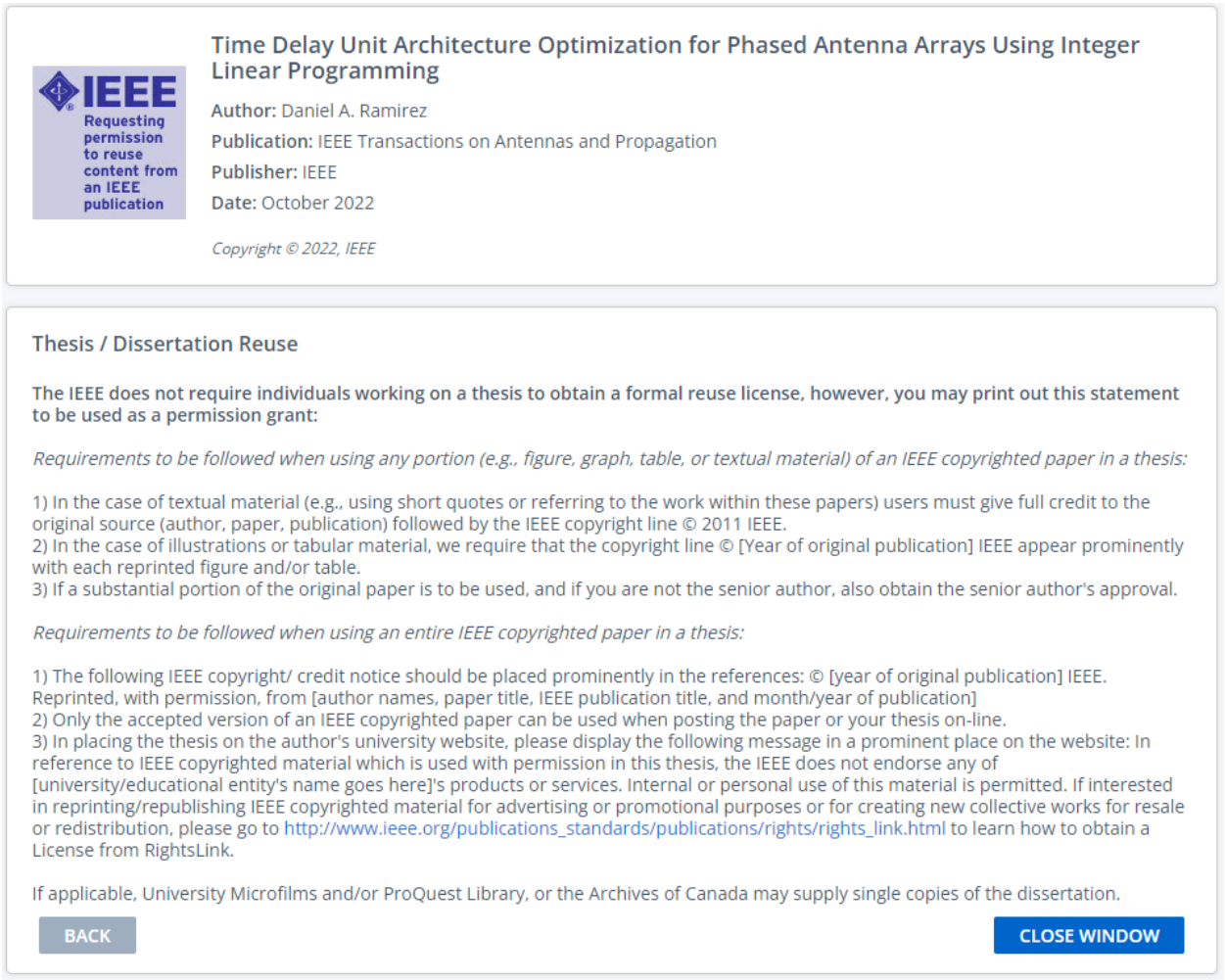

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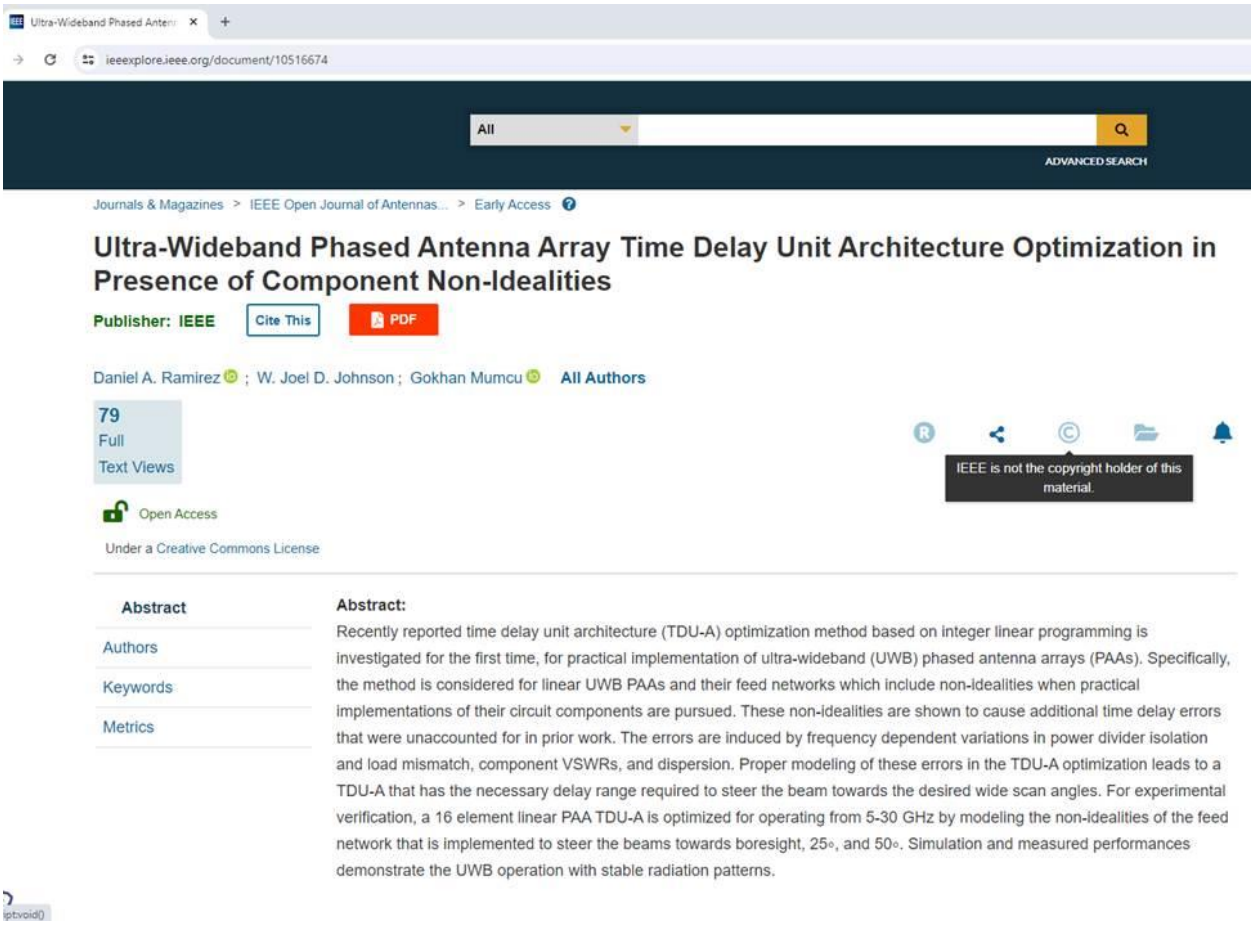
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Abstract:
Recently reported time delay unit architecture (TDU-A) optimization method based on integer linear programming is investigated for the first time, for practical implementation of ultra-wideband (UWB) phased antenna arrays (PAAs). Specifically, the method is considered for linear UWB PAAs and their feed networks which include non-idealities when practical implementations of their circuit components are pursued. These non-idealities are shown to cause additional time delay errors that were unaccounted for in prior work. The errors are induced by frequency dependent variations in power divider isolation and load mismatch, component VSWRs, and dispersion. Proper modeling of these errors in the TDU-A optimization leads to a TDU-A that has the necessary delay range required to steer the beam towards the desired wide scan angles. For experimental verification, a 16 element linear PAA TDU-A is optimized for operating from 5-30 GHz by modeling the non-idealities of the feed network that is implemented to steer the beams towards boresight, 25◦, and 50◦. Simulation and measured performances demonstrate the UWB operation with stable radiation patterns.

Appendix C: Example Derivations of the $\boldsymbol{A}$ and $\boldsymbol{K}$

C.1 Example Derivation for Variant 14 of the 8-Element Example of Chapter 2

A full derivation for the row of the $\boldsymbol{A}$ and $\boldsymbol{K}$ matrices and vector are shown here for the optimal TDU-A, variant 14. As a reminder, $\boldsymbol{b}$ is simply the requirement for the performance characteristics we care about, which leads to

$$\boldsymbol{b} = [\phi_{max} \quad \tau_{msb_{d=1}}^{max} \quad \tau_{msb_{d=2}}^{max} \quad \tau_{msb_{d=3}}^{max}] = [5° \quad 120\,psec \quad 60\,psec \quad 30\,psec]$$

To show how the $\boldsymbol{A}$ matrix is derived, we first find row 14 in the $\boldsymbol{\Psi}$ matrix which is

$$\boldsymbol{\Psi}(14) = [T_1 \quad T_2 \quad T_3 \quad b_1 \quad b_2] = [1 \quad 0 \quad 1 \quad 4 \quad 5]$$

Given for our example that $M_0 = 8$, $\theta_{max} = 60°$, and $f_{max} = 30\ GHz$ we can solve the entries for the $\boldsymbol{A}$ matrix. (Note, at 30 GHz wavelength $\lambda \cong 0.01m$)

$$M_1 = \frac{2M_{1-1}}{2^{d_1-d_0}} = \frac{16}{2^{1-0}} = 8$$

$$M_2 = \frac{2M_{2-1}}{2^{d_2-d_1}} = \frac{16}{2^{3-1}} = 4$$

$$h_1 = M_1 e_p \left(1 - \frac{1}{2^{d_1-d_{1-1}}}\right) = 8\left(\frac{\lambda}{2}\right)\left(1 - \frac{1}{2^{1-0}}\right) = 4\lambda\left(\frac{1}{2}\right) = 2\lambda$$

$$h_2 = M_2 e_p \left(1 - \frac{1}{2^{d_2-d_{2-1}}}\right) = 4\left(\frac{\lambda}{2}\right)\left(1 - \frac{1}{2^{3-1}}\right) = 2\lambda\left(\frac{3}{4}\right) = \frac{3\lambda}{2}$$

$$h_{scan_1} = h_1 \sin(\theta_{max}) = 2\lambda \sin(60) = 0.017\ m$$

$$h_{scan_2} = h_2 \sin(\theta_{max}) = \frac{3\lambda}{2}\sin(60) = 0.013\ m$$

$$\tau_{max_1} = \frac{h_{scan_1}}{c} + \tau_{qe_{1-1}} = \frac{0.017}{3 \times 10^8} + 0 = 57.74\,psec$$

$$\tau_{lsb_1} = \frac{\tau_{max_1}}{2^{b_1} - 1} = \frac{57.74}{2^4 - 1} = 3.85\, psec$$

$$\tau_{qe_1} = \frac{\tau_{lsb_1}}{2} = 1.92\, psec$$

$$\tau_{max_2} = \frac{h_{scan_2}}{c} + \tau_{qe_1} = \frac{0.013}{3 \times 10^8} + (1.92 \times 10^{-12}) = 45.29\, psec$$

$$\tau_{lsb_2} = \frac{\tau_{max_2}}{2^{b_2} - 1} = \frac{57.74}{2^5 - 1} = 1.46\, psec$$

$$\tau_{qe_2} = \frac{\tau_{lsb_2}}{2} = 0.73\, psec$$

$$\boldsymbol{a}_{\phi_e}(14) = \phi_{e,deg} = \left(\frac{\tau_{qe_2}}{\sqrt{3}} + \frac{\tau_{max_{L+1}}}{2}\right)(f_{max})(360) = \left(\frac{0.73 \times 10^{-12}}{\sqrt{3}} + \frac{0}{2}\right)(30 \times 10^9)(360)$$

$$= 4.5°$$

$$\boldsymbol{a}_{1_{msb}}(14) = \tau_{msb_{d_1=1}} = \tau_{lsb_1}(2^{b_1 - 1}) = 3.85(2^3) = 30.8\, psec$$

$$\boldsymbol{a}_{3_{msb}}(14) = \tau_{msb_{d_2=3}} = \tau_{lsb_2}(2^{b_2 - 1}) = 1.46(2^4) = 23.3\, psec$$

Note that since there is not a TDU on division level 2, $\boldsymbol{a}_{2_{msb}}(14) = \tau_{msb_2} = 0$. Therefore, the 14th row of the $\boldsymbol{A}$ matrix is

$$\boldsymbol{A}(14) = [\boldsymbol{a}_{\phi_e}(14) \quad \boldsymbol{a}_{1_{msb}}(14) \quad \boldsymbol{a}_{2_{msb}}(14) \quad \boldsymbol{a}_{3_{msb}}(14)]$$

$$= [4.5° \quad 30.8\, psec \quad 0.0\, psec \quad 23.3\, psec]$$

Finally, the 14th row of the $\boldsymbol{K}$ matrix is composed of the number of TDUs, the number of bits, and the phase error of the 14th variant of the $\boldsymbol{\Psi}$ matrix, by the following derivation.

$$\boldsymbol{m} = [2 \quad 4 \quad 8]$$

$$\boldsymbol{\eta}_{TDU}(14) = [\psi_1 \quad \psi_2 \quad \psi_3][2 \quad 4 \quad 8]^T = [1 \quad 0 \quad 1][2 \quad 4 \quad 8]^T = 10$$

$$\boldsymbol{\eta}_{bits}(14) = \sum_{l=1}^{2} \boldsymbol{m}(d_l) b_l = (2)(4) + (8)(5) = 48$$

As discussed earlier, the weighting vector is

$$[w_{TDU} \quad w_{bits} \quad w_{\phi}] = [1 \quad 0.1 \quad 0.001]$$

which leads us to the 14th row of $\boldsymbol{K}$ as

$$\boldsymbol{K}(14) = [w_{TDU} \quad w_{bits} \quad w_{\phi}][\boldsymbol{\eta}_{TDU} \quad \boldsymbol{\eta}_{\text{bits}} \quad \boldsymbol{a}_{\phi_e}]^T = [1 \quad 0.1 \quad 0.001]\begin{bmatrix}10\\48\\4.5\end{bmatrix}$$

$$= 10 + 4.8 + 0.0045 = 14.8045$$

C.2 Example Derivation for Variant 250 of the 10×6-Element Example of Chapter 2

A full derivation for the row of the $\boldsymbol{A}$ and $\boldsymbol{K}$ matrices and vector are shown here for the optimal TDU-A, variant 14. As a reminder, $\boldsymbol{b}$ is simply the requirement for the performance characteristics we care about, which leads to

$$\boldsymbol{b} = [\phi_{max}] = [5°]$$

To show how the $\boldsymbol{A}$ matrix is derived, we first find row 250 in the $\boldsymbol{\Upsilon}$ matrix which is $\boldsymbol{\Upsilon}_{250} =$

$$\left[[\boldsymbol{\Psi}_{\mathrm{x}}]_{1,1}[\boldsymbol{\Psi}_{\mathrm{x}}]_{1,2}[\boldsymbol{\Psi}_{\mathrm{x}}]_{1,3}\left[\boldsymbol{\Psi}_{\mathrm{y}}\right]_{1,1}\left[\boldsymbol{\Psi}_{\mathrm{y}}\right]_{1,2}\left[\boldsymbol{\Psi}_{\mathrm{y}}\right]_{1,3}[\mathbf{T}_{\mathrm{x}}]_{5,1}[\mathbf{T}_{\mathrm{x}}]_{5,2}[\mathbf{T}_{\mathrm{x}}]_{5,3}\left[\mathbf{T}_{\mathrm{y}}\right]_{4,1}\left[\mathbf{T}_{\mathrm{y}}\right]_{4,2}\left[\mathbf{T}_{\mathrm{y}}\right]_{4,3}[\mathbf{B}]_{7,1}[\mathbf{B}]_{7,2}\right]$$

$$= [\ 1 \quad 2 \quad 10 \quad 1 \quad 2 \quad 6 \quad 0 \quad 1 \quad 1 \quad 1 \quad 0 \quad 1 \quad 4 \quad 6]$$

Given for our example that $M_0 = 16$, $\theta_{max} = 64.34°$, and $f_{max} = 30\ GHz$ we can solve the entries for the $\boldsymbol{A}$ matrix. (Note, at 30 GHz wavelength $\lambda \cong 0.01m$)

$$M_1 = \frac{M_{l-1}}{\frac{[\boldsymbol{\Psi}]_{x_{v,d_{x_l}}}}{[\boldsymbol{\Psi}]_{x_{v,d_{x_{l-1}}}}}} = \frac{M_0}{\frac{[\boldsymbol{\Psi}]_{250,d_{x_1}}}{[\boldsymbol{\Psi}]_{250,d_{x_0}}}} = \frac{10}{\frac{2}{1}} = 5$$

$$M_2 = \frac{M_{l-1}}{\frac{[\boldsymbol{\Psi}]_{x_{v,d_{x_l}}}}{[\boldsymbol{\Psi}]_{x_{v,d_{x_{l-1}}}}}} = \frac{M_1}{\frac{[\boldsymbol{\Psi}]_{250,d_{x_2}}}{[\boldsymbol{\Psi}]_{250,d_{x_1}}}} = \frac{5}{\frac{10}{2}} = 1$$

$$N_1 = \frac{N_{l-1}}{\frac{[\boldsymbol{\Psi}]_{y_{v,d_{y_l}}}}{[\boldsymbol{\Psi}]_{y_{v,d_{y_{l-1}}}}}} = \frac{N_0}{\frac{[\boldsymbol{\Psi}]_{250,d_{y_1}}}{[\boldsymbol{\Psi}]_{250,d_{y_0}}}} = \frac{6}{\frac{1}{1}} = 6$$

$$N_2 = \frac{N_{l-1}}{\frac{[\boldsymbol{\Psi}]_{y_{v,d_{y_l}}}}{[\boldsymbol{\Psi}]_{\boldsymbol{y}_{v,d_{y_{l-1}}}}}} = \frac{N_1}{\frac{[\boldsymbol{\Psi}]_{250,d_{y_2}}}{[\boldsymbol{\Psi}]_{250,d_{y_1}}}} = \frac{6}{\frac{6}{1}} = 1$$

$$h_{x_1} = M_{l-1}e_p\left(1 - \frac{1}{\frac{[\boldsymbol{\Psi}]_{x_{v,d_{x_l}}}}{[\boldsymbol{\Psi}]_{x_{v,d_{x_{l-1}}}}}}\right) = M_0 e_p\left(1 - \frac{1}{\frac{[\boldsymbol{\Psi}]_{250,d_{x_1}}}{[\boldsymbol{\Psi}]_{250,d_{x_0}}}}\right) = 10\left(\frac{\lambda}{2}\right)\left(1 - \frac{1}{2/1}\right) = \frac{5\lambda}{2}$$

$$h_{x_2} = M_{l-1}e_p\left(1 - \frac{1}{\frac{[\boldsymbol{\Psi}]_{x_{v,d_{x_l}}}}{[\boldsymbol{\Psi}]_{x_{v,d_{x_{l-1}}}}}}\right) = M_1 e_p\left(1 - \frac{1}{\frac{[\boldsymbol{\Psi}]_{250,d_{x_2}}}{[\boldsymbol{\Psi}]_{250,d_{x_1}}}}\right) = 5\left(\frac{\lambda}{2}\right)\left(1 - \frac{1}{10/2}\right) = 2\lambda$$

$$h_{y_1} = N_{l-1}e_p\left(1 - \frac{1}{\frac{[\boldsymbol{\Psi}]_{y_{v,d_{y_l}}}}{[\boldsymbol{\Psi}]_{\boldsymbol{y}_{v,d_{y_{l-1}}}}}}\right) = N_0 e_p\left(1 - \frac{1}{\frac{[\boldsymbol{\Psi}]_{250,d_{y_1}}}{[\boldsymbol{\Psi}]_{250,d_{y_0}}}}\right) = 6\left(\frac{\lambda}{2}\right)\left(1 - \frac{1}{1/1}\right) = 0$$

$$h_{y_2} = N_{l-1}e_p\left(1 - \frac{1}{\frac{[\boldsymbol{\Psi}]_{y_{v,d_{y_l}}}}{[\boldsymbol{\Psi}]_{\boldsymbol{y}_{v,d_{y_{l-1}}}}}}\right) = N_1 e_p\left(1 - \frac{1}{\frac{[\boldsymbol{\Psi}]_{250,d_{y_2}}}{[\boldsymbol{\Psi}]_{250,d_{y_1}}}}\right) = 6\left(\frac{\lambda}{2}\right)\left(1 - \frac{1}{6/1}\right) = \frac{5\lambda}{2}$$

$$h_{scan_1} = \sqrt{h_{x_l}^2 + h_{y_l}^2}\sin(\theta_{max}) = \sqrt{\left(\frac{5\lambda}{2}\right)^2 + 0^2}\ \sin(64.34) = 0.023\ m$$

$$h_{scan_2} = \sqrt{h_{x_l}^2 + h_{y_l}^2}\sin(\theta_{max}) = \sqrt{(2\lambda)^2 + \left(\frac{5\lambda}{2}\right)^2}\ \sin(64.34) = 0.029\ m$$

$$\tau_{max_1} = \frac{h_{scan_1}}{c} + \tau_{qe_{1-1}} = \frac{0.023}{3 \times 10^8} + 0 = 76.67\ psec$$

$$\tau_{lsb_1} = \frac{\tau_{max_1}}{2^{b_1} - 1} = \frac{76.67}{2^4 - 1} = 5.11\ psec$$

$$\tau_{qe_1} = \frac{\tau_{lsb_1}}{2} = 2.55\ psec$$

$$\tau_{max_2} = \frac{h_{scan_2}}{c} + \tau_{qe_1} = \frac{0.029}{3 \times 10^8} + (2.55 \times 10^{-12}) = 99.22\ psec$$

$$\tau_{lsb_2} = \frac{\tau_{max_2}}{2^{b_2} - 1} = \frac{99.22}{2^6 - 1} = 1.57\ psec$$

$$\tau_{qe_2} = \frac{\tau_{lsb_2}}{2} = 0.79\ psec$$

$$\boldsymbol{a}_{\phi_e}(250) = \phi_{e,deg} = \left(\frac{\tau_{qe_2}}{\sqrt{3}} + \frac{\tau_{max_{L+1}}}{2}\right)(f_{max})(360) = \left(\frac{0.79 \times 10^{-12}}{\sqrt{3}} + \frac{0}{2}\right)(30 \times 10^9)(360)$$

$$= 4.9°$$

Therefore, the 250th row of the $\boldsymbol{A}$ matrix is

$$\boldsymbol{A}(250) = [\boldsymbol{a}_{\phi_e}(250)] = [4.9°]$$

Finally, the 250th row of the $\boldsymbol{K}$ matrix is composed of the number of TDUs, the number of bits, and the phase error of the 250th variant of the $\boldsymbol{\Psi}$ matrix, by the following derivation.

$$\boldsymbol{\eta}_{TDU}(250) = \sum_{l=1}^{2} [\boldsymbol{\Psi}]_{x_{250,d_{x_l}}} [\boldsymbol{\Psi}]_{y_{250,d_{y_l}}} = (2)(1) + (10)(6) = 62$$

$$\boldsymbol{\eta}_{TDU}(250) = \sum_{l=1}^{2} [\boldsymbol{\Psi}]_{x_{250,d_{x_l}}} [\boldsymbol{\Psi}]_{y_{250,d_{y_l}}} [\boldsymbol{B}]_{250,l} = (2)(1)(4) + (10)(6)(6) = 368$$

As discussed earlier, the weighting vector is

$$[w_{TDU} \quad w_{bits} \quad w_{\phi}] = [1 \quad 0.01 \quad 0.001]$$

which leads us to the 14th row of $\boldsymbol{K}$ as

$$\boldsymbol{K}(14) = [w_{TDU} w_{bits} w_{\phi}][\boldsymbol{\eta}_{TDU} \boldsymbol{\eta}_{\text{bits}} \boldsymbol{\alpha}_{\phi_e}]^T = [1 \quad 0.01 \quad 0.001] \begin{bmatrix} 62 \\ 368 \\ 4.9 \end{bmatrix} = 62 + 3.68 + 0.0049$$

$$= 65.6849$$

About the Author

Daniel Ramirez received the B.S. degree in electrical engineering from the University of Central Florida, Orlando, FL, USA in 2013, and the M.S. degree in electrical engineering from the University of South Florida, Tampa, FL, USA in 2017. His research has been focused on the architecting of hierarchical time delay configurations. He has completed this research under the funding provided by L3Harris Technologies, Inc. His publication record includes two journal articles and five total patents (some patents pending). He has been employed at L3Harris Technologies since 2013 and is a member of the IEEE Antenna Propagation Society (AP-S) and the Microwave Theory and Techniques Society (MTT-S).