October 2021

Development of Small-Scale Power Supplies for Wearable Medical Diagnostic Devices

Donny Stiner
University of South Florida

Development of Small-Scale Power Supplies for Wearable Medical Diagnostic Devices

by

Donny Stiner

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Electrical Engineering
Department of Electrical Engineering
College of Engineering
University of South Florida

Co-Major Professor: Arash Takshi, Ph.D.
Co-Major Professor: Ashwin Parthasarathy, Ph.D.
Sylvia Thomas, Ph.D.

Date of Approval:
October 18, 2021

Keywords: Power Management, Wearables,
Voltage Regulator, Power Efficiency, Printed Circuit Board Assembly Methods

Dedication

This thesis is dedicated to my beloved parents, Vicki and Alan, who successfully provided me with the means to pursue a fruitful and happy life. Also, to my valued brother Kevin, who made sure I grew up surrounded by science fiction and sparked my interest in engineering as a career. Finally, to my dearest girlfriend Bianca, who supported me to further expand my academic horizons and pursue a graduate level degree. You all have revealed to me the potential I can achieve if I just set my mind to the task and think outside the box. Thank you all for your endless love, sacrifices, and support.

Acknowledgments

The completion of this thesis would not have been possible if not for the guidance of my advisor, Dr. Arash Takshi. His expertise proved invaluable in the progression of the project, and he provided the tools to develop the project in a laboratory setting. I also wish to extend my thanks to my co-supervisor Dr. Ashwin Parthasarathy for his helpful knowledge in the subject area and agreeing to include me in this project's work. I also want to extend my gratitude to Arindam Biswas for his invaluable advice and consistent availability to answer inquiries when needed. Furthermore, I wish to express my appreciation for Dr. Sylvia Thomas and her continued support throughout my graduate career.

Table of Contents

List of Tables

List of Figures

Abstract

As devices continue the trend of becoming increasingly smaller in scale to allow for wearability, the power supply modules driving these technologies will in turn become reduced in size as well. This progression will call for advanced techniques to fabricate power supplies on wearable device platforms which still permit the circuit to operate effectively. One such crucial technique, which is discussed in this thesis, is the implementation of power saving measures to increase battery lifespan on wearable devices.

Equipment found in the medical field today can be quite bulky and require inconvenient means of transportation and take up an excessive amount of space. Thus, the medical industry is booming with a demand for wearable small scale devices to be used as medical diagnostic equipment. This study takes a closer look at the development of a power supply design for a wearable medical diagnostic device. This apparatus utilizes Speckle-plethysmography to effectively analyze the cardiovascular health of the patient, and therefore must utilize a relatively noise-free and battery operated power supply to function properly.

Chapter 1: Introduction

1.1 Overview

Wearable technologies have drastically grown in popularity among the public and are becoming an increasingly common occurrence in the day to day lives of the average individual. With products ranging from fitness tracking watches to navigational eye wear, the appeal to many consumers lies in the innovativeness of such devices. With today's wearable technologies, someone wearing a smart watch can schedule a calendar event using their voice. Equally, someone wearing smart glasses could be given navigational assistance on their heads-up display. These are just a couple of advantages seen from such devices and the possibilities are seemingly endless.

Furthering the development of wearables is the expansion of wearable medical diagnostic devices. One instance where this can be seen in action can be found in modern day smartwatches which can monitor your sleeping habits, track your fitness activity, and even measure your heart rate. There are even developments into using these wearable technologies to remotely monitor patients from home in between visits with their medical team [1]. The convenience of all of your medical diagnostic data at your fingertips is an attractive concept for many and thus grows the demand for wearable products even more so.

Market trends also show a positive outlook for wearable technologies and have even predicted that the market size for the industry will exceed one-hundred billion dollars by 2023 [2]. This positive market trend both ranging from the years of 2015 to 2026 can

be graphically depicted in Figure 1.1 [2]. With such a rapid potential for growth, the motivation behind researching wearable technologies strengthens further.

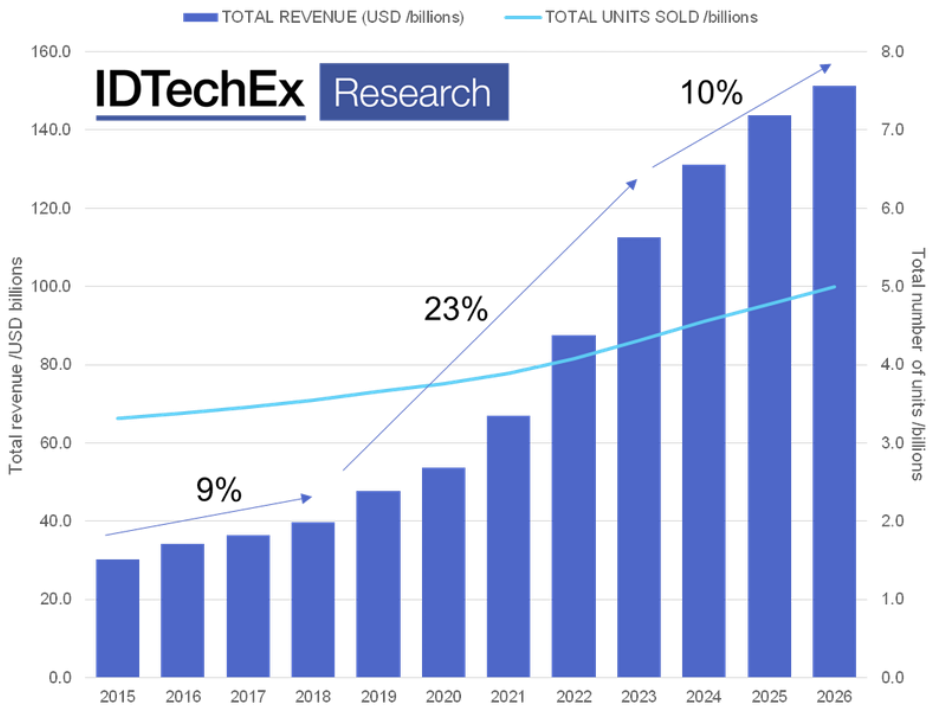


Figure 1.1: Global market predictions for wearable technologies from 2015 to 2026. Reprinted from “Wearable Technology 2017-2027: Markets, Players, Forecasts” by James Hayward, retrieved: https://www.idtechex.com/en/research-report/wearable-technology-2017-2027-markets-players-forecasts/536 Reprinted with permission. [2]

While the potential of wearables is certainly promising, there are still challenges which must be overcome. Many wearable technology companies are focused on providing users with ergonomically comfortable designs and digital security in an IoT market. Most notably however is the problem pertaining to energy consumption, which is regarded as being, “one of the most critical challenges in wearable computing.” [3]. Making devices both wearable and power efficient can be a daunting task for a variety of reasons. Factors such as thermal dissipation and compact layouts can force certain design parameters to fall out of desired ranges quite easily, so the balance between efficiency and functionality must be prioritized.

Many designs have been proposed that attempt to address this widespread issue. One such design includes a thermoelectric power source which can utilize the heat produced by our bodies to power any wearable devices the consumer may have directly positioned on their skin [4]. Other power supply designs, much more like the one to be created in this project, use a battery as a power source and implement a creative design to replenishing battery life. For instance, a Texas Instruments design from 2016 installed a wireless charging module to allow for a more compact and simplified product [5]

1.2 Thesis Objective

Wearable technology has changed aspects of many of our lives in a positive way, but its continued development efforts must tackle the problems it faces such as the lack of power efficiency. This thesis attempts to address a host of challenges associated with the design process such as on-board thermal management, placement of components, and use of integrated circuit feedback systems. This thesis also guides the reader through the development of a small-scale power supply from start to finish that is intended for installation on a wearable device platform.

Specifically, the wearable platform this power supply design will be utilized for is a wrist mounted apparatus devised by the researchers at Translational Optics Imaging & Spectroscopy Lab (TROPICS) at the University of South Florida. This device will be capable of utilizing speckleplethysmography (SPG) to shed light on the cardiovascular health of the device user, in a similar manner to devices which utilize photoplethysmography (PPG). SPG and PPG are both measurement methodologies that involve using a concentrated light and photoreceptor to record reflected light from tissues in the human body. An important reason for choosing to employ SPG rather than PPG

lies in a number of critical output waveform advantages including more favorable overall harmonic content which produces less noisy output signals [6]. There have even been reports demonstrating how SPG analysis results in more accurate output waveforms when the user is under excessive physical stress, such as one might be when exercising [7].

Consequently, it is important to note that the design for the SPG analysis circuit falls outside the scope of this research and will not be discussed in detail. Curious readers are encouraged to follow the publications from TROPICS, including the article which covers this measurement methodology in more detail [8]. As far as physical design is concerned, this thesis discusses only the portions of the SPG sensing circuit that is directly powered by the designed power supply circuit. The end goal of the project is to design and fabricate a wearable, space and energy efficient battery-operated circuit which incorporates the power supply design as well as the required components to generate signals for the analysis of SPG waveforms. A process block flow diagram depicting this desired system can be observed in Figure 1.2 for further clarity.

This thesis covers the design and test results of a prototype power supply circuit for the proposed SPG analysis system. In chapter 2, the characterization of a selection of voltage regulators will be explored to determine if frequency harmonics are problematic in any future power supply circuit designs. Also in chapter 2, the PSpice model will be used to reaffirm the proper operation of the current limiting feedback circuit. Both of these sections in chapter 2 will be crucial in determining any preliminary design considerations before fabrication of the final power supply circuit prototype. Chapter 3 will describe the design, assembly, and testing of the final circuit schematic. Finally, chapter 4 will wrap up

the discussion with a conclusion and deliberate on a number of future design considerations which may enhance the project overall.

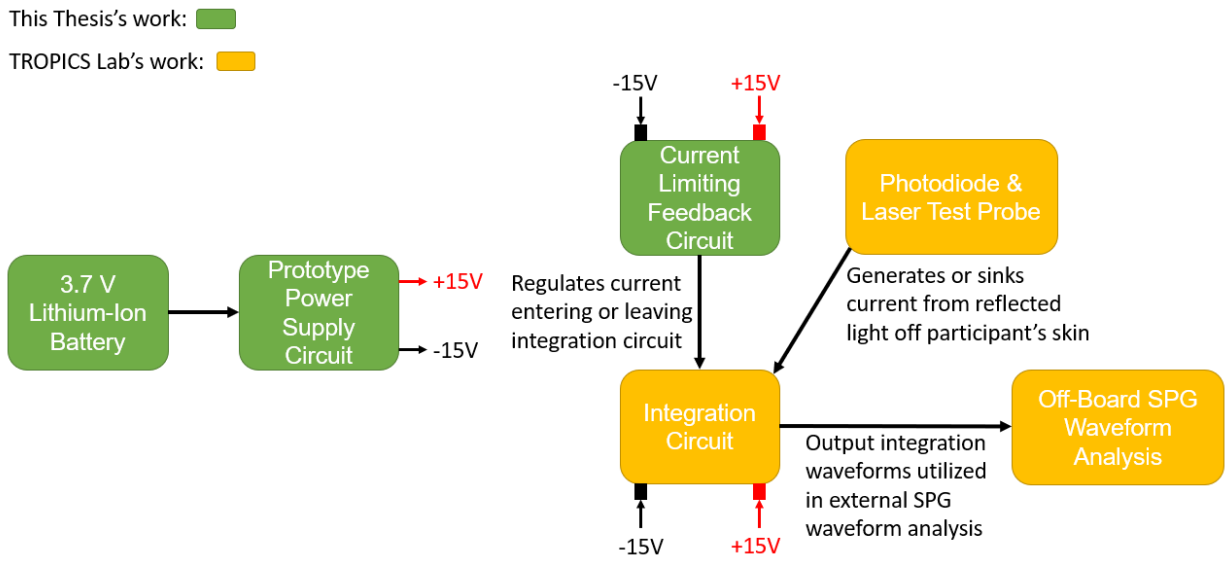


Figure 1.2: Thesis process flow block diagram

Chapter 2: Preliminary Design Considerations

2.1 Characterization of Linear and Switching Regulators

When attempting to record the output signals of a sensor device, it is important to have a high signal to noise ratio. In other words, one must verify that there are no interfering signals being combined with the desired signals distorting the sensing results and giving invalid data. While shielding sensors from external noises is required, a serious design challenge is to protect the signal from any internal interferences, particularly from the circuit power supply. A direct effect from power supplies is a phenomenon known as frequency harmonics. Frequency harmonics are specific frequencies located at multiples of the fundamental frequency of the signal. These harmonics can distort the fundamental waveform of the signal, thus giving cause to inaccurate output signal readings.

A large portion of modern day power supplies utilize some form of switching mechanism to operate properly. These switching power supplies are more compact and energy efficient than their relative counterparts, such as linear power supplies, and are thus ideal for wearable technologies. As identified by Zhu et al., however, switching power supplies are the main damaging source effecting energy quality [9]. These harmful qualities can be pinpointed to the harmonic components produced by the switching power supply's internal components. With this in mind, it is even more crucial the potential negative consequences of these frequency harmonics be analyzed to protect the designed system.

In order to identify if these harmonics impede the path to reliable output results, the fast Fourier transform (FFT) of two switching and one linear DC-DC converter power supply chip were studied in this work. The FFT analysis converts a time domain waveform into a frequency domain Fourier series signal. Through this converted waveform, signal characteristics of any existing frequency harmonics can be identified for the two different power supply designs [10]. Thus, this analysis can help determine which type of power supply would be best suited for the wrist mounted device. Additionally, one could assess the output voltage waveform of both types of power supplies and determine which type has a more desirable signal to noise ratio for the application.

2.1.1 Characterization Experimental Setup

The experiment consisted of testing three separate DC-DC converters, two of which were a switching power supply type and one which was a linear power supply. The two switching power supply models utilized XL6009 and MT3608 chips, both of which are boost converter modules. The linear power supply utilized the LM317 voltage regulator chip. All power supplies were tested both with and without a 750 Ω resistor load in order to investigate if there were any harmonics present on the board without being connected to any external circuit. Testing with the load resistor also further emphasizes any noise that may be present at the output and allow us to get an estimate for what the peak to peak voltage may be for each chip. The 750 Ω load resistance was obtained by an analysis of the total current flow found in the PSpice simulation associated with this project. The simulation determined that the total current required by the circuit would be 17.74 mA. Therefore, an estimated load resistance can be found by dividing the maximum voltage of 15 V by 20 mA. Figures 2.1 and 2.2 can be referenced to become oriented with

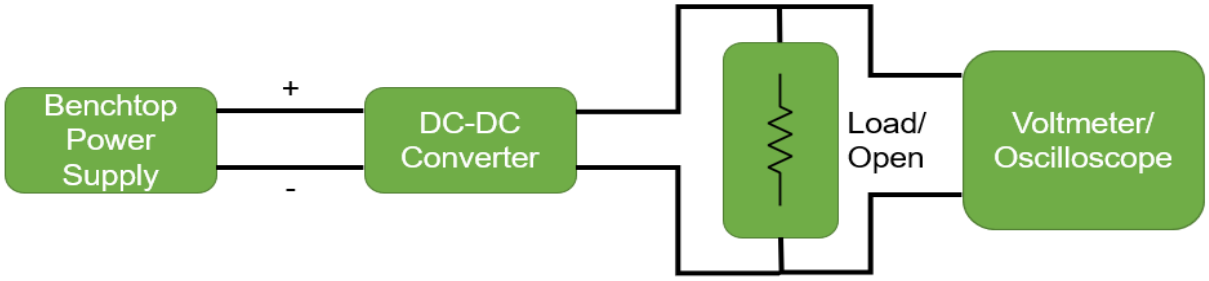


Figure 2.1: Diagrammatic representation of voltage regulator experimental setup

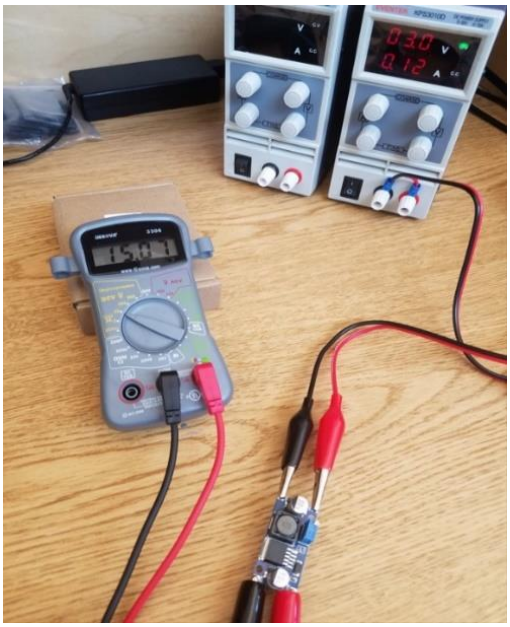


Figure 2.2: In-lab experimental setup for the off-the-shelf XL6009 DC-DC converter module under no load conditions

the experimental setup. A benchtop power supply was used to provide a potential to the DC-DC converter under testing. The converter was then either tested under the open-circuit mode to represent a no load condition or connected to the 750 Ω resistor to represent a loaded condition. In parallel to this connection, a voltmeter or oscilloscope was connected to allow readings of the output voltage/waveform and perform an FFT analysis on the output system signal. The target voltage at the output of the DC-DC converter in this experiment was 15 V.

2.1.2 Characterization Results

The results obtained from these experiments yielded some promising results which dictated the direction of the future power supply design. The first DC-DC converter module tested was a MT3608 circuit that was purchased from Dorhea through Amazon. Figures 2.3 through 2.6 depict the oscilloscope screenshots obtained for the MT3608 circuit under load and no load conditions.

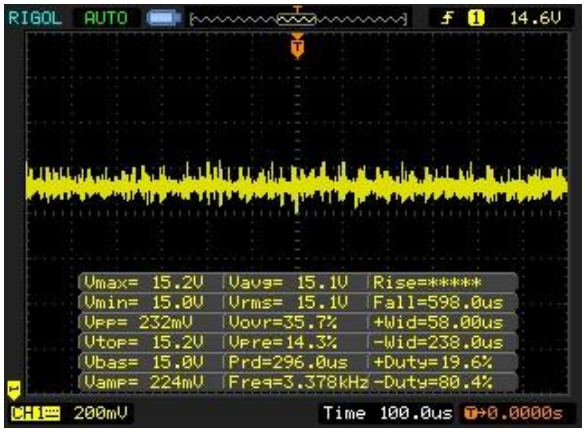


Figure 2.3: Output voltage waveform with no load conditions for MT3608

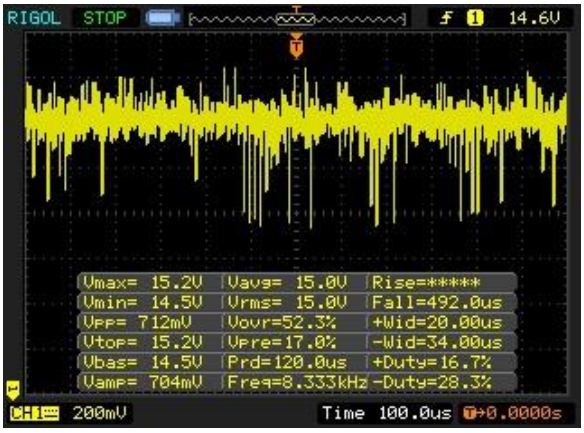


Figure 2.4: Output voltage waveform with load conditions for MT3608

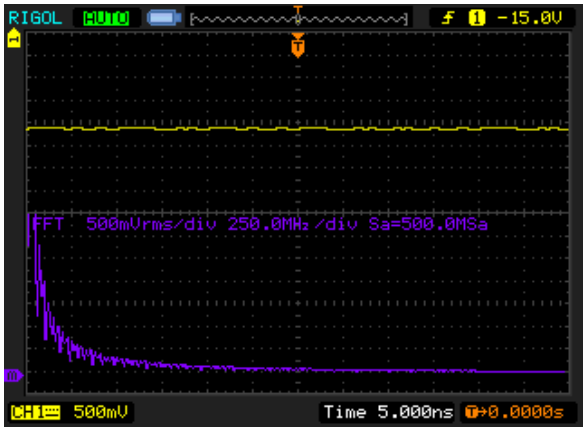


Figure 2.5: Output FFT analysis with no load conditions for MT3608

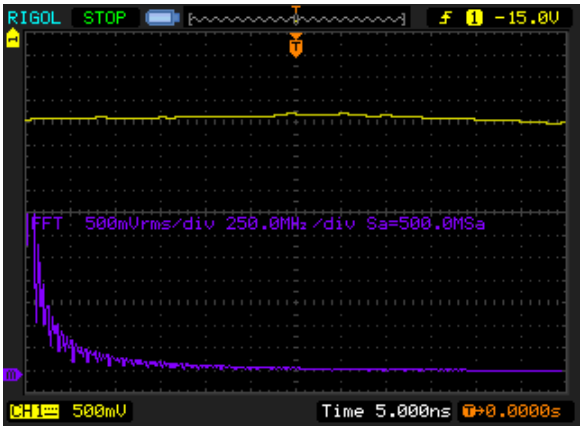


Figure 2.6: Output FFT analysis with load conditions for MT3608

Evaluating the captured screenshots of the oscilloscope, one noticeable change is the difference between the load and no load conditions of the experiment. When the MT3608 was placed under load conditions, the peak to peak voltage increased from 232 mV to 712 mV, nearly half a volt difference. Even with this notable change however, the FFT analysis did not become altered by the introduction of the load condition. Additionally, both FFT analyses remained largely identical irrespective of the presence of a load and any there were no visible frequency harmonics with significant amplitudes to cause concern.

Next up, the XL6009 converter module from DZS Electronics was tested under the same conditions as the MT3608 module. Figures 2.7 through 2.10 depict the oscilloscope screenshots obtained for the XL6009 under load and no load conditions. Similar to the MT3608 converter, the XL6009 module showed a change in the peak to peak voltage when introduced to the load resistor. However, the peak to peak voltage was lower on average overall between the load and no load conditions. Notably, the FFT analysis revealed similar harmonic characteristics to the MT3608.

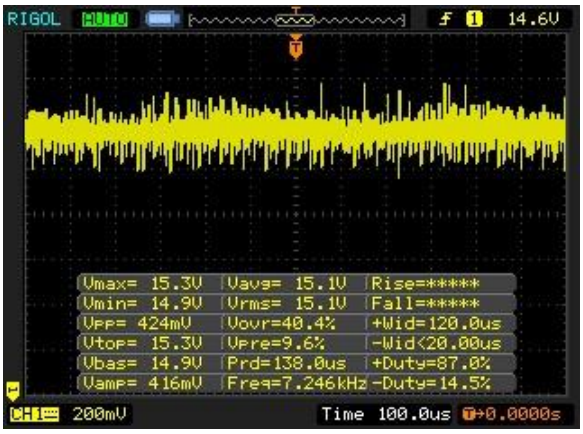


Figure 2.7: Output voltage waveform with no load conditions for XL6009

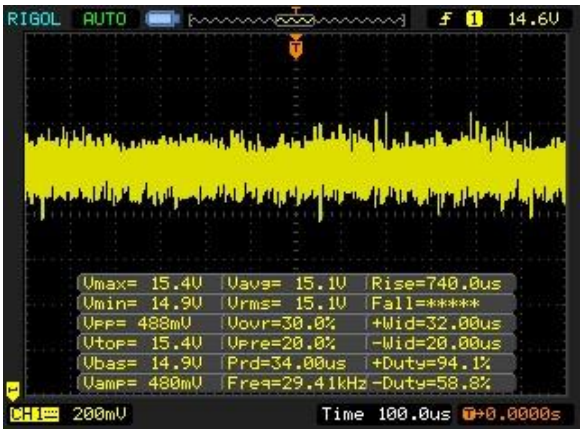


Figure 2.8: Output voltage waveform with load conditions for XL6009

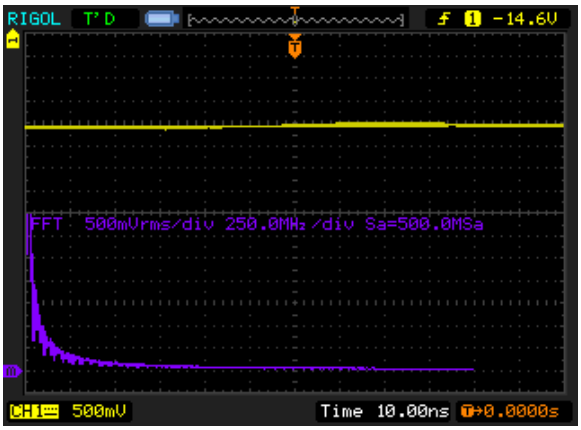


Figure 2.9: Output FFT analysis with no load conditions for XL6009

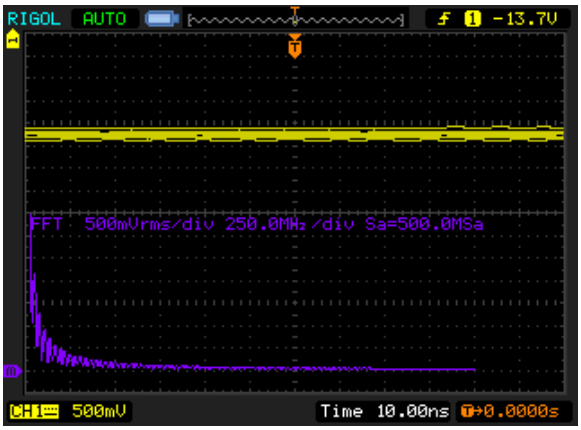


Figure 2.10: Output FFT analysis with load conditions for XL6009

With the two switching power supplies characterized, it is important to make a distinction between both of their fixed switching frequencies. Given the nature of this project, the most desirable switching frequency is that which allows us to create the most compact circuit design. To meet this end, higher switching frequencies were prioritized as this results in size reductions to the regulator integrated circuit (IC) overall [11]. It's important to note however that the balanced tradeoff between smaller IC size and reductions in efficiency was closely monitored during the design phase.

In an effort to identify the most effective converter to meet the requirements of the wearable PCB design, a closer look at the fixed switching frequency of the two converters is required. The MT3608 utilizes a fixed switching frequency of 1.2 MHz while the XL6009 operates at a fixed switching frequency of only 400 kHz. While there is a larger difference between the maximum and minimum voltages of the MT3608 compared to the XL6009, the peak to peak voltage is still minimal enough that it will not likely interfere with base operations of the design. With this in mind, a relevant design consideration was to find a

DC-DC converter chip that would utilize a switching frequency similar in value to 1.2 MHz to construct a more compact circuit layout.

Moving onto the final DC-DC converter, the oscilloscope screenshots pertaining to the linear LM317 module from Stemedu can be seen in Figures 2.11 through 2.14. One significant difference in the linear regulator compared to the switching regulator was the reduction in peak to peak voltage. This can likely be explained by the lack of a switching based circuit element to provide the pulse width modulated signal controlling the

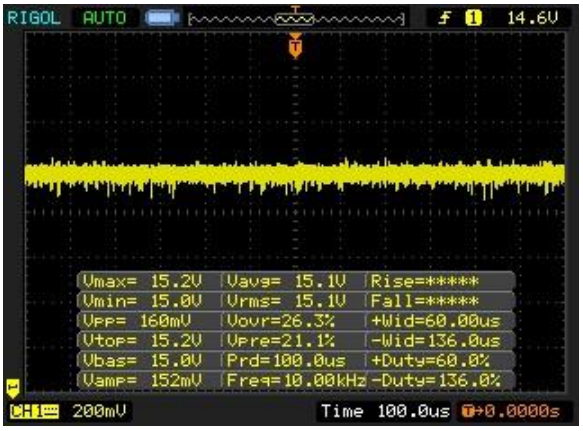


Figure 2.11: Output voltage waveform with no load conditions for LM317

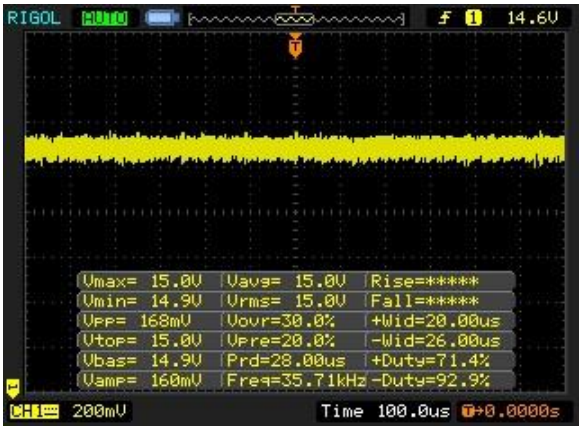


Figure 2.12: Output voltage waveform with load conditions for LM317

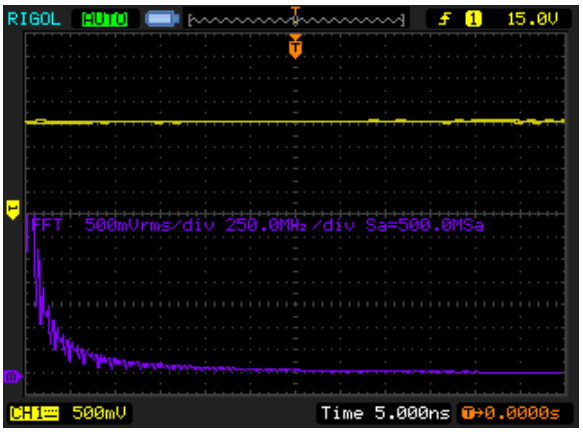


Figure 2.13: Output FFT analysis with no load conditions for LM317

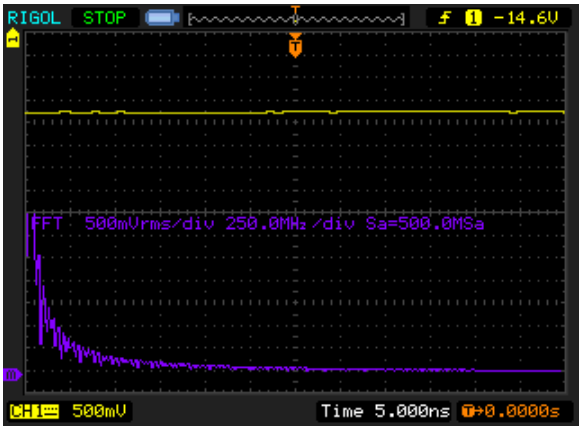


Figure 2.14: Output FFT analysis with load conditions for LM317

operations of the circuit. This switching mechanism can produce a lot of noise as well as electromagnetic interference [12], thus distorting the output waveform to a degree and giving the switching regulator a higher peak to peak voltage.

For the linear regulator, the FFT analysis revealed frequency harmonics in a nearly identical structure to those analyzed with the switching regulators. Taking this into consideration, it can be hypothesized that the frequency harmonics for a switching regulator will not cause any major complications for the design circuit. This is probable as long as they operate within the frequencies showing little to no amplitude in the FFT analysis depicted in this section. Thus, it can be safe to assume that a switching regulator can be utilzed in the final design to provide the proper voltage biases for the circuit.

Table 2.1 depicts the overall findings for all three regulators in this experiment. The crucial numerical factors worth mentioning are the peak to peak voltage and the average voltage of each waveform. Summariliy, the LM317 regulator module produced the smallest peak to peak voltage, the MT3608 generated the largest peak to peak voltage and all three regulators displayed an output voltage waveform of 15 V +/- 0.1 V.

Table 2.1 Summary of Regulator Characterization Results

Voltage Regulator Identification	Peak to Peak Max Voltage (No Load)	Peak to Peak Max Voltage (Load)	Average Voltage
MT3608	232 mV	712 mV	15.05 V
XL6009	424 mV	488 mV	15.1 V
LM317	160 mV	168 mV	15.05 V

Through the characterization of these voltage regulators, signifigant progress was achievable in identifying key design characteristics which must be incorporated into the final power supply design. It was uncovered that a higher switching frequency, though slightly decreasing effeciency of the regulator and minimally increasing the output voltage waveform peak to peak values, was still prefereable as it allowed for the chip package to become more viable for a wearble technology platform. Furthermore, it was realized that the switching regulator frequency harmonics were identical to that of the linear regulator. Thus, it was concluded that a switching regulator would not negatively affect the quality of the output waveform.

2.2 PSpice Simulation

Another aspect of this project which heeds mentioning is the development of the PSpice simulations for the overall circuit before PCB development. The software used to develop these simulations was OrCAD Capture with PSpice version 17.4. Through these models, a multitude of important design considerations, such as power consumption, were discovered and subsequently incorporated into the final circuit model. In addition to this, the simulation acted as a reassurance that the circuit would behave as anticipated after fabrication of the circuit.

It is worth noting that there are two PSpice simulation models and as such there are two PCB configurations associated with these models. The reason being for two designs lies in the desire to allow for flexibility of the operation of the circuit. The SPG analysis utilizes an integrator chip to formulate its readings for each test. Seeing as how it is possible to obtain the same output by integrating over the input signal in either a positive or negative fashion, it was decided that the overall design shall have a layout

which allows for both modes of integration. This is a useful feature for future experimentation as the researcher may want to investigate the difference, if any, that may exist between integrating over the input signal in the positive integration mode versus the negative integration mode.

2.2.1 Design of Current Limiting Feedback Circuit

A critical component that the final design circuit must implement is the current limiting feedback circuit, which will be identified as the feedback circuit for the remainder of this thesis. This circuit utilizes a closed loop architecture which describes a system where the operational amplifier output is fed back into its own input [13]. This feedback circuit is capable of setting and maintaining a voltage bias across a set resistance in order to draw the required amount of current away or to the SPG analysis circuit. This reduction or addition of current is crucial to the operation of the analysis circuit, as the photodiode used in the SPG analysis has a varying amount of generated current. Thus, the feedback circuit compensates for this fluctuation of current and ensures that the output results remain desirable.

Figures 2.15 and 2.16 can be used as a reference for closer inspection of the PSpice simulation models in both of its respective integration mode configurations. The overall layout of both circuits is more or less the same save for a few minor adjustments. For instance, the polarity of the LM336 and the photodiode are flipped depending on the desired integration method. Additionally, the MOSFET tied to the output off the LM324 amplifier changes from the 2N7002 N-channel transistor for the negative integration to the BS250 P-channel transistor for the positive integration. Therefore, when explaining

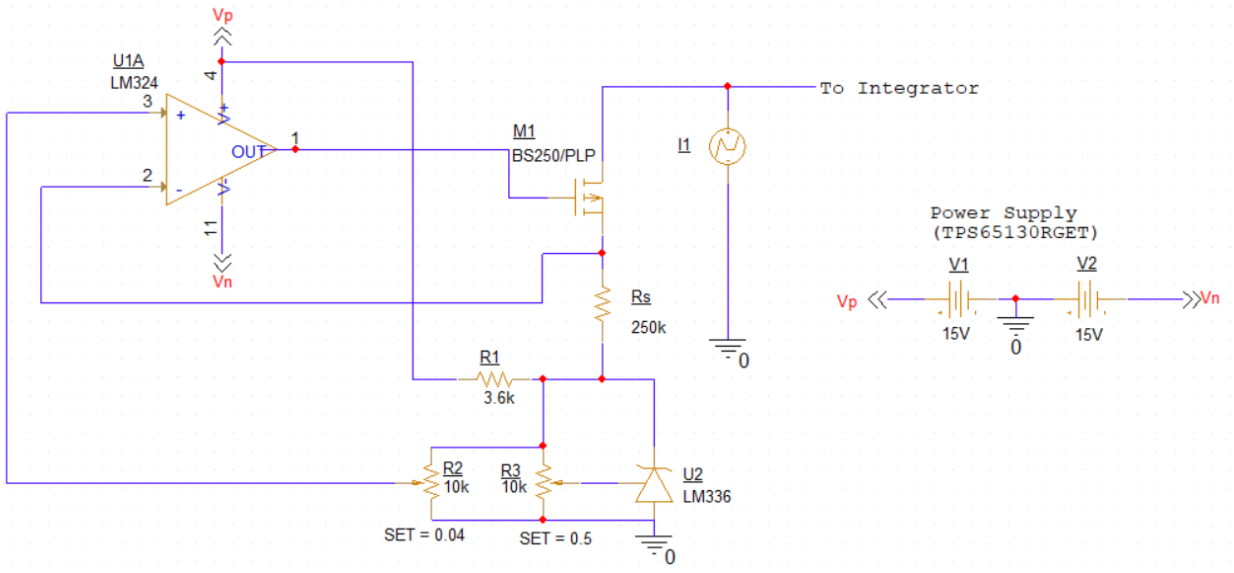


Figure 2.15: Circuit diagram for negative integration layout scheme

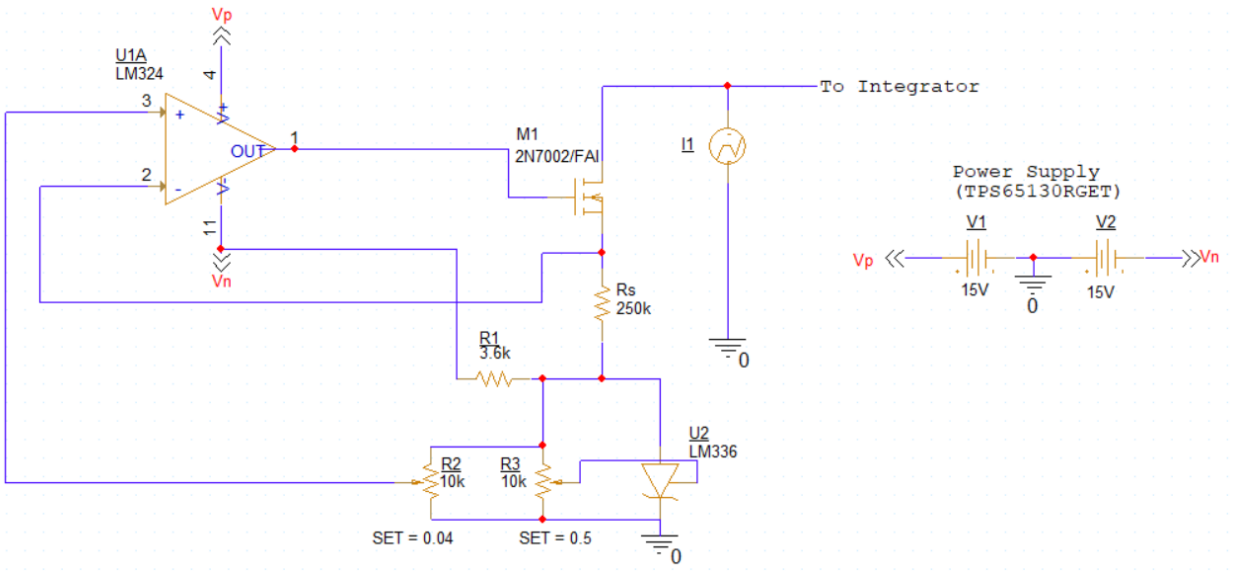


Figure 2.16: Circuit diagram for positive integration layout scheme

the operation of these designs in further detail, the components on-board can be generalized. It is important to note, that the LM324 chip will not be placed on the future PCB design but rather the LM321. This version of OrCAD Capture did not possess the

LM321 model which is simply the single operational amplifier version of the quad operational amplifier IC package known as LM324.

As briefly mentioned previously, the design utilizes the resistor Rs to act as the resistor that has a controlled potential on either side of it to dictate the amount of current flowing into or out of the integrator. The side of Rs not connected to the operational amplifier is connected to the LM336 voltage reference diode. Also connected to this node is either a positive or negative 15 V provided by the power supply circuit via a 3.6 kΩ resistor. This reference voltage can then be adjusted by the LM336 voltage reference diode with its associated 10 kΩ potentiometer R12 to set a stable +/- 2.5 volt reference

With this voltage set, the other side of the resistor Rs must be inspected in order to set the current that will flow through it. This voltage is set through the inverting pin of the LM324 amplifier. This voltage is identical to the voltage applied at the non-inverting pin of the LM324 as dictated by the electrical characteristics of an ideal operational amplifier. There are two ways that the researcher can apply a control voltage to the non-inverting pin. The first method involves using the potentiometer R13 set in parallel to the 2.5 V reference diode. By adjusting R13 the user can set a voltage slightly varied from 2.5 V, thus creating a small potential difference across R_S and initiating a current flow. Alternatively, this control voltage can be controlled by a data acquisition system (DAQ) via an SMA cable connection.

Moving onto the MOSFET component, the gate of the transistor is connected to the output pin of the amplifier while the inverting pin of the amplifier is connected to either the source pin of the N-channel transistor or the drain pin of the P-channel transistor. These two connections constitute the feedback loop of the system and enable the

amplifier to adjust its output to keep the voltage potentials accurate. Finally, the drain/source is connected to the same node as the photodiode and integrator to provide a path for the current through Rs to flow.

Crucially, the combination of all these design elements provides the researcher with the means to control the slope of the integration before reaching its maximum charge capacity. This can be a useful feature as the feedback circuit can be setup to allow the integrator to reach its peak just before the integration cycle resets the accumulated charge. Figures 2.17 and 2.18 depict these ideal output integration waveforms.

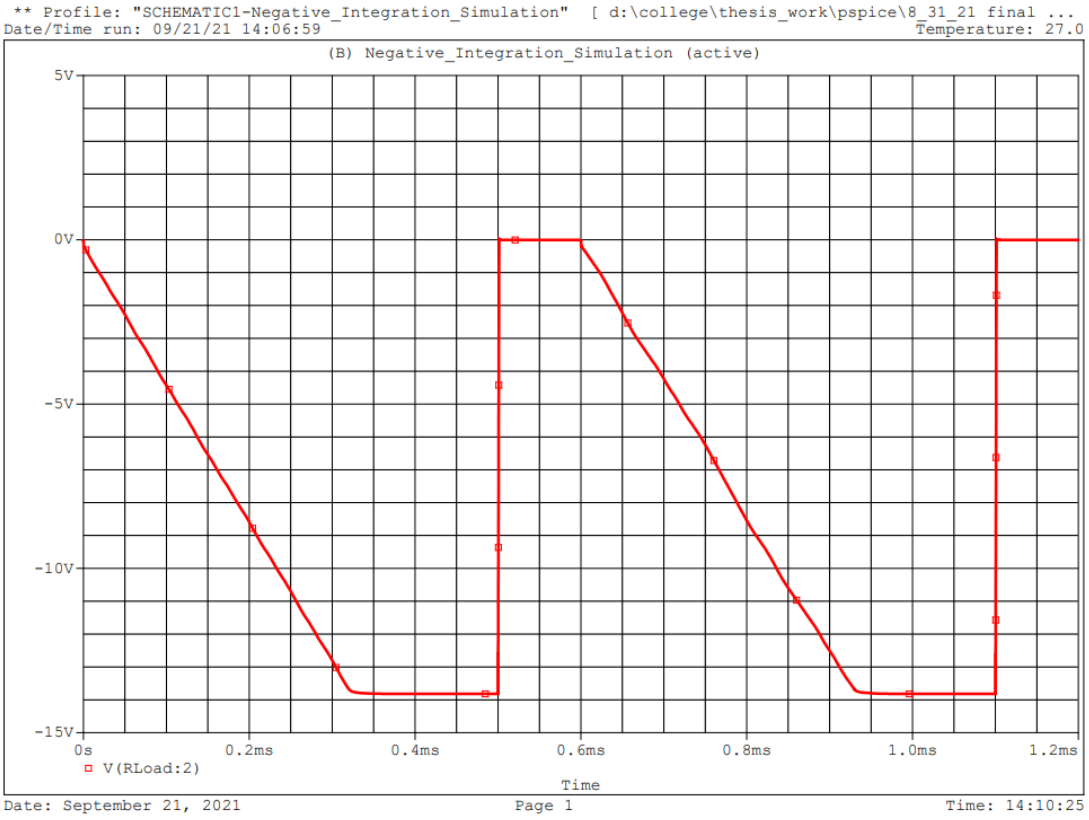


Figure 2.17: Negative integration mode output waveform plot

These models also served a useful purpose in estimating what the approximate current draw the overall design would utilize. By running a transient simulation on the

circuit, PSpice automatically runs a bias point analysis to meet this end. As stated by Fitzpatrick, “In PSpice, the bias point analysis calculates the node voltages and currents through the devices in the circuit” [14]. By observing the currents leaving the +/- 15 V DC power supply block, the overall circuit design can be predicted to require that amount of current to operate properly. As such in these designs, the current draw for the positive integration circuit was 17.74 mA and for the negative integration circuit the current draw was also 17.74 mA.

There is important clarification to make when discussing the power supply used in these simulations. Preferably, using the actual IC that will later be incorporated into the final design would give a more accurate reading with regards to the power consumption

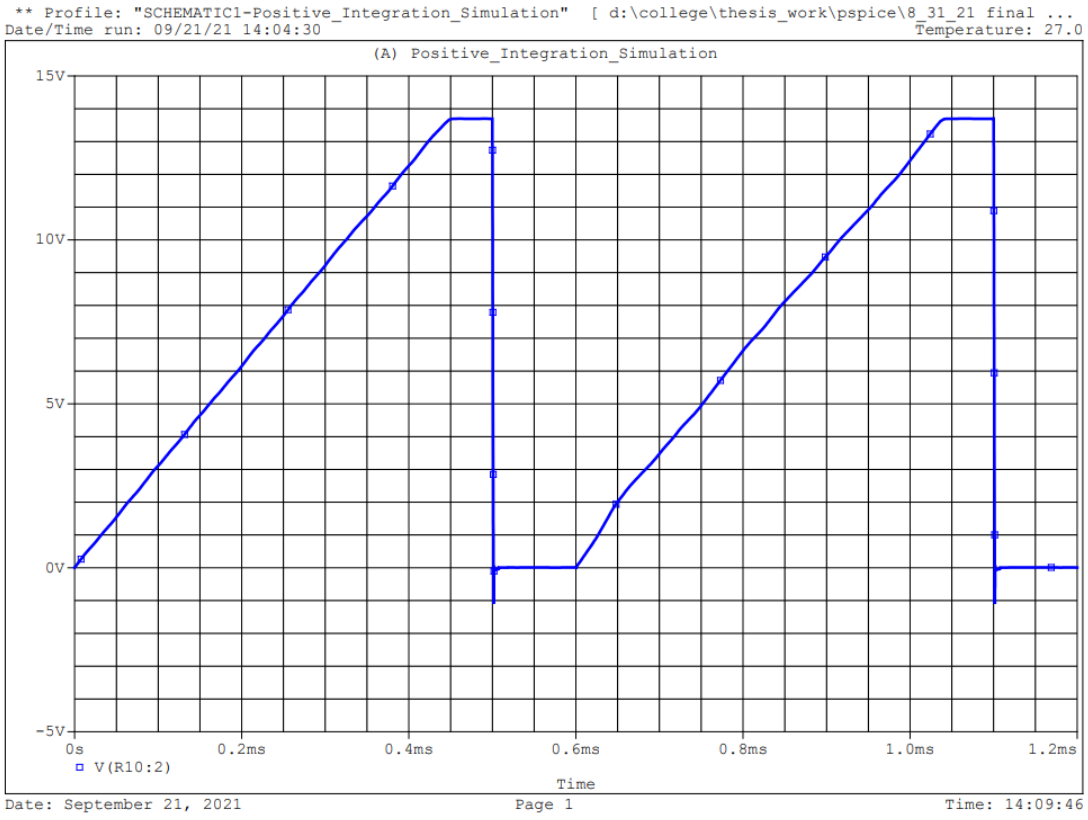


Figure 2.18: Positive integration mode output waveform plot

of the overall circuit. However, this version of OrCAD Capture did not include in its libraries the TPS65130RGET DC-DC converter chip which was selected for this project. Other software packages such as PSpice for TI were also investigated for the availability of this product but still did not yield a model for it. Therefore, it was decided that the power supply would only be composed of two DC voltage sources and a ground for the simulation aspect of the project.

Overall, the PSpice simulation models depicted in this section were instrumental in determining the design which would work best for this project's application. The simulations also helped bolster the idea that once fully assembled physically, these circuit designs would work as intended. In addition to this, they also helped identify an estimate to the design's power consumption which is a critical factor given that the design is powered through a battery.

Chapter 3: Assembly and Testing

3.1 PCB Design

With the initial design considerations accounted for, the actual PCB designing stage of the project can be discussed. For this project, the PCB design software used was EasyEDA as that was the most familiar software platform for the author. Considering that this device is meant to be wearable, there are a number of factors to consider in its design including but not limited to power supply chip implementation and component placement. Specifically for this project, the PCB also needs to implement a unique design which allows for the user to choose which integration mode they would like to utilize or to provide a voltage potential via an SMA connection if desired.

Possibly the most important aspect of the overall PCB design lies with the power supply chip implementation. This project makes use of the TPS65130RGET DC-DC converter by Texas Instruments. The chip is housed in a space conservative QFN package which is only 4 mm in length and width [15], thus making this chip ideal for a wearable technology application. This supply chip was selected for a host of additional reasons including its switching frequency, power efficiency, and ability to be powered by a compact battery cell.

The switching frequency of this chip can vary from a minimum of 1250 kHz to a maximum of 1500 kHz. The typical frequency of the converter lies at approximately 1380 kHz [15]. Compared to the switching frequencies discussed in section 2.1.2, this range of frequencies is acceptable for the final design. This effort to match the switching

frequencies ideally decreases the overall construction size of the PCB at a small cost to the efficiency of the regulator.

With regards to power efficiency, this IC also boasts many unique advantages. The chip accommodates the user with a power-save mode which allows for the efficiency of the regulator to increase for low current applications [15]. Figure 3.1 can be used as a reference to observe this design consideration. Notably, the PCB design utilizes a positive voltage of 15 V rather than 12 V, but this chart depicts a relatively consistent trend for both setups.

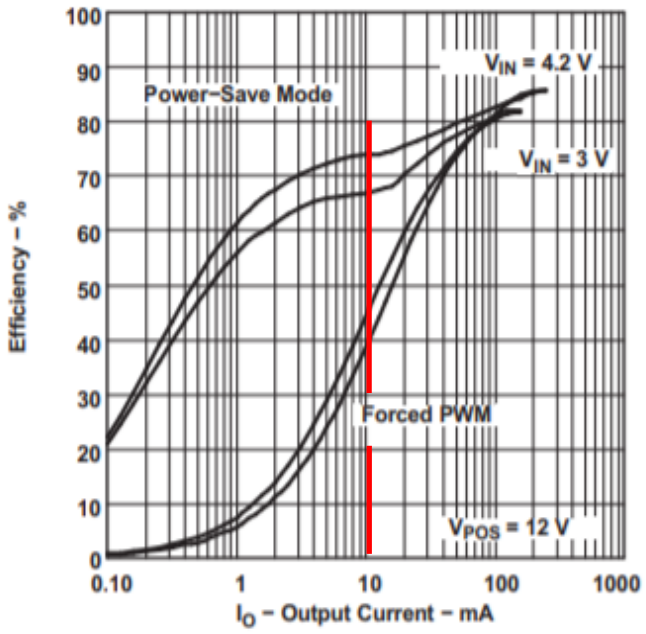


Figure 3.1: TPS65130 Efficiency vs. Output Current with red vertical line indicating estimated output current. Reprinted from “TPS6513x Positive and Negative Output DC-DC Converter” by Texas Instruments, retrieved: https://www.ti.com/lit/ds/symlink/tps65130.pdf?ts=1635189017122 Reprinted with permission. [15]

Based on the PSpice simulation estimate of 17.74 mA current draw, one can follow the red vertical line at to see the drastic difference in efficiency the power saving mode can provide. At 17.74 mA the forced pulse width modulation (PWM) mode rests at an

efficiency of about 50% to 54% depending on the input voltage. In contrast though, the same chip with the power-save mode enabled can attain even higher efficiencies ranging from 68% to 74%. This dramatic upgrade in efficiency of the regulator has positive effects on the battery life of the wearable device and ensure longer usage times before charging is required.

Another significant factor which led to this voltage regulator to act as a power supply was its input voltage range. The preferred input terminal voltage, as recommended by the product datasheet, lies in a range from 2.7 V to 4.2 V [15]. Furthermore, Texas Instruments intended for this chip to be powered by a single-cell lithium-ion battery. This makes the TPS65130RGET an even more attractive option for this project, as it was by design intended for battery operated systems such as those found in wearable technologies.

Moving on from the voltage regulator, the rest of the PCB design incorporated many specific advantages pertaining to this project scope. One such advantage is a design which allows for flexibility of testing the circuit in multiple configurations. These multiple configurations can be identified as the unconnected pins in the overall circuit schematic in Figure 3.2. Another beneficial design perk is easy access to the required SMA cable connections while maintaining a relatively small PCB board design. Both of these qualities can be linked back to smart placement of on-board components.

To create a design which can incorporate a multi-configuration PCB layout, a standard must be used to keep consistency throughout the board. For any connections which required modification beyond the PCB fabrication process, 0.5 mm by 0.5 mm

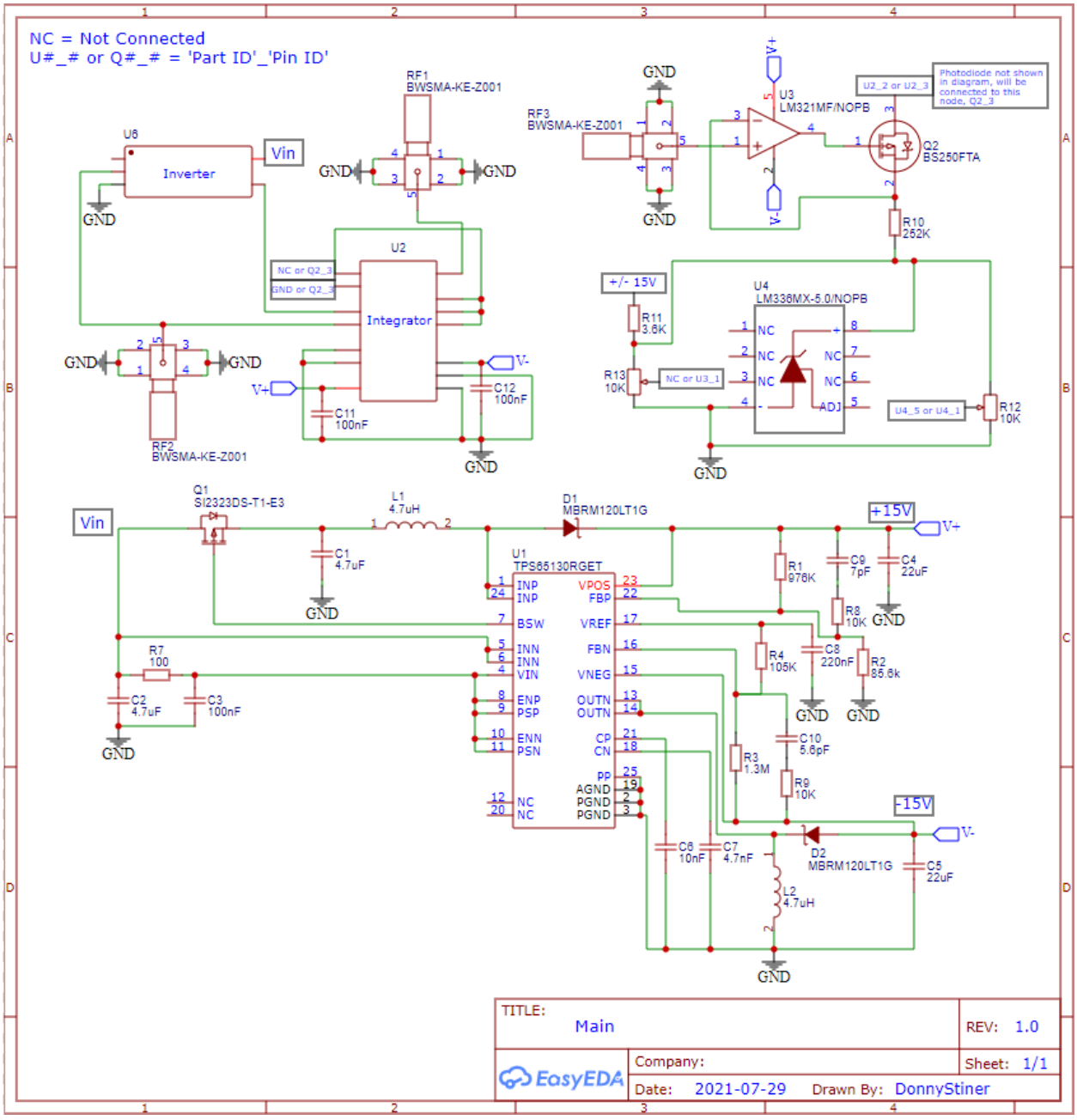


Figure 3.2: Snapshot of final circuit design in EasyEDA

contact pads were placed to allow for hand soldered connections between pads. For further clarification on this, Figure 3.3 can be used as a reference. In this way, each PCB

has the potential to integrate in either the positive or negative integration modes with a few pieces of well-placed solder.

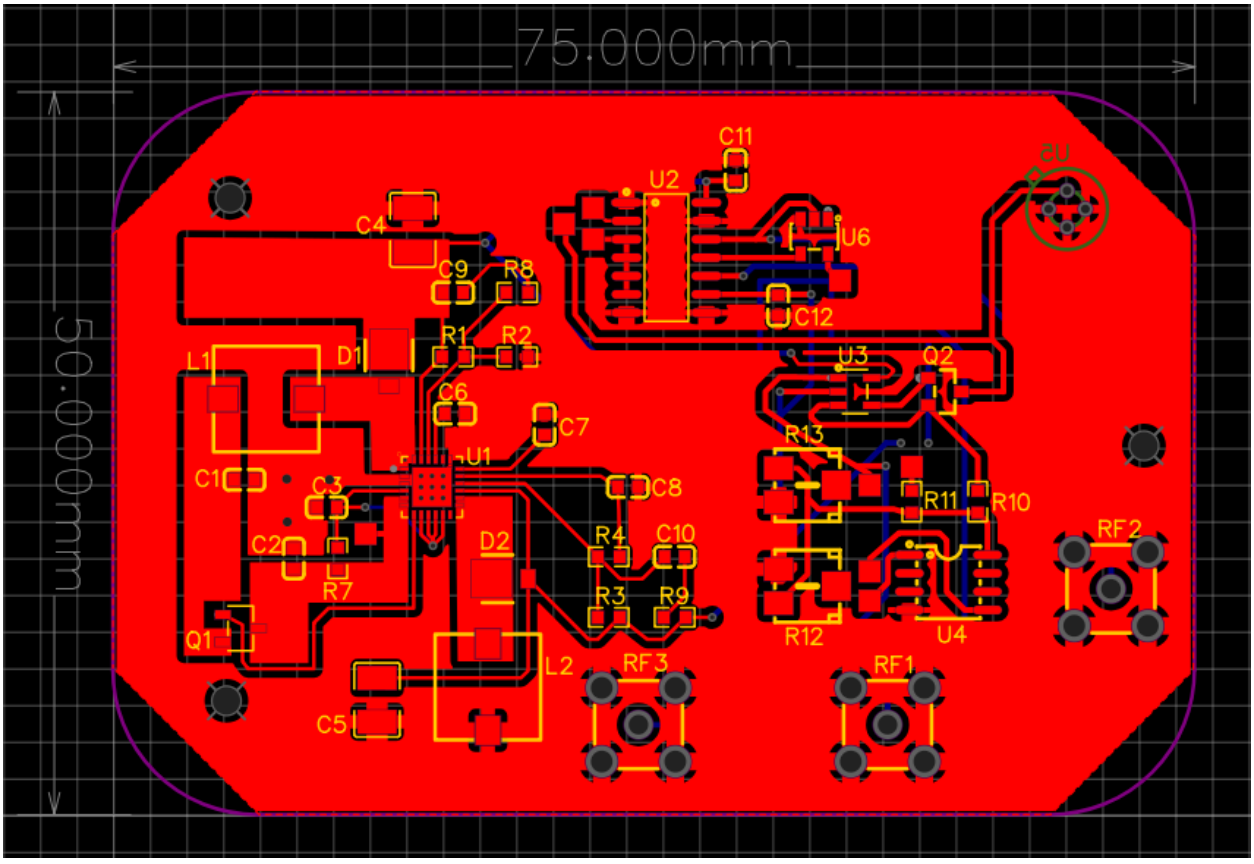


Figure 3.3: Snapshot of final PCB design layout in EasyEDA

The SMA connections on the board are crucial to the project's scope of work as they are needed to communicate with the analysis software located separately from the PCB. To make sure these SMA connections were easily accessible, the footprints for these components were placed towards the outer edges of the PCB. These connectors in particular also need clearance above them as they are not to be connected parallel to the board but rather vertically. Thus, care must be taken to ensure that a prototype casing design does not interfere with accessibility to these critical connections

An additional design consideration worth noting is the physical location of the components on this PCB design. All components, save for the photodiode and a few copper traces, are located on one side of the board. This is to ensure that the photodiode can be placed firmly and safely on the skin of the subject to allow for accurate readings and thus producing useful results at the output of the system. Furthermore, to safeguard the subject from the potential of an electric shock, a 3D printed case was designed to cradle the PCB within it and provide a layer of insulation between the PCB and the subject's skin. The 3D printed case was constructed using PLA as it is an inexpensive material and allows for and potential revisions to be incorporated and printed with ease [16].

Attention should also be drawn to the small black circles depicted inside the "U1" footprint outline. These small symbols represent 0.3mm diameter vias which lie underneath the QFN packaged TPS65130RGET converter. These PCB vias directly enhance the heat transfer from the converter package and increase the overall thermal conductivity of the design [17]. This increase in thermal conductivity can decrease IC temperatures during operation and allow for extended running times, which is a critical factor in this analysis application.

3.2 PCB Assembly Techniques

In order to effectively assemble the PCB, a host of tools and equipment is required to complete this process. To begin, the assembly utilizes a soldering iron and hot air rework station, rosin core solder, a wet or bronze sponge, a syringe of solder paste, a syringe of no clean flux, and a multimeter. One tool that is optional but exceptionally useful for assembly is a pair of solder helping hands. These instruments can help the assembler

in positioning the PCB at the correct orientation to allow for a clean soldering connection. The role of the multimeter in this assembly grants the fabricator the ability to verify that all connections are properly connected via a continuity check. All the equipment applied to this assembly procedure can be seen in Figure 3.4.

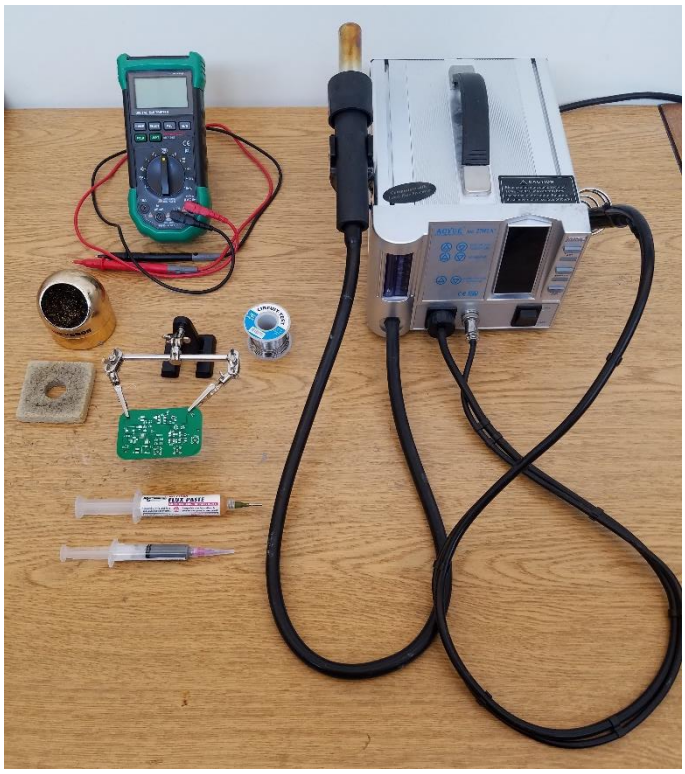


Figure 3.4: Image depicting equipment utilized in assembly procedure

The PCB design was intended for most components to be soldered by hand using a standard soldering iron. One must take care when pursuing this avenue of fabrication however, as the design of the PCB plays a crucial role in how simple the procedure is. Bulky copper areas, such as the ground plane found in this design, can very effectively dissipate heat away from any connection pad you may be attempting to solder. This can lead to a number of soldering problems including dry joints [18]. Therefore, one must

compensate for this increased heat dissipation by setting the soldering gun temperature approximately 20° to 30°C above the melting point of the solder in use.

One component which cannot be hand soldered to the PCB is theTPS65130RGET DC-DC converter IC. This chip has a QFN package which utilizes 24 single pin contact pads and a larger ground power pad on the underside of the chip. Seeing as how these connection points are on the bottom of the package, a conventional soldering iron cannot be used to ensure a reliable connection. Therefore, for these connections, the most effective method to be employed is a solder paste heated up with a hot air reflow tool. To properly perform this method, one must first analyze the solder paste to be utilized in this procedure. The solder paste used is an industry standard type 4 with a 63Sn and 37Pb alloy composition. Crucially, it must be noted that the standard melting point temperature for this specific alloy composition is 183°C [19]. This temperature is an important detail in the reflow soldering process, which involves slowly raising the temperature of the PCB to effectively heat up, reflow, and then harden the solder paste per its explicit thermal characteristics [20]. An important resource to use when characterizing these temperatures is a solder paste's reflow profile. This graph depicts the relationship between the varying stages the solder undergoes over time as it corresponds to the temperature it is being exposed to. Figure 3.5 depicts the reflow profile of a 63Sn/37Pb solder, just as is used in this project [21]. As can be seen in the figure, the time window for reflow is relatively small as temperatures exceeding the reflow region of the chart can cause damage to the solder paste or PCB if left on for an extended period of time.

After a small amount of solder paste is applied to all the contact pads of the QFN package, the TPS65130RGET is located as closely as possible to the outline of the PCB silk screen of the component. Once this chip has been properly oriented, the hot air reflow applicator is slowly lowered towards the IC in order to gently ramp the temperature of the solder paste until the point of melting, thus entering the reflow stage. As the solder paste enters a molten state, the solder distributes itself across the contact pads of the PCB. After remaining in this state for approximately 15 seconds, the hot air reflow pencil is then slowly distanced from the IC to allow the solder to solidify and form a solid connection between the contact pad and the chip pins.

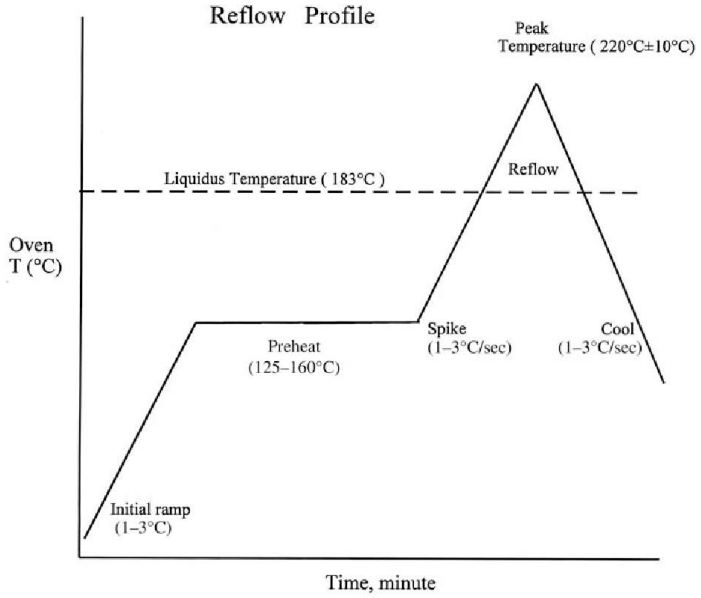


Figure 3.5: Reflow profile of 63Sn/37Pb solder paste. Reprinted from “Power Electronic Modules: Design and Manufacture” by W. Sheng & R. Colino Reprinted with permission. [21]

One common issue that can occur after this procedure is known as a solder bridge, which has been referred to as a “major soldering defect in the reflow process” by Zhang [22]. This issue can be remedied by a useful technique which only requires the use of a

soldering iron and flux applied at the solder joint. By taking a soldering iron with a fine tip which has been tinned with a small amount of solder, one can simply drag the iron across the pins and break any existing bridges that may have formed during the reflow process [23].

3.3 PCB Testing Setup

Once the PCB assembly was complete, the next step was to investigate whether the power supply design works as intended. The first thing to examine is the voltage outputs from the voltage regulator IC. For the second phase of testing, it must be verified that the integrator chip is performing within expected parameters. By confirming the operation of these two aspects of the power supply design, this simultaneously guarantees the ability of the power supply to provide the signals required for the SPG process.

For the first portion of my testing procedure, the proper potentials needed to be identified at their respective nodes on the circuit. To do this, the benchtop power supply would be powered up and then the multi-meter probes set to record potential could be applied to the nodes of interest. The points of circuit which require an external power connection are the Vin and analog ground pins of the voltage regulator and the Vin pin on the inverter chip. For testing purposes, these connections are made by some jumper cables soldered into place.

The next part of testing involves identifying if the circuit properly incorporates the integration chip with the current limiting feedback circuit. In order to do this, an external GUI using the SMA connectors provides the paths for the inputs and outputs of the circuit. The connector identified as RF1 provides the integrator chip with the digital input signal

needed to reset the integration for each 50 ms cycle. Circuit component RF2 is utilized to output the final integration signal which is later needed in the SPG watch signal analysis. Finally, RF3 is essential to control the voltage held at the inverting side of the LM321 operational amplifier.

Once the proper SMA connections have been made, one must then analyze how the circuit is powered. Based on what the TPS65130RGET datasheet recommends as an input power source, this project utilizes a Samsung 3.7 V 800 mAh lithium-ion battery. The batteries three pins are distributed to the circuit through the series connection of a right angle 3-pinned connector and the previously mentioned jumper wires utilized when testing the circuit with the benchtop power supply.

In an effort to stress test the overall final design as well, the negative integration configuration PCB was turned on continuously until the battery became fully discharged in order to identify the actual estimated battery life of the prototype. During this discharging period, the device will be periodically inspected with a multimeter to ensure that the 30V output range is maintained throughout the test. Additionally, both configurations will be tested for variance over a span of at least 10 minutes to ensure that the output signal from the circuit remains desirable. This variance test will also be performed using two separate integration, reset, and sampling times. The high frequency test utilized a 200 ms integration time, a 10 ms reset time, and a 10 ms sampling time. The low frequency test utilized a 500 ms integration time, a 100 ms reset time, and a 50 ms sampling time. These tests guaranteed the stability of the output signal over a typical period of time needed to analyze the SPG output waveform.

3.4 PCB Testing Results

With regards to the verification of the crucial voltages found throughout the circuit, Table 3.1 depicts the voltages recorded for both the positive integration and negative integration circuit designs. As one can summarize from this table, the TPS65130RGET voltage regulator operates almost exactly as designed. With an input of 3.7 V, the total output voltage range of both configurations is approximately 30V which is utilized to power the integrator IC and LM321 operational amplifier. It is also worth noting that during this testing, the current draw recorded on the power supply for both integration schemes were approximately 56 mA as opposed to the 17.74 mA estimated by the PSpice simulation. This is the current measured from the battery terminals however, not the output of the voltage regulator which is where the PSpice simulation estimated current was obtained from. Therefore, the 56 mA reading can be used to estimate the battery life of the design. With an 800 mAh battery as a source, the battery life span is approximately 14 hours, which is still quite impressive given that the wearable device will likely be charged on a daily basis.

After stress testing the design however, we were able to confirm if the hypothesis of a 14 hour battery life was accurate or not. It was discovered that while the output of the voltage regulator did indeed maintain the 30 V output range the entire time the battery was providing charge, it only lasted about 8.5 hours as opposed to the 14 hour prediction. The output battery voltage was recorded at 2.9 V moments before the voltage regulators failed to output any voltage whatsoever. Given that the battery's stable output voltage is 3.7 V at full charge, this recorded 2.9 V was likely the minimum voltage the battery could maintain before fully discharging and providing 0 V at the output battery pins. It should be

noted that only the negative integration circuit was tested but given that the positive integration circuit also consumed nearly the exact same amount of current, it should yield a similar battery life to that of the negative integration circuit. This reduced time of battery life can likely be attributed to the voltage regulator efficiency or the battery itself, as it may not be able to effectively hold a charge for the full 800 mAh due to excessive use in the past.

Table 3.1 Summary of PCB Testing Results

Circuit Integration Type	TPS65130RGET Positive Output Voltage	TPS65130RGET Negative Output Voltage	LM336 Output Voltage
Positive	15.04 V	-14.97 V	2.501 V
Negative	15.02 V	-14.99 V	-2.496 V

Moving onto the results obtained from testing the integrator, it is important to note that the current fed into the integrator to test its operation was provided via the current limiting feedback circuit. The output integrator circuit signal is the crucial factor in properly analyzing an SPG waveform for this device. Additionally, the current limiting circuit provides the user with the flexibility to control the amount of current entering or leaving the integrator IC. Therefore, verifying the proper operation of this integrator IC and the current adjusting circuit proves that the power supply design circuit would also be compatible fully incorporated into the SPG analysis hardware.

Following that clarification, one can then look at Figures 3.6 and 3.7 to observe the final output waveforms produced by the design's integrator chip. Figure 3.6 depicts the positive integration output waveform while Figure 3.7 shows us the negative integration output waveform. These results are operating as expected and both have voltages set through RF3 to reset the integration just before saturation. If the user desired to adjust the RF3 input voltage, this would in turn then alter the slope of the integration causing it to either saturate before resetting or reset the integration well before saturation is reached.

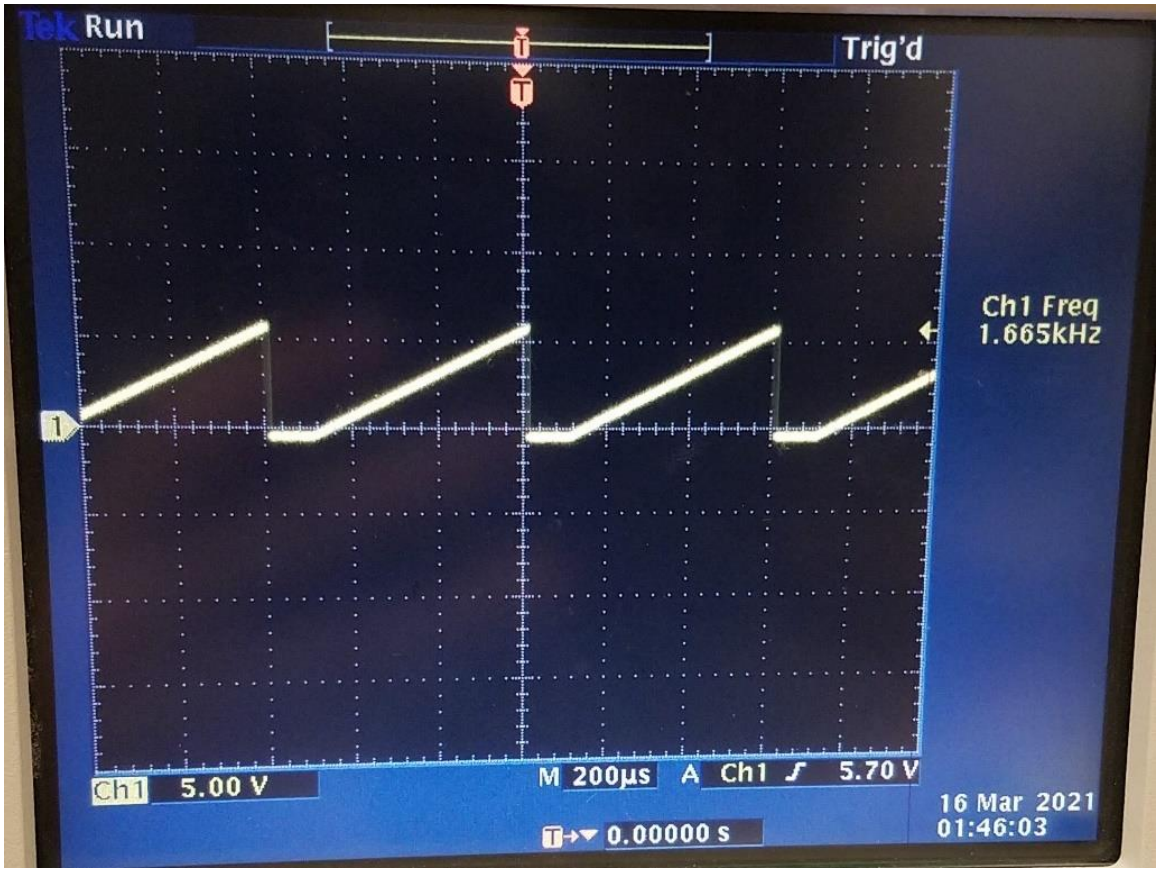


Figure 3.6: Positive integration PCB output waveform

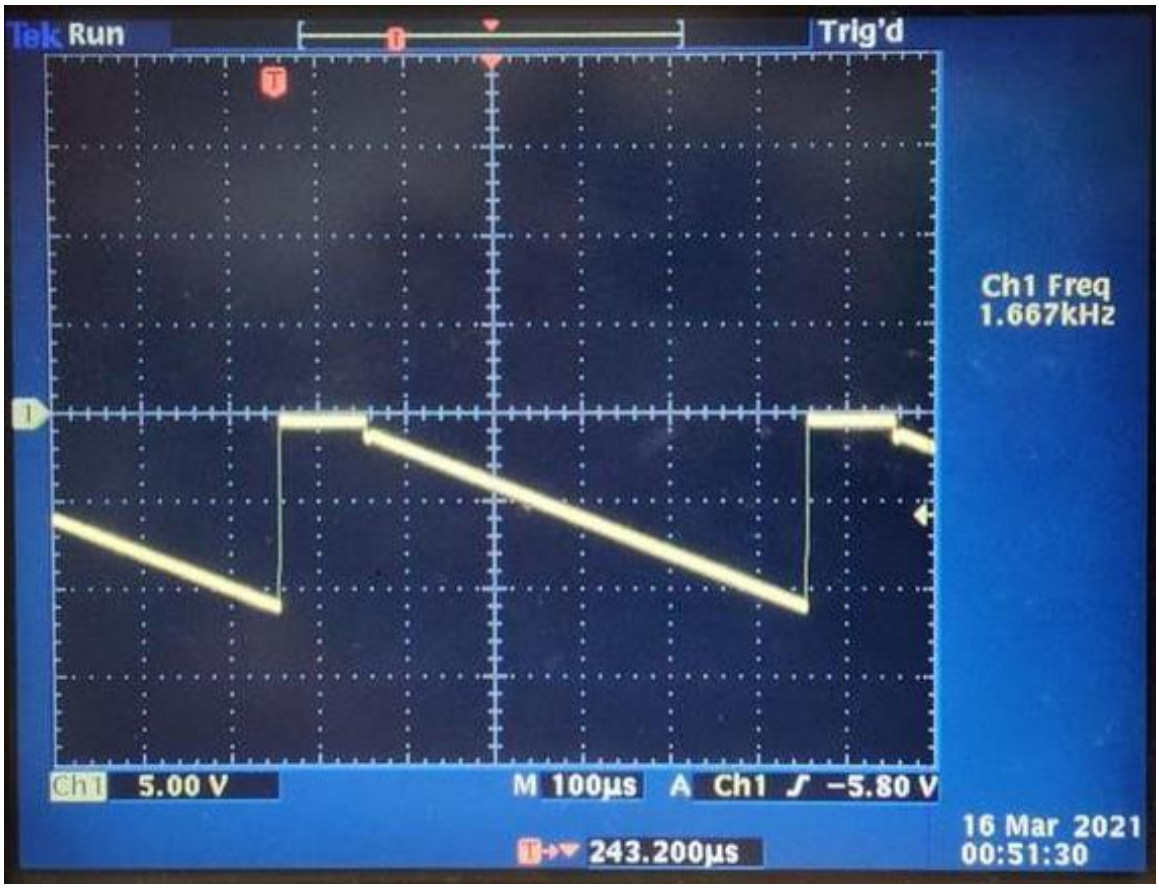


Figure 3.7: Negative integration PCB output waveform

The results produced were essentially noiseless which can likely be attributed to the design considerations implemented into the specific integrator IC such as grounding non-connected pins. Guarding the input pins with the circuit analog ground also likely contributed to the noiseless output signal. Another factor to consider in obtaining these desired output waveforms is the resistors R8 and R9 placed in series with the feedforward capacitors C9 and C10. These resistors help with coupling noise from the DC-DC converter and help give us a lower noise output from the voltage regulator.

It is also critical to note that the two integration schemes essentially produce the same waveform flipped over the x-axis of the oscilloscope. With this being said, the user can utilize either the negative or positive integration waveforms to perform an SPG signal

analysis. In this instance, the preferred integration scheme by the tester was the negative integration waveform as it produced the least amount of variance as observed in the external GUI controlling certain aspects of the circuit. The lower the amount of variance in the output integration waveform, the more reliable the results will become after performing a full SPG signal analysis.

Summarizing the results from the variance tests at both the high and low frequency settings, it was discovered that as the frequency of integration and reset increased, so did the variance of the output signal. This means that the frequency with the 200 ms integration time, 10 ms reset time, and the 10 ms sampling time produced the least desirable output signals. It's also worth mentioning that again, the variance for both the positive and negative integration schemes did not change over the ten minute testing time period, thus proving the device could indeed output consistent results for a testing period for SPG analysis.

Chapter 4: Conclusion and Future Considerations

4.1 Conclusion

The objective of this research investigation was to develop a wearable, space efficient PCB design powered by a battery source which incorporated the power supply converter as well as the SPG analysis IC's. Through the development of this project, the power efficiency and compact dimensioning of the final power supply design were prioritized over most other factors. Unique design considerations were also implemented which gave this power supply design an advantage in terms of its relatively noise free output signals and gave the final device longer battery life overall.

Critically, the final selection of the DC-DC converter chip allows the designer to utilize a single cell lithium-ion battery to power the IC This chip boasts an efficiency of 68% to 74% by taking advantage of the power saving feature incorporated into its design. This power saving mode reduces the overall power consumption of the circuit and improves the battery life of the design. Both of these features are critical to obtaining an effective final product when designing a wearable device.

With this final design, it can be shown that the proper output voltages needed to power the various on-board chips for the design have been met. The positive and negative 15 V biases are used to power both the integrator chip as well as the LM321 operational amplifier. Then, the LM336 is supplied a voltage of either positive or negative 15 V and converts that voltage to bias the current controlling resistor in such a way to properly setup the current limiting feedback circuit for use.

From the stress testing of the device, it was discovered that the approximate battery life of both circuit configurations is 8.5 hours before the voltage regulator no longer creates the 30 V potential bias for the circuit. Additionally, the negative integration configuration produced less variance at the output than the positive integration configuration. This could also be seen through the ten minute testing period for the differing frequencies, which depicted a system that could reliably produce stable output signals over this time period.

Perhaps most importantly, the final design also correctly incorporates the relationship found between the current limiting circuit and the integrator chip. This gives the experimenter flexibility in adjusting the current leaving or entering integrator and compensate for any current generated or sunk by the photodiode. With the ability to control this current flow, the final integration curve slope and reset time can be optimized to give a future SPG watch analysis the most effective output integration waveform for the application.

4.2 Future Considerations

Wearable technologies are in a booming industry providing many attractive options for the average consumer. However, there remains many design hurdles which must be overcome to provide the person wearing the technology all the advantages it has to offer. This thesis attempts to address these more critical issues such as the issue of power consumption but there are further still improvements which could be made to this design which will prolong battery life and increase time periods between charges. This section attempts to highlight the more significant enhancements that will give the technology the edge it would need to perform well in today's modern industry.

For this specific project, there are additional measures one must verify before fully incorporating the power supply design into a wearable device utilizing SPG waveforms. One such step is to determine that the noise levels at the output of the integrator are sufficiently low enough to not interfere with desired waveform readings. An additional aspect which needs to be developed and implemented is the laser and photodiode probe which will be used to more effectively quantify the amount of light reflected off the skin of the participant. This probe must be designed to allow for reflected light to be measured in a standardized manner. This will allow for an accurate recording of SPG waveforms between trials.

One potential improvement upon this design would be a mechanism to disable the circuit when not in use. Currently, the circuit is drawing a small amount of current to operate once the battery is connected. By introducing a method which allows the user to suspend this current flow, one could theoretically prolong the battery life of this device. Long battery life for wearables is a crucial factor when creating a practical design that can be used by the consumer on a day to day basis.

At its current state, the device overall is larger than most typical wearable devices found today, such as smart watches. Therefore, in an effort to shrink down the device size, the PCB dimensions need to be reduced. One reason for the increased PCB size was overcompensating for the size of the ground plane needed to dissipate heat. Given the devices low current draw, the ground plane size could be decreased therefore saving a significant portion of the space utilized on the PCB currently.

Another way in which the PCB dimensions could be reduced would be to determine the optimal integration scheme and only implement that component configuration into

future PCB builds. This would save space on the board as the leftover contact pads used to provide the fabricators with the flexibility of integration modes could then be removed from the design. With this extra space, crucial components which need to remain in the final design could be spaced closer together without the concern for solder joint connections which normally require extra space between contacts.

An additional facet worth exploring for this design would be to develop the on-board circuitry on a flexible PCB. A flexible circuit board such as this would allow for a more space efficient and form fitting design if for instance the measurement was being taken on the forearm. Rigid circuit boards can cause an issue with readings obtained from the photodiode and laser probe. If the circuit board were flexible however, this would allow for the measurement probe to be more effectively integrated as one could make more consistent contact with the skin of the participant.

References

[1] Y. Liao et al., “The Future of Wearable Technologies and Remote Monitoring in Health Care”, American Society of Clinical Oncology Educational Book, Vol 39, 2019

[2] “Wearable Technology 2017-2027: Markets, Players, Forecasts”. IDTechEx. https://www.idtechex.com/en/research-report/wearable-technology-2017-2027-markets-players-forecasts/536

[3] A. Ometov et al., “A Survey on Wearable Technology: History, State-of-the-Art and Current Challenges”, Computer Networks, Vol. 193, 2021.

[4] Y. Liu et al., “A wearable real-time power supply with a Mg_3Bi_2-based thermoelectric module”, Cell Reports Physical Science, Vol. 2, No. 5, 2021.

[5] S. Schnier et al., “Power Management Reference Design for a wearable Device with Wireless Charging Using the bq51300 and bq25120”, Texas Instruments, Application Report, Apr. 2016

[6] M. Ghijsen et al., “Wearable speckle plethysmography (SPG) for characterizing microvascular flow and resistance”, Biomedical Optics Express, Vol. 9, No. 8, 2018.

[7] C. Dunn et al., “Speckleplethysmographic (SPG) Estimation of Heart Rate Variability During an Orthostatic Challenge”, Scientific Reports, Vol. 9, 2019.

[8] A. Biswas & A. Parthasarathy, "Fast Diffuse Correlation Spectroscopy with a low-cost, fiberless embedded diode laser", Biophotonics Congress: Biomedical Optics 2020.

[9] J. Zhu et al., “Study on the Harmonics of Switching Power Supply”, Procedia Engineering, Vol. 29, pp. 2098-2102, 2012.

[10] J. Bird (2006). Higher Engineering Mathematics, Fifth Edition. Elsevier. p. 683

[11] “Considerations on Switching Frequencies.” (2015). Tech Web. https://techweb.rohm.com/knowledge/dcdc/s-dcdc/02-s-dcdc/101

[12] D. Hubbard, “Reducing noise on the output of a switching regulator”, Analog Design Journal, 2018.

[13] D. Terrell (1996). Op Amps (Second Edition). Elsevier Science. p. 19

[14] D. Fitzpatrick (2012). Analog Design and Simulation using OrCAD Capture and PSpice. Elsevier. p. 23.

[15] Texas Instruments, “Positive and Negative Output DC-DC Converter,” TPS6513x datasheet, Mar. 2004 [Revised Jan. 2016].

[16] A. Dey et al., “A Review on Filament Materials for Fused Filament Fabrication”, Journal of Manufacturing and Materials Processing, Vol. 5, No. 69, 2021.

[17] K. Hollstein et al., “Thermal analysis of the design parameters of a QFN package soldered on a PCB using a simulation approach”, Microelectronics Reliability, Vol. 120, 2021.

[18] D. Jones, “PCB Design Tutorial,” AlternateZone.com, June 29, 2004. [Online] Available: http://alternatezone.com/electronics/files/PCBDesignTutorialRevA.pdf. [Accessed Sept. 29, 2021].

[19] “Reflow soldering profiles” (2018). Compu Phase. https://www.compuphase.com/electronics/reflowsolderprofiles.htm

[20] E. Brunvand, “Using Surface-Mount Components in an Embedded Systems Lab”, University of Utah, 2015.

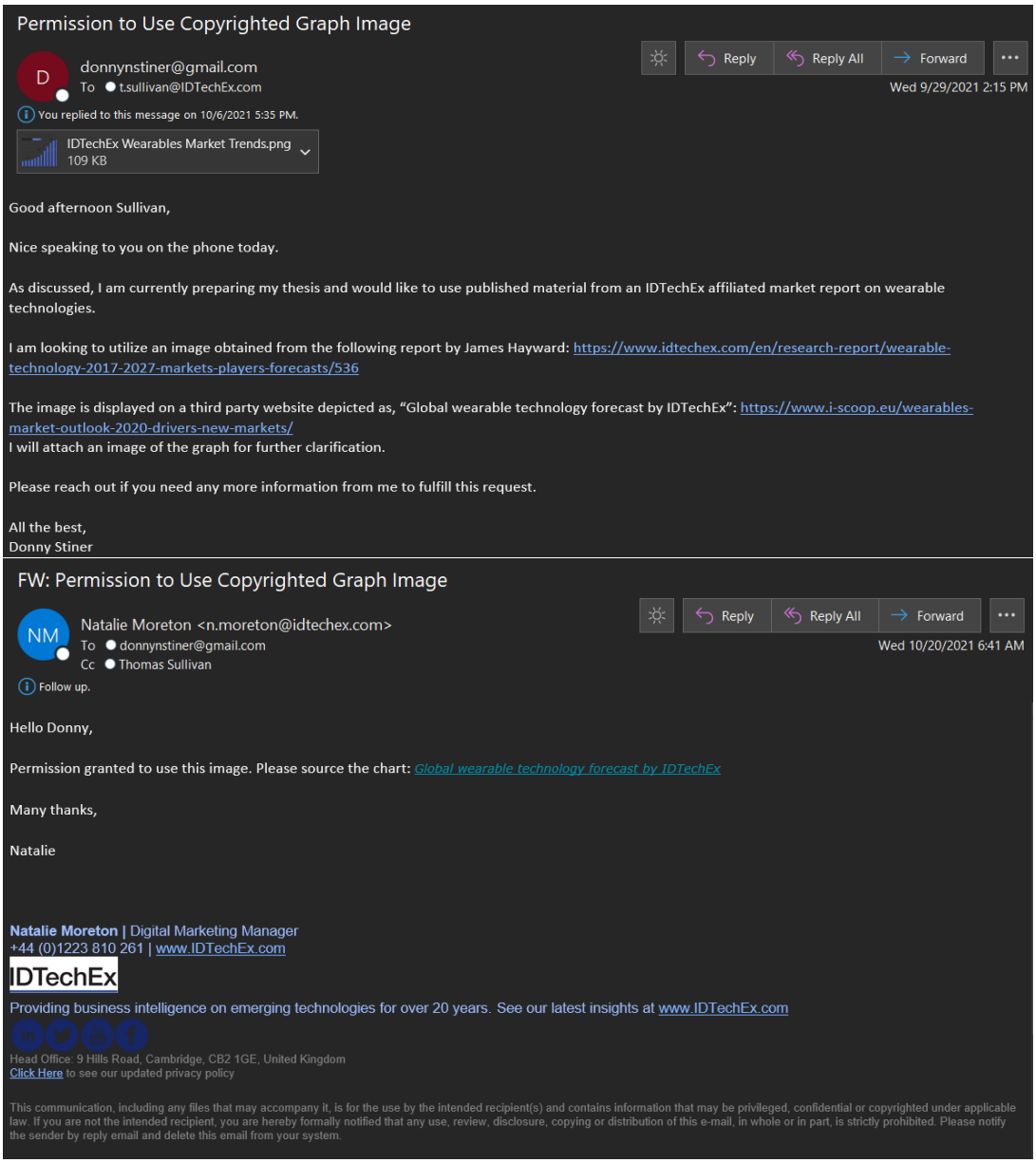
[21] W. Sheng & R. Colino, (2004). Power Electronic Modules: Design and Manufacture, First Edition. Taylor & Francis Group.

[22] L. Zhang et al., “Avoid Solder Bridging: Dewetting of SnAgCu Solder liquid on Non-Wetting Zone”, IEEE ICEPT2006 Proceeding: 8th International Conference on Electronics Packaging Technology, pp. 400-404, 2006.

[23] “How to Solder a QFN Component Using a Hot Air Rework Station” Digi-Key. https://www.digikey.be/de/maker/projects/how-to-solder-a-qfn-component-using-a-hot-air-rework-station/77b9331e7183452f97041c75d946c7c7

Appendix A: Copyright Permissions

The permission below is for the use of Figure 1.1. The hyperlink in the forwarded email response is as follows: https://www.idtechex.com/en/research-report/wearable-technology-2017-2027-markets-players-forecasts/536.



Permission to Use Copyrighted Graph Image

D donnynstiner@gmail.com
To t.sullivan@IDTechEx.com

Reply | Reply All | Forward | ...
Wed 9/29/2021 2:15 PM

You replied to this message on 10/6/2021 5:35 PM.

IDTechEx Wearables Market Trends.png
109 KB

Good afternoon Sullivan,

Nice speaking to you on the phone today.

As discussed, I am currently preparing my thesis and would like to use published material from an IDTechEx affiliated market report on wearable technologies.

I am looking to utilize an image obtained from the following report by James Hayward: https://www.idtechex.com/en/research-report/wearable-technology-2017-2027-markets-players-forecasts/536

The image is displayed on a third party website depicted as, "Global wearable technology forecast by IDTechEx": https://www.i-scoop.eu/wearables-market-outlook-2020-drivers-new-markets/
I will attach an image of the graph for further clarification.

Please reach out if you need any more information from me to fulfill this request.

All the best,
Donny Stiner

FW: Permission to Use Copyrighted Graph Image

NM Natalie Moreton <n.moreton@idtechex.com>
To donnynstiner@gmail.com
Cc Thomas Sullivan

Reply | Reply All | Forward | ...
Wed 10/20/2021 6:41 AM

Follow up.

Hello Donny,

Permission granted to use this image. Please source the chart: *Global wearable technology forecast by IDTechEx*

Many thanks,

Natalie

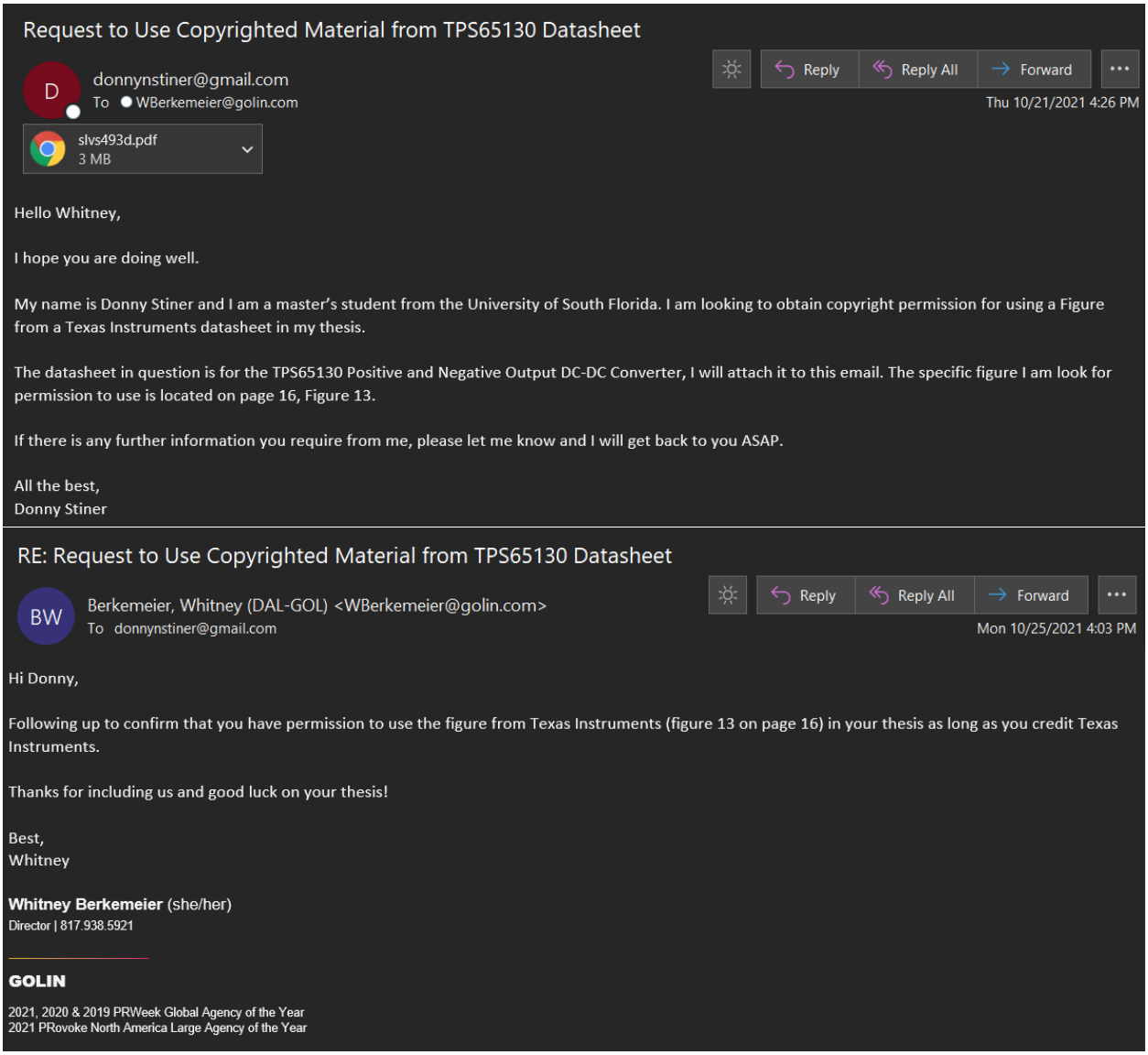
Natalie Moreton | Digital Marketing Manager
+44 (0)1223 810 261 | www.IDTechEx.com

IDTechEx

Providing business intelligence on emerging technologies for over 20 years. See our latest insights at www.IDTechEx.com

Head Office: 9 Hills Road, Cambridge, CB2 1GE, United Kingdom
Click Here to see our updated privacy policy

The permission below is for the use of Figure 3.1.



Request to Use Copyrighted Material from TPS65130 Datasheet

D donnynstiner@gmail.com
To WBerkemeier@golin.com

Reply | Reply All | Forward

Thu 10/21/2021 4:26 PM

slvs493d.pdf
3 MB

Hello Whitney,

I hope you are doing well.

My name is Donny Stiner and I am a master's student from the University of South Florida. I am looking to obtain copyright permission for using a Figure from a Texas Instruments datasheet in my thesis.

The datasheet in question is for the TPS65130 Positive and Negative Output DC-DC Converter, I will attach it to this email. The specific figure I am look for permission to use is located on page 16, Figure 13.

If there is any further information you require from me, please let me know and I will get back to you ASAP.

All the best,
Donny Stiner

RE: Request to Use Copyrighted Material from TPS65130 Datasheet

BW Berkemeier, Whitney (DAL-GOL) <WBerkemeier@golin.com>
To donnynstiner@gmail.com

Reply | Reply All | Forward

Mon 10/25/2021 4:03 PM

Hi Donny,

Following up to confirm that you have permission to use the figure from Texas Instruments (figure 13 on page 16) in your thesis as long as you credit Texas Instruments.

Thanks for including us and good luck on your thesis!

Best,
Whitney

Whitney Berkemeier (she/her)
Director | 817.938.5921

GOLIN

2021, 2020 & 2019 PRWeek Global Agency of the Year
2021 PRovoke North America Large Agency of the Year

The permission below is for the use of Figure 3.5.

CCC | Marketplace™

This is a License Agreement between Donny Stiner ("User") and Copyright Clearance Center, Inc. ("CCC") on behalf of the Rightsholder identified in the order details below. The license consists of the order details, the CCC Terms and Conditions below, and any Rightsholder Terms and Conditions which are included below.

All payments must be made in full to CCC in accordance with the CCC Terms and Conditions below.

Order Date	26-Oct-2021	Type of Use	Republish in a thesis/dissertation
Order License ID	1157103-1	Publisher	TAYLOR & FRANCIS GROUP LLC
ISBN-13	9780849322600	Portion	Image/photo/illustration

LICENSED CONTENT

Publication Title	Power electronic modules : design and manufacture	Country	United States of America
		Rightsholder	Taylor & Francis Group LLC - Books
Author/Editor	Colino, Ronald P., SHENG, WILLIAM W.	Publication Type	Book
Date	09/29/2004		
Language	English		

REQUEST DETAILS

Portion Type	Image/photo/illustration	Distribution	Worldwide
Number of images / photos / illustrations	1	Translation	Original language of publication
Format (select all that apply)	Electronic	Copies for the disabled?	No
Who will republish the content?	Academic institution	Minor editing privileges?	Yes
Duration of Use	Life of current edition	Incidental promotional use?	No
Lifetime Unit Quantity	More than 2,000,000	Currency	USD
Rights Requested	Main product		

NEW WORK DETAILS

Title	Development of Small-Scale Power Supplies for Wearable Medical Diagnostic Devices	Institution name	University of South Florida
		Expected presentation date	2022-10-01
Instructor name	Arash Takshi		

ADDITIONAL DETAILS

Order reference number	N/A	The requesting person / organization to appear on the license	Donny Stiner

REUSE CONTENT DETAILS

Title, description or numeric reference of the portion(s)	Figure 4.2: A ramp / soak / spike reflow profile for 63Sn / 37Pb solder	Title of the article/chapter the portion is from	Manufacturing of Power IGBT Modules
Editor of portion(s)	Donny Stiner	Author of portion(s)	Colino, Ronald P.; SHENG, WILLIAM W.
Volume of serial or monograph	1st	Issue, if republishing an article from a serial	N/A
Page or page range of portion	?	Publication date of portion	2004-09-29