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Packaging of Active RF Beamforming IC Utilizing Additive Manufacturing

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Packaging of Active RF Beamforming IC

Utilizing Additive Manufacturing

by

Ryan Murphy

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Electrical Engineering
Department of Electrical Engineering
College of Engineering
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Abstract

Packaging of an RF Beamforming IC was performed using an additive manufacturing platform with FDM, microdispensing, laser subtractive manufacturing, and milling. The beamforming IC was embedded within a multilayer device structure in order to feed a 2x2 antenna sub-array in a compact and completely integrated package. Additive manufacturing allows for simple variation in material parameters and properties that enhances the ability to develop integrated system packaging. This study builds on previous investigations and demonstrates the ability to embed an active RF device with measurable gain within a printed plastic substrate. Critical to developing a repeatable method for this packaging solution, initial studies were made to characterize the materials used and to duplicate the structures and printing methods needed to fabricate the final device.

The commercial-off-the-shelf beamforming IC uses mixed signal technology to allow for RF I/O and digital control to allow for phase shifting of the different channels. This chip also exhibits a dense array of pads as compared to other packaging solutions using additive manufacturing. Several steps are required to complete the testing including printing low loss, small width interconnects to address signal routing of printed RF and DC transmission lines. Due to the active devices on the beamforming IC, thermal management required changes to the initial design and altered antenna performance.

Chapter 1: Introduction

Additive manufacturing is the process of building a structure layer by layer to develop a single part and has come to envelope several different technologies including Fused Deposition Modeling (FDM) which requires a thermoplastic that is extruded from a nozzle and hardened layer by layer on a surface to build a structure, Selective Laser Sintering (SLS) where a laser is used to fuse tiny particles together to slowly build up the device, Binder Jet Printing which utilizes a printer head that dispenses a binder to temporarily hold particles together until they can be infiltrated by another material at a high temperature to improve the mechanical characteristics, and new additive manufacturing methods are constantly being investigated and pursued all for the same goal to reduce cost of manufacturing for complex designs and to offer flexibility with material properties or geometry that traditional manufacturing methods can't achieve. The RF field has taken a particular interest in additive manufacturing to realize better performing devices and more cost effective methods to develop a similar performing device.

1.1 Direct Digital Manufacturing

Direct Digital Manufacturing (DDM) is the ability to take a design from a computer and to manufacture it on a single platform without significant human input. Within this study, a particular facet of DDM utilizing a single platform tool with the ability to perform additive and subtractive manufacturing with a variety of materials is demonstrated for the development of packaged RF devices. One of the key advantages of direct digital manufacturing is the ability to customize material properties through different parameters or material preparation techniques and also the

ability to use customized layer heights and material geometry to do things that may otherwise be impossible through traditional manufacturing on a Rogers's board or other purchasable substrates. Specifically within this paper, fused deposition modeling (FDM) and micro-dispensing are utilized with ABS and a variety of different inks are tested.

1.2 Laser Enhanced Manufacturing

In previous studies, the use of an optical laser has been shown to complement the development of additive manufacturing by allowing very precise subtractive modification to the printed device. A picosecond laser for micromachining to show improved high frequency performance and design capabilities by providing lower loss through vias that have been laser machined away and providing improved conductivity through the improved heating on the edges of micro-dispensed conductive ink used as the microstrip lines [1]. Similar studies mentioned their results being dependent upon the functionality of the laser to print W-band CPWs with small spacing's only realizable with the precision of the laser [2]. Another study showed the ability to create spiral inductors within a plastic package using FDM and laser machined cavities. [3].

1.3 Device Packaging Using Additive Manufacturing

The ability to develop and realize specific RF components using additive manufacturing is useful and allows a more cost effective solution however, the real benefit is being able to integrate several components within an integrated package solution using additive manufacturing. A study was performed to investigate different embedding orientations for active RF devices such as a ring resonator and tunable patch antenna using additive manufacturing to exhibit better electrical performance [4]. Other work has addressed the ability to stack different substrates and components through a 3d printed interposer layer [5]. Integrating passives into an embedded system becomes

critical when bypassing and matching is needed off chip and a study addressed the ability to print different passives using different additive manufacturing techniques [6].

One of the papers that initiated this thesis was the packaging of a 75-110 GHz communication system which utilizes additive manufacturing to develop novel interconnects and packaging that exhibits performance that exceeds conventional packaging [7].

1.4 Antennas

Additive manufacturing has been used to print antennas to explore the possibilities of driving down the cost of phased arrays and to offer more compact, broadband solutions then what has typically been developed using traditional manufacturing.

A multilayer antenna structure was developed and embedded with passive phase shifter MMIC elements using direct digital printing on a similar platform to what is being utilized at the University of South Florida [8]. These studies have laid the foundation for this work which is an attempt to realize more complete front end modules that are completely integrated using additive manufacturing [9]. While these papers lead to the development of antenna arrays, additive manufacturing has proven itself to produce Ka-band and V-band corrugated horn antennas with 6-8 dB gain using a polyjet technology with curable photopolymer [10]. A 3D Lundeberg lens antenna was also fabricated for K-band using additive manufacturing and a dielectric flat plate lens antenna was printed and showed the advantages of 3D printing by allowing more efficient geometries and customizable dielectric properties [11] [12].

Extremely high frequency corrugated horn antennas up to 300 GHz were fabricated using additive manufacturing for a more lightweight design and electroplated with gold to improve the materials conductivity [13]. A study also was done to consider other advantages to additive manufacturing for the fabrication of patch antennas where an air cavity was constructed to attempt

to increase the bandwidth compared to a traditional patch antenna [14]. A C band antenna front end was printed on the surface of a printed substrate and showed the ability to print and embed multiple different components eventually leading to an antenna [15].

1.5 Thesis Outline and Contributions

This work shows the capabilities to embed and package active RF components using additive manufacturing and documents the buildup and fabrication of the device.

In Chapter 2, this work attempts to investigate different conductive inks to allow for a higher conductivity to reduce significant power loss along transmission lines of considerable length. Different conductive inks with smaller particle size also improves the microdispensing ability to permit smaller feature printing and the ability to print high density circuitry.

In Chapter 3, while additive manufacturing is being pursued by many research groups and companies, one of the largest drawbacks preventing significant practical use is the heat handling capabilities of many materials that additive manufacturing utilizes. The low heat handling capability restricts the level of active circuitry that can be integrated into the printed substrate due to the material's low glass transition temperature. This paper investigates the different parameters that greatly impact the ability to dissipate heat and offers a solution in a single case to embed active circuitry into a printed substrate.

In Chapter 4, with the materials further investigated and thermal handling characterized, an active device is embedded into a multilayer package to provide appropriate feeding to an antenna array with the ability to scan in different directions. While similar devices have been printed, this study contains components with a high pad density requiring alternative techniques print the device in a feasible manner.

Chapter 2: Process Development and Material Characterization

Although significant research on 3D printing RF devices has been performed, the ability to package devices using additive manufacturing has experienced limitations due to material capabilities as more realistic and practical circuits are attempted to be printed. Like traditional manufacturing of circuit boards or any RF/microwave device, there is a need for precise conductive elements, dielectric substrates, and usually a method for subtractive manufacturing for vias or cavities. On the 3D printing platform used within this study, a substrate is directly printed layer by layer using Fused Deposition Modeling (FDM) and a conductive paste is dispensed from a pressurized syringe on to the substrate on the same platform. The process of developing vias or cavities can be done during the FDM stage where the substrate is printed one layer at a time around the cavity or in other cases it can either be milled away or lasered away depending on the platform capabilities. Lasering or milling, both provide more precise methods of small features such as vias or small component cavities.

In this study, an nScrpyt 3Dn-Tabletop with an nFD and Smartpump gizmo is utilized for both the FDM process for printing the substrate and the micro dispensing of the conductive paste for signal and ground layers. The subtractive process for development of cavities and vias is done using a Coherent picosecond laser at 355 nm wavelength to remove substrate material as well as a milling capability on a different printing platform. In order to facilitate smooth printing of packaged devices, thorough investigation of necessary printing scenarios and conductive inks were tested to develop the optimum recipe for circuit integration.

2.1 Substrate Characterization

The choice of substrate in a traditional sense would depend on the needed mechanical stiffness, the thermal conductivity, dielectric permittivity, loss tangent, and maximum temperature experienced for a particular application. Due to the inherent need for FDM thermoplastics to have a low melting temperature, our substrate material choice in the recent years have been limited to plastics with melting temperatures lower than around 300 C due to equipment limitations and need to reduce heat spreading up the extruder housing where melted plastic away from the extruder nozzle could develop and prevent extrusion. While the options are limited we still desire mechanical strength and resistance to the environment so Acrylonitrile butadiene styrene (ABS) was chosen for this study. While higher permittivity and lower loss plastics are being developed for FDM such as COP-MgCaTIO$_2$, they typically require higher melting temperatures and the smaller circuit size that would be enabled for a higher permittivity substrate requires highly precise dispensing of conductive paste [16].

To characterize the substrates utilized within this study and ensure confidence in simulation parameters a 0-20 GHz cavity resonator and (ENA) was used to measure the loss tangent and permittivity within the target frequency range.
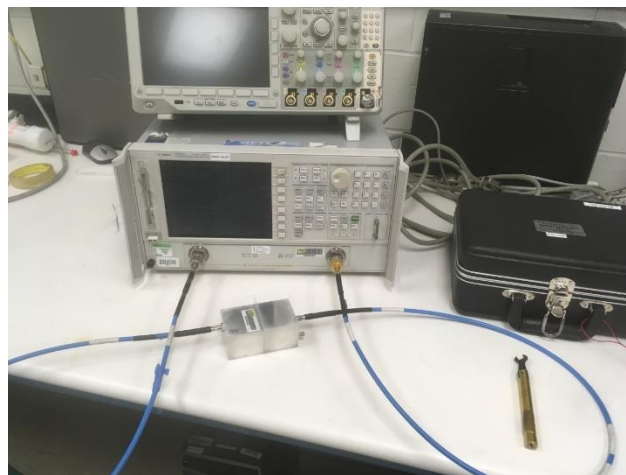
Figure 2.1 – Measurement setup for permittivity and loss tangent up to 20 GHz
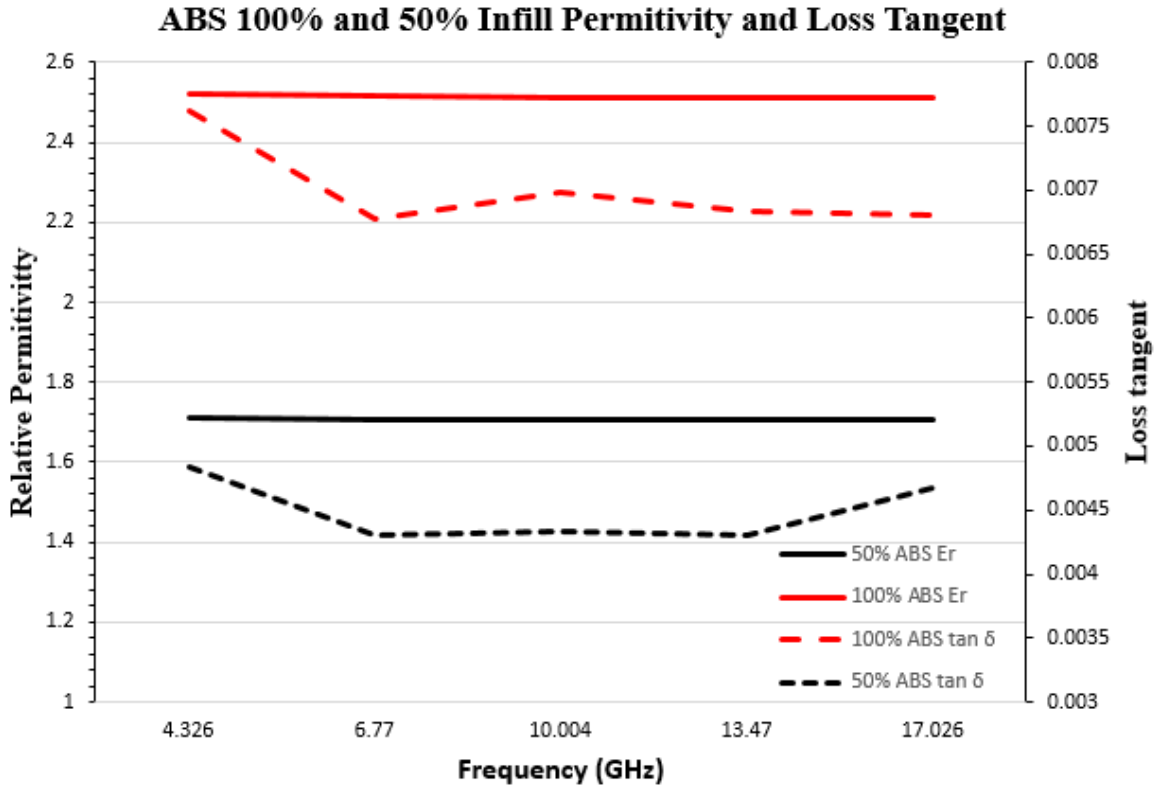
Figure 2.2 – Measurement results for 100% and 50% Infill ABS

As seen in Figure 2.2, the permittivity and loss tangent are measured at specific resonant frequencies and remains pretty constant (ε_r = 2.51 +/- 0.01) (Tan б = .007 +/- .0005) across the measured frequency range. This supports previous measured data where the permittivity was measured to be about 2.4 and the loss tangent around 0.006, however, ABS has been shown to absorb moisture over time and would expect to increase the loss and increase the permittivity. Based on the printing platform available, substrates with higher glass transition temperatures or more desirable performance can be printed if the extruder is compatible with the printing temperatures and methods needed but ABS is investigated for the purposes of this study. To compare this substrate to other commonly used substrates including other material properties, the following table was constructed.

Table 2.1 – Substrate properties at 10 GHz

Plastic	Dielectric Constant	Loss Tangent	T_g (C)	Specific Heat (J/kg C)	Thermal Conductivity (W/m K)	Density (kg/m^3)	FDM Compatibility
ABS (50%, 100%)	1.7, 2.51	0.004, 0.007	90	1990	0.172	1080	Good
PLA [18]	3.471	0.073	53	-	-	1290	Good
PC [19]				1540	0.196	1200	
PEEK [20]	3.2 – 4.5	-	146	1570	.293	1330	Moderate
COP MgCaTIO$_2$ [21]	4.6	0.003	-	-	-	-	Moderate
COP [22]	2.1	0.0004	136	-	-	1010	Bad
RT/duroid 5870 [23]	2.33	0.0005	-	960	0.220	2200	No
RO4000 [24]	2.55 – 6.15	0.002	280	-	0.71	1790	No

2.2 Microdispensing Conductive Pastes

The development and choice of the conductive ink is primarily dependent on the method for placing it on the substrate with high accuracy. The nScrypt platform we have been using has the capability to dispense conductive pastes with viscosities between 1 cP and 10^6 cP. Particular materials properties have been investigated and reported, however limited studies have been done on the necessary DC and RF conductivity of some inks at low curing temperatures which is required for usage on ABS. Due to microdispensing paste thickness having a significant impact on laser performance and effective permittivity of CPW traces it is imperative that not only characterization is done, but also extensive process development to be aware of what thickness is being dispense and how this will impact subsequent layer processes.

The following study investigates the DC conductivity of 3 different inks using a 4-point probe measurement scheme, the Van der Pauw method, and a mechanical profilometer to measure the cured thickness and evaluate the material conductivity.

Figure 2.3 – CB028, Novacentrix FG57B, and Novacentrix FG77 dispensed onto Kaptop tape in 10 mm squares.

The 3 inks were dispensed using the same code, Z-height above substrate, and printing parameters aside from increasing the syringe pressure on FG57B to get similar volume flow due to its higher visocsity. It should be noted that for CB028, FG57B, and FG77, the reported particle size (Mass Loading %) is 10 µm (60%), 1.5 µm (70%), and 0.3 µm (85%), respectively [25][26]. Several 10 mm squares of each material were printed on kapton tape and cured in an oven at different temperatures and different lengths of time to observe the effects on conductivty within the limited thermal limits avaialbe when using ABS as the substrate. After the test results were found through curing in an oven, a Pulseforge machine was used to perform photonic curing further investigate how to improve conductivity.
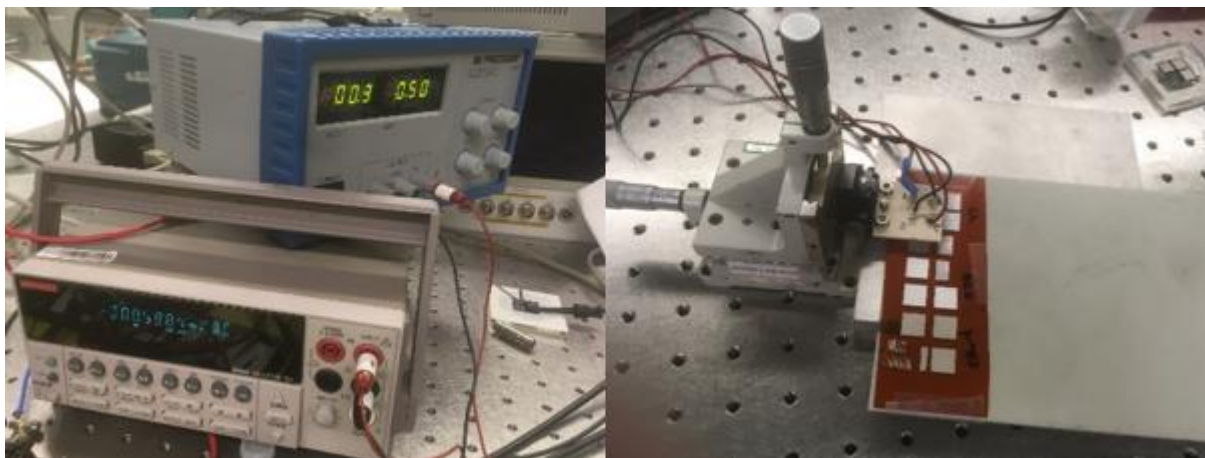
Figure 2.4 – Test setup for 4 point probe with DMM and DC power supply in constant current mode (Left) and the probe holder and kapton substrate with various samples of each ink (Right).

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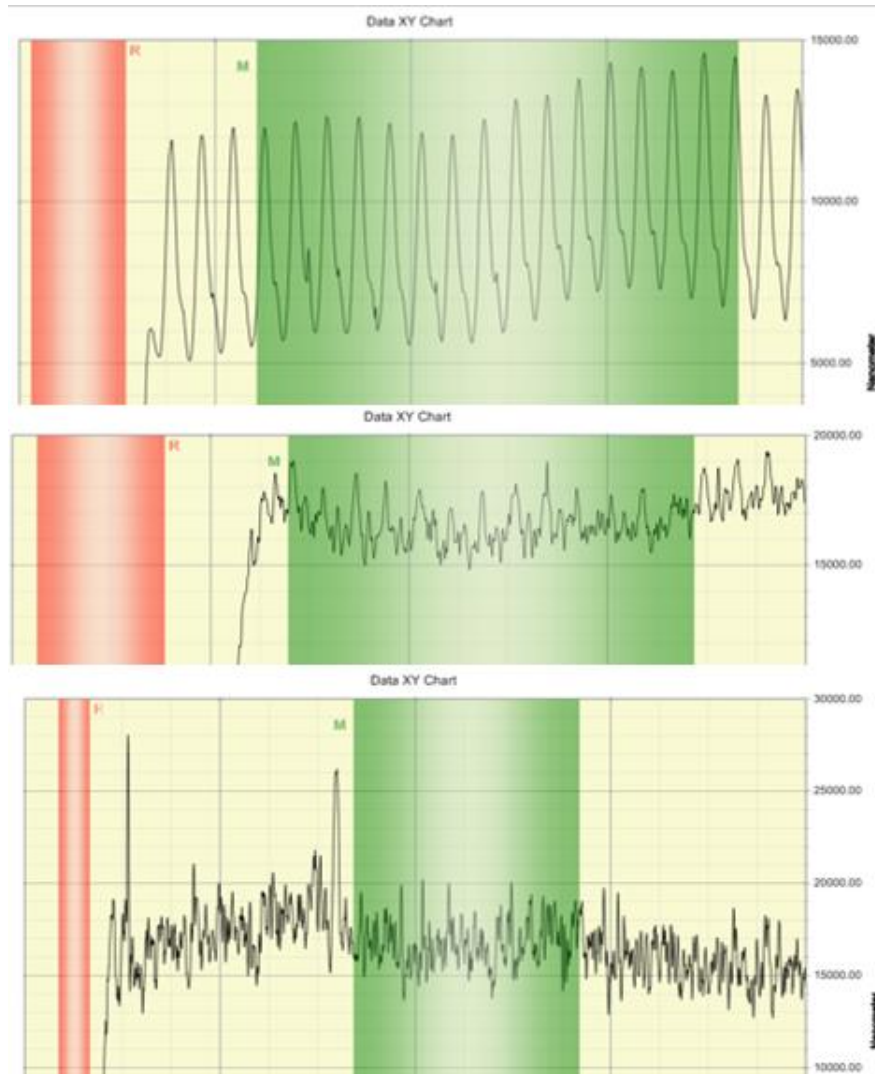
Figure 2.5 – Mechanical profilometer measurements made after curing the ink at 90C for 3 hours. (Top) FG77 with an average height of 10 µm and roughness 2.36 um. (Middle) FG57B with an average height of 17 µm and roughness 2.5 um. (Bottom) CB028 with an average height of 17 µm and roughness of 2 um.

The above 3 figures were measured on a mechanical profilometer over the printed area where the DC 4-point probe measurement was made. The green area represents the area where height and roughness are measured with respect to the red area. The red area in the case above was selected as the kapton tape before the mechanical profilometer tip reached the conductive ink.

Figure 2.6 – DC Conductivity Comparison for the 3 inks with respect to curing steps.

The DC conductivity of different inks was investigated at different stages when using a traditional oven to cure the inks. As seen in Figure 2.6 an expected gradual increase was measured as solvents in the ink were evaporated and the silver particles were drawn closer to each other. At these temperatures it may not be accurate to characterize the ink as being cured but rather only dried.
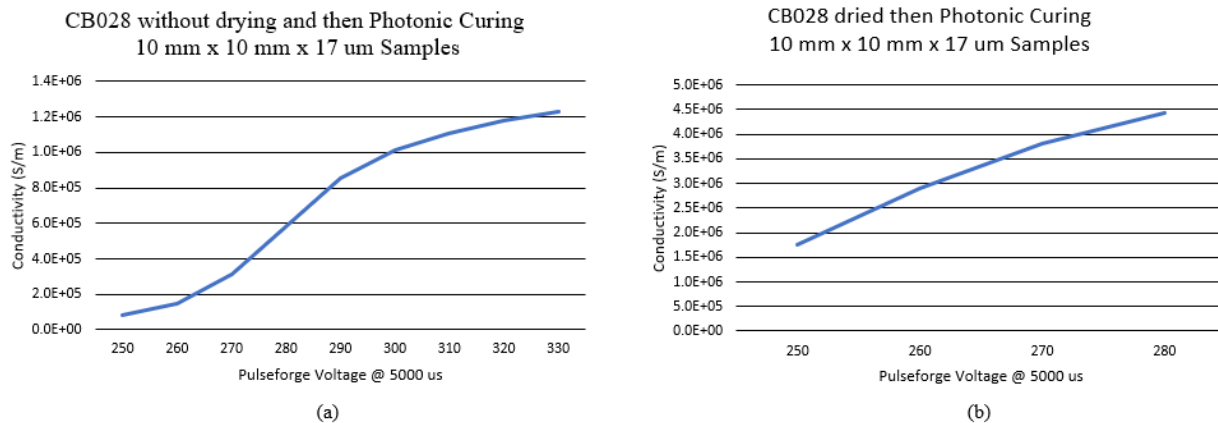
Figure 2.7 – CB028 conductivity after photonic curing and under different conditions. (a) After ink has been recently dispensed and before drying and (b) after ink has dried on the printer bed at 90C.

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Pre Dried and Photonic Curing
FG57B (orange) and FG77 (blue)
10mm x 10mm x 17 um Sample
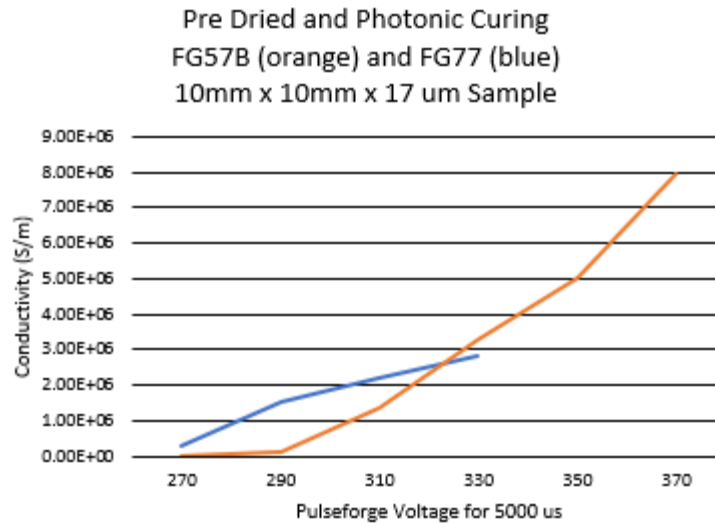
Figure 2.8 – FG57B and FG77 after drying and curing.

The pulseforge utilizes capacitor charging banks to discharge a high voltage to a broadband lamp with wavlegnths ranging from 200nm to 1500 nm. Due to the limited experience with the photonic curing process within the group, experimental testing was initially performed to establish the operating limits of the process with each print on kapton and on ABS. It was observed that the inks on kapton could withstand higher voltages and only expeiencing failure through loss of adhesion to substrate likely due to evaporating or altering of chemicals ink responsible for surface adhesion. The inks printed on ABS experienced failure earlier through a burning of the substrate and drastic increase in surface roughness. The burning is likely due to the silver particles in the ink absorbing the wideband light and converting the energy to thermal energy. The localized thermal energy results in abrupt increases in substrate temperature, causing buring. Although a voltage limit for photonics curing could be found based on the prints used it was also discovered it was dependant on the amount of ink exposed to the wideband light allowing for it to dissipate the energy easier. Failure was most often observed on small traces when experiementing with other substrates that had been printed on.
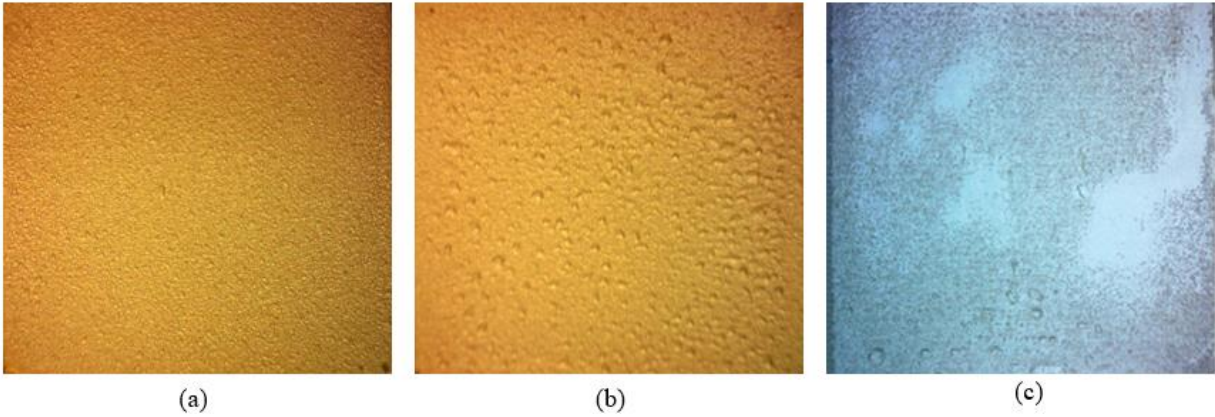
Figure 2.9 – FG57B after photonic curing under different conditions. (a) On Kapton tape 280V. (b) On Kapton tape 300V. (c) On ABS at 270V 5000 us.
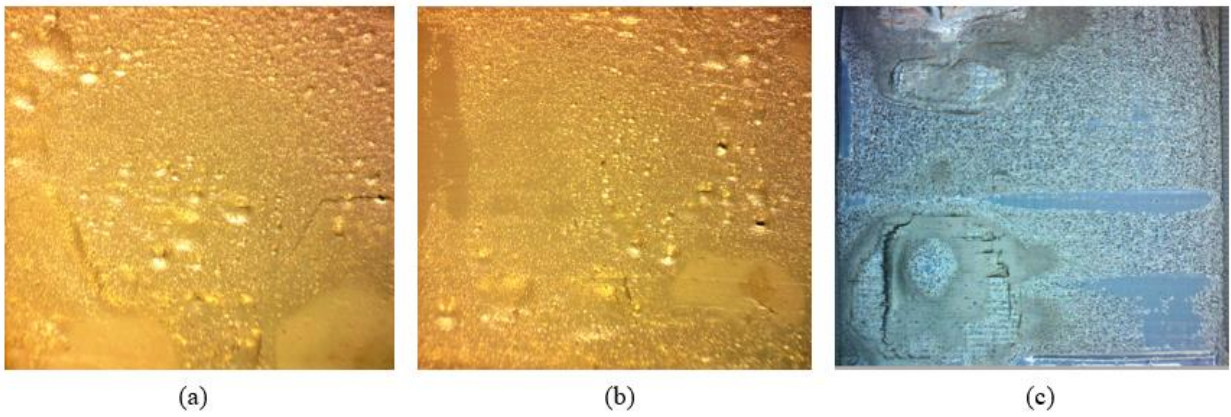
Figure 2.10 – FG77 after photonic curing under different conditions. (a) On Kapton tape 280V. (b) On Kapton tape 300V. (c) On ABS at 260V 5000 us.
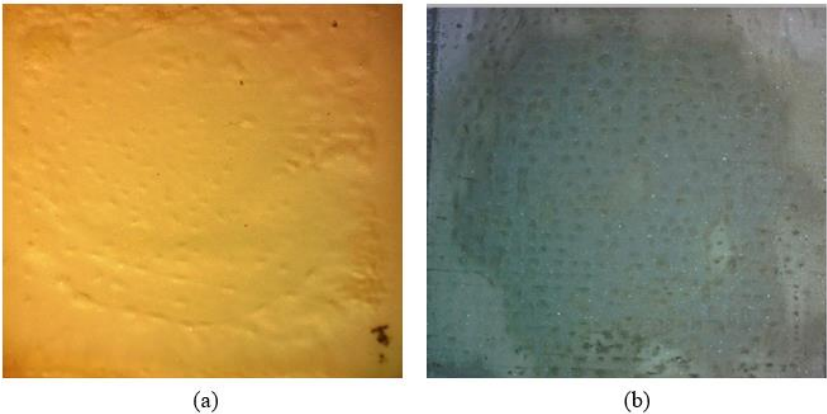
Figure 2.11 – CB028 after photonic curing under different conditions. (a) On Kapton tape 250V. (b) On ABS at 260V 5000 us.

It is worth noting that the ink is not curing at these temperatures based on the datasheet listed resistivity, and is instead drying and forming a smaller trace volume where the particles are just closer together. Although these inks are not recommended for use below 120C, based on experience with CB028 where moderate conductivity was shown at a lower curing temperature, the inks with smaller particles sizes do not appear to be exhibiting the same performance. CB028 at low temperatures is roughly 2.5x more conductive than the other inks and all inks level out at 90C for 3 hours and start to increase again once they were baked at 120C.

To further characterize the inks and measure the performance at higher frequencies, a 4-layer board was printed for each ink in a CPWG to microstrip to CPWG connectorized configuration as seen in Figure. The device was fabricated in a 4-layer configuration to allow for a thick base substrate for mechanical support for the ground layer to be printed on. This is followed by printing of the microstrip ABS substrate and conductive ink microstrip layer.
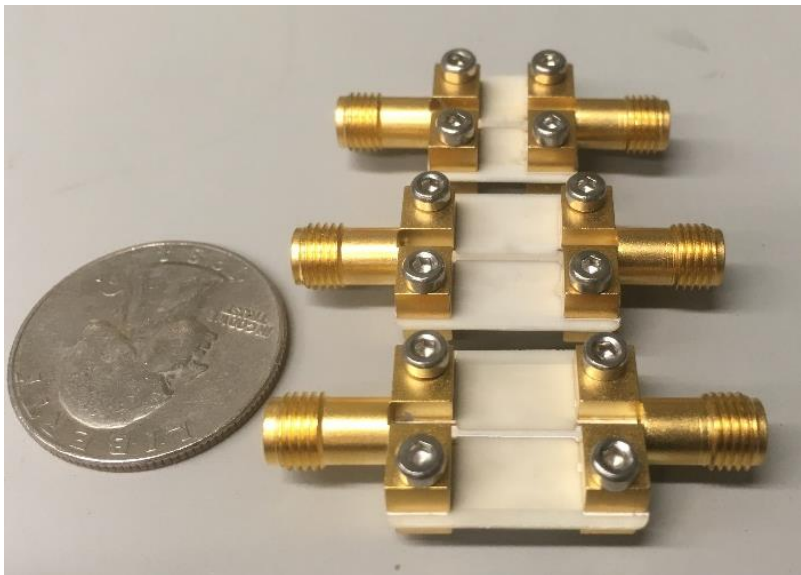
Figure 2.12 – 5 mm and 10 mm CPWG-Microstrip-CPWG test substrates with Rosenberger connectors. 4 Layer printed structures with printed ground layer under visible microstrip trace.
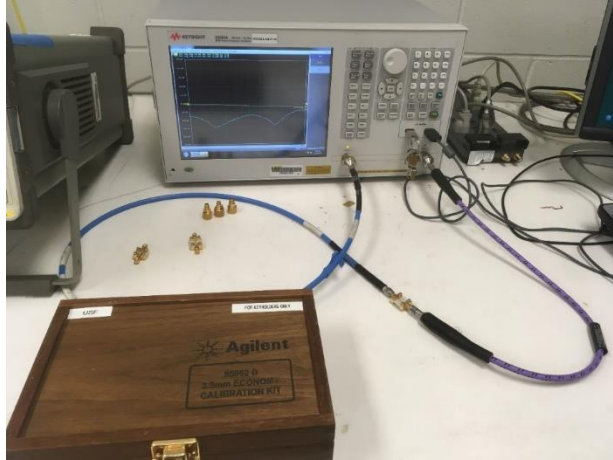
Figure 2.13 – Test setup for connector measurement with 85052D calibration kit.

With the Rosenburger connectors removed the following images were taken. The prints involved filling of via holes to connect the GCPW pads to the bottom ground plane and lasering the edges of the pads to get the appropriate spacing. In Figure (a) additional laserign was needed to repair a shorted gap when applying conductive epoxy to the connector center conductor to establish a good connection.
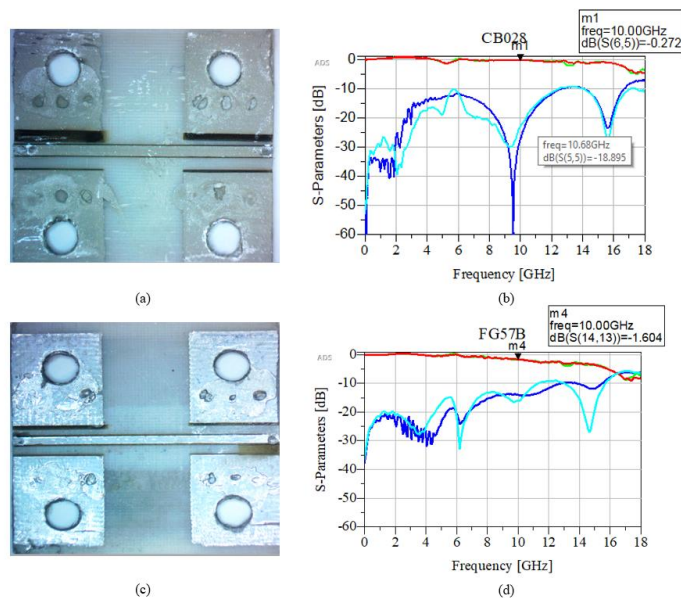
Figure 2.14 – GCPW prints using (a) CB028 and (c) FG57B and cooresponding measured results for (b) CB028 and (d) FG57B. The red and green curves are the S21 and S12 while the teal and blue curves are S11 and S22.

The return loss and several resonances observed in the measurements created reason to simulate and observe how the connector may be playing a role in the measurements. The Rosenberger connector was compared to a Southwest Microwave (SM) connector to simulate both an ideal condition with a good contact between the connector and substrate and a more realistic condition where there may be small gaps of around 50 µm between the connector and substrate in the lateral direction.
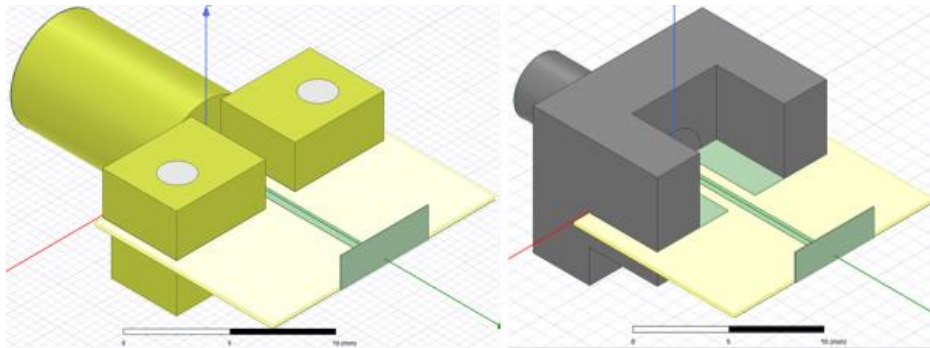
Figure 2.15 – Rosenberger connector and Southwest Microwave/Gigalane HFSS model for comparing GCPW lines.
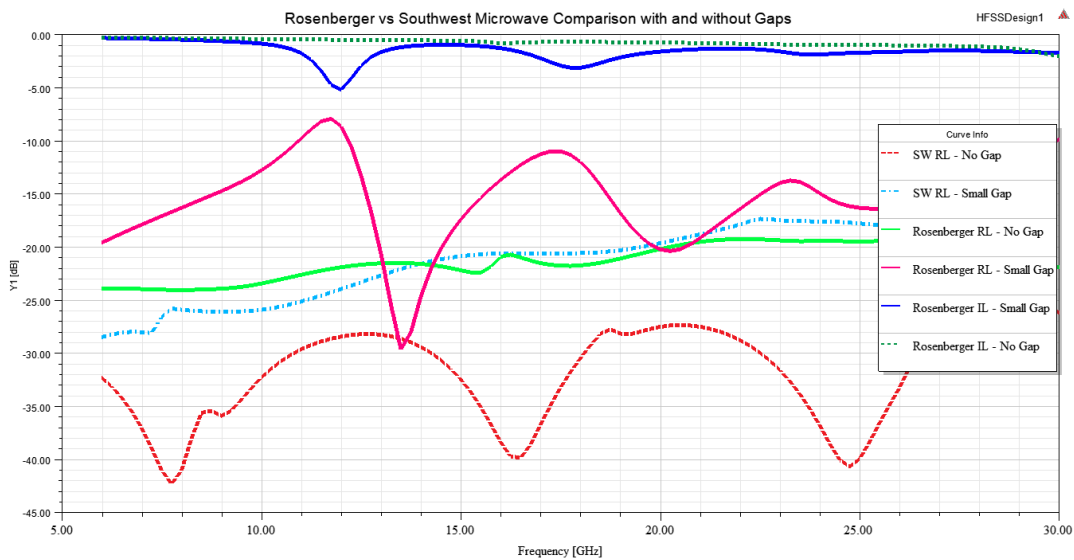
Figure 2.16 – Connector Insertion loss and Return loss comparison for Southwest Microwave and Rosenberger connectors. A small gap was also introduced between substrate substrate edge that touches the Coax cylindrical housing.

From the above results, the red dotted and solid green plots directly compare ideal Southwest Microwave (SM) and Rosenbeger connector return loss with the SM connector showing a 5 dB better return loss across the simulated frequency band in the ideal conditon. The teal dashed and pink solid represent performance with a small lateral gap and this makes it evident that the design of the Rosenberger connector makes it more suspecitble to probems and resonances when a small gaps are existent. This may also explain the resonancs from the measured data when using the Rosenberger connector where the surface roughness where the connector is seated may also be a problem.

A similar test was also done using a simple connectorized CPW with different inks to reduce the number of variables needed to characterize the performance. The main problem with fabriacting these models are the large continuous ground plane which may exhibit frequent clogging or air bubbles. The continuous stopping and dispensing on similar locations causes a larger ground plane thickness and affects the necessary laser passes to cut through the conductor. Printing on top of the large ground plane may also result in warping of the substrate as the temperature gradient between the materials grows with the heated bed on.

Figure 2.17 – CPW substrate with improved connectors (Left) and 10 mm CB028 and 5 mm FG77 substrates (Right).
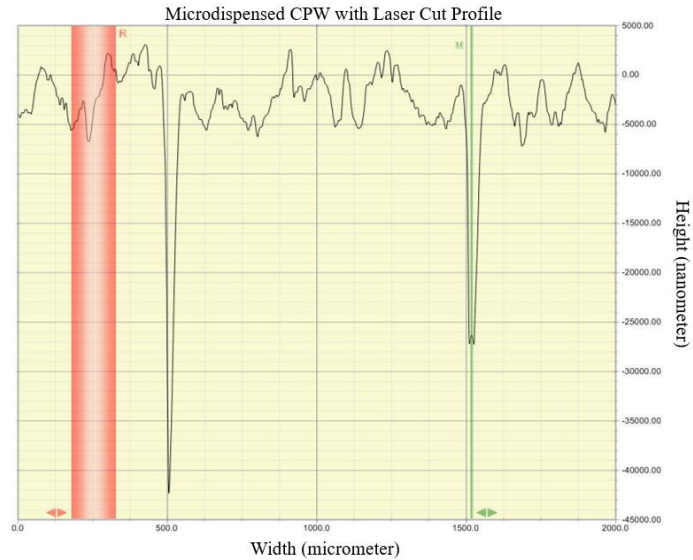
Figure 2.18 – Mechanical profilometer measurement of CB028 CPW fabricated by microdispenisng conductor layer and lasering gaps.

Measurements that didn't match the simulation as well as they should caused reason to again question the repeatability of the connectors and the quality of the print with respect to the geometry dimensions. Figure 2.18 shows the results of a mechanical profilometer measurement across a sample that resembles Figure 2.17 (right) to measure the depth and gap of the CPW spacing fabricated using the 355 nm laser. The plot shows a top surface of ABS with printed CB028 paste on top with an 8 µm thickness variation across the surface. The two valleys are the laser cut gaps which were designed to be 940 µm apart and 65 µm wide which matches the measurement pretty well. However, the number of cuts needed to succesfully separate the conductive regions results in a gradual widening in the gap near the top surface which could create problems and reduced return loss due to changes in the effective permittivity.

There were many samples printed in the configuration seen above with CB028, FG77, and FG57B conducitve inks, however, few of the measured results provided good and repeatable results. This is likely due to fabrication issues of printing the thin microstrip ABS layer above the ground plane where there is poor adhesion along the edges. The less conductive inks (FG57B and

FG77) may also show worse results due to a more resitive ground plane. Photonic curing was expected to show improvments as seen in the following sections, but the 4 layer print configuration with the connectorized interface did not provide repeatable enough results to deduce and measure noticable improvments with photnic curing. For this reason, an alternative print method to extract conductivity improvements was investigated.

The results from this study exposed difficulties with printing such as the reluctance for the 3rd layer nFD microstip substrate to stick to the 2nd layer ground plane. The Rosenberger connectors were also modeled and compared to Southwest (SW) and Gigalane connectors to see if there was a significant performance difference. From the models it is clear that the Southwest microwave has a better connection to ground whereas the Rosenberger greatly suffers if any gap is formed between substrate and connector.
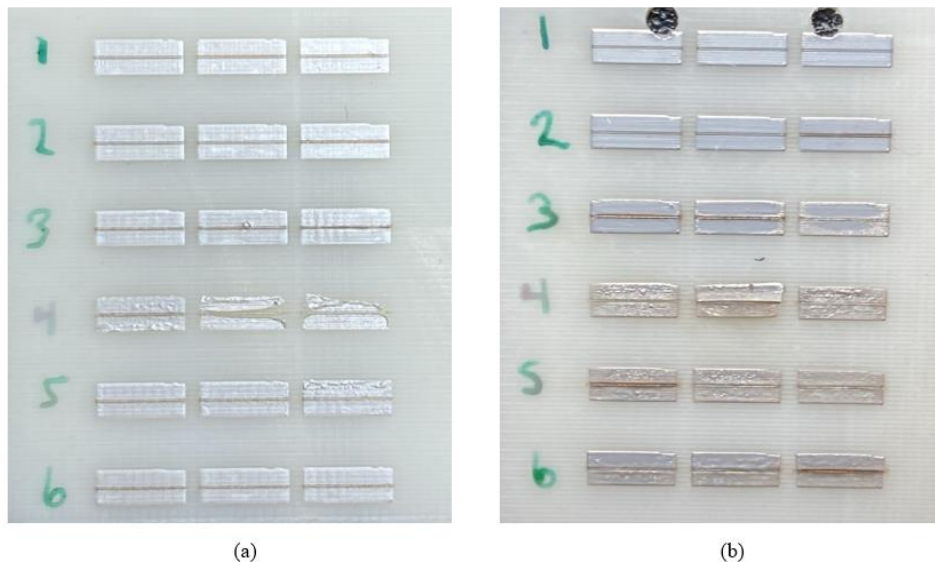
Figure 2.19 – 18 sample CPW substrates printed with (a) FG57B and (b) FG77 on ABS after photonic curing.
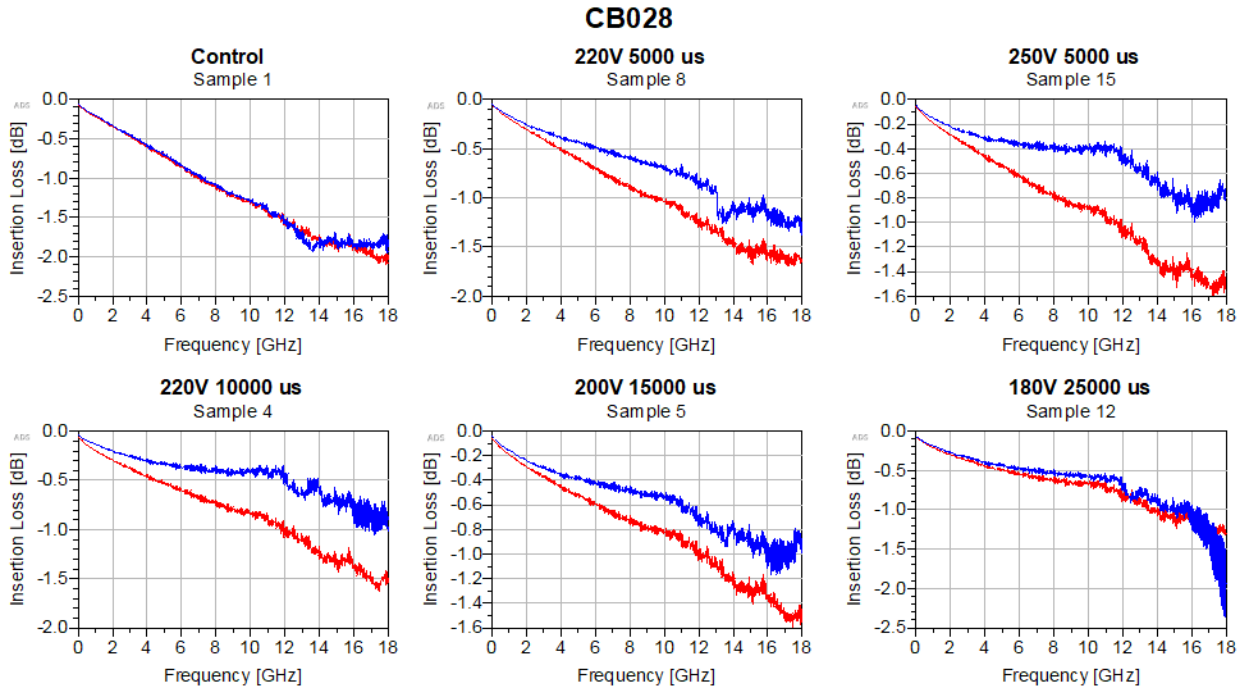
Figure 2.20 – CB028 CPW Insertion Loss results before photonic curing (red) and after photonic curing (blue).
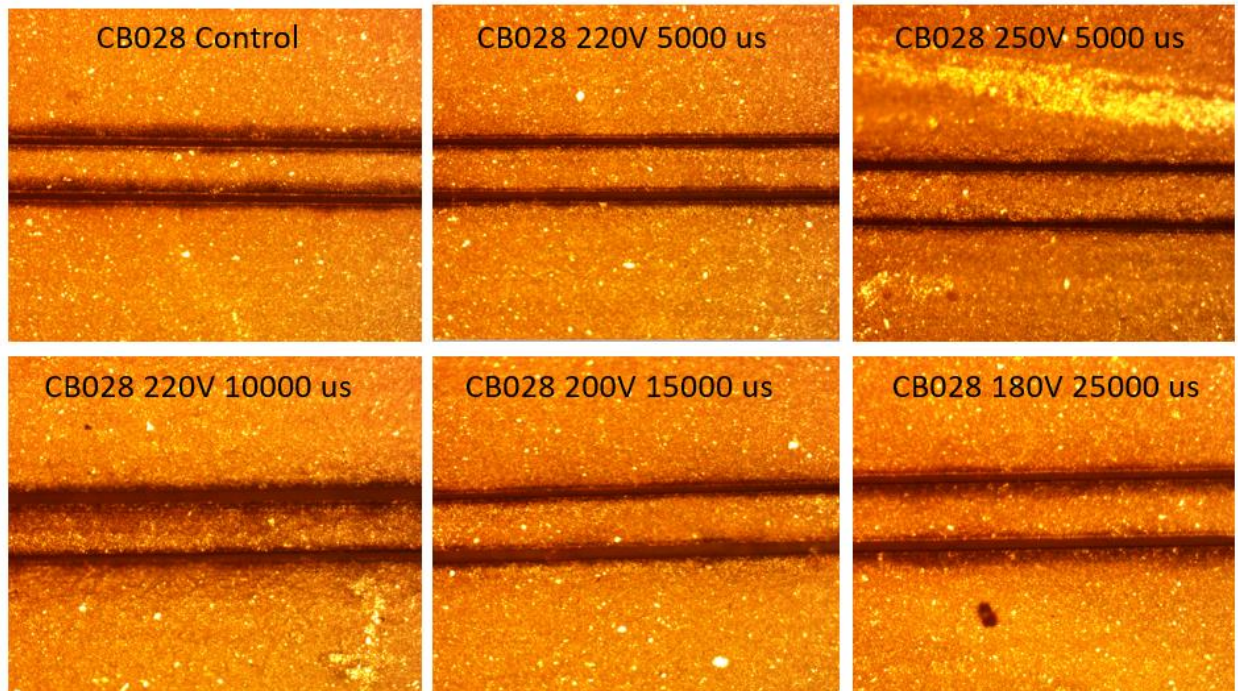
Figure 2.21 – Microscopic images of CB028 CPW's on probe station after different exposure to different photonic curing conditions.
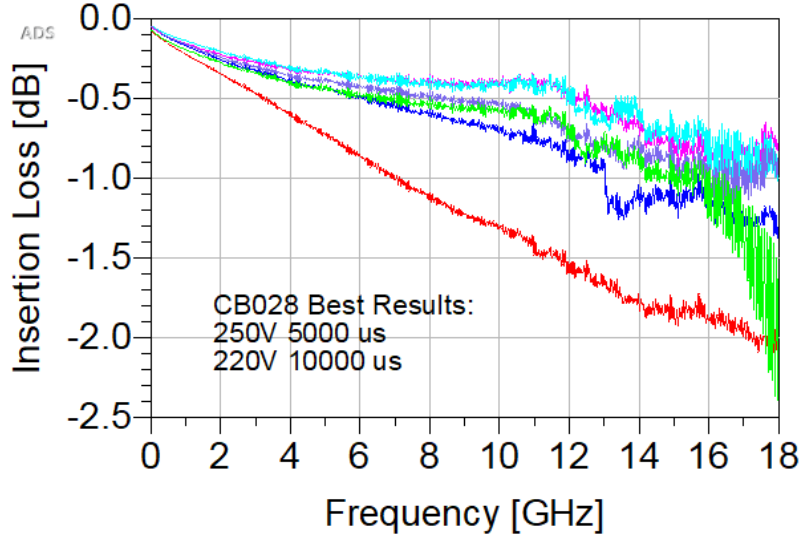
Figure 2.22 – Insertion loss comparison between the various photonic curing conditions on CB028.
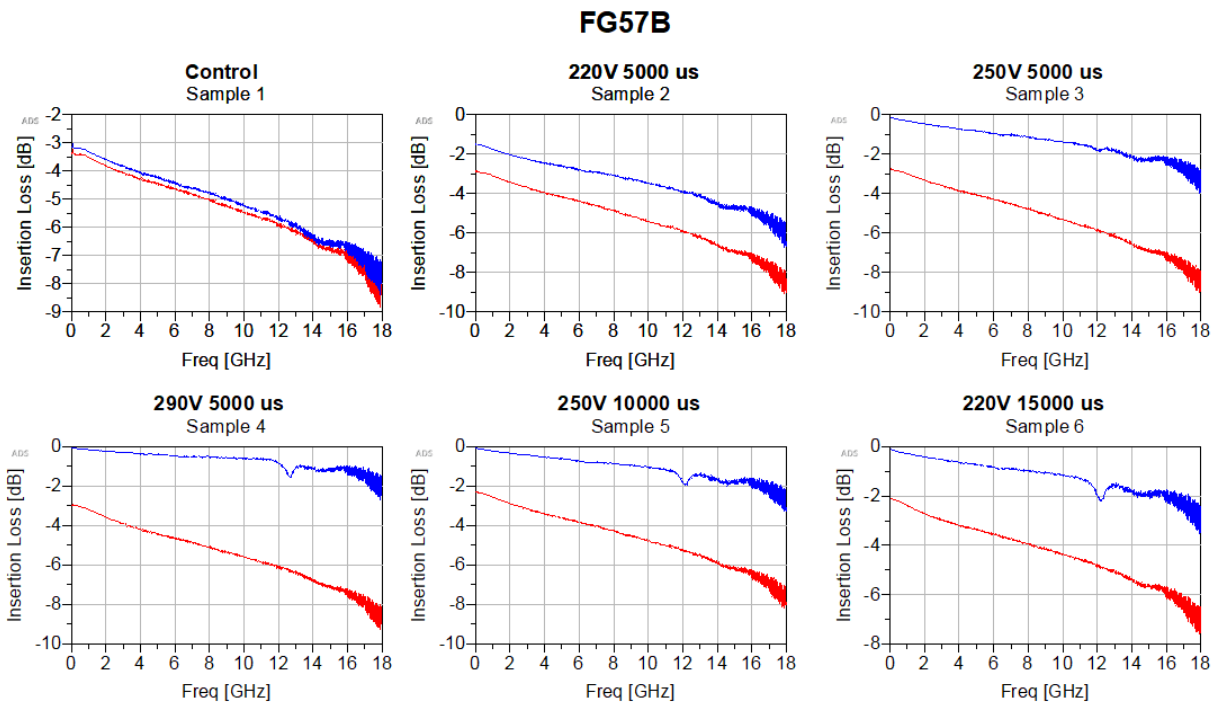
Figure 2.23 – FG57B CPW Insertion Loss results before photonic curing (red) and after photonic curing (blue).
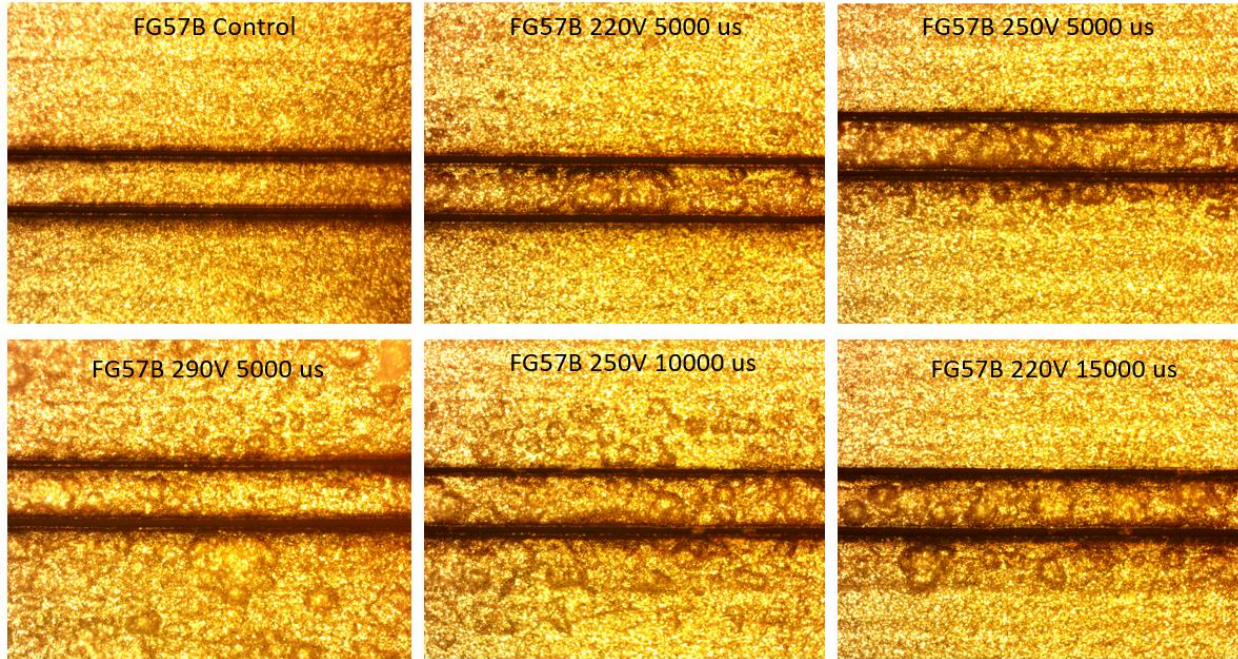
Figure 2.24 – Microscopic images of FG57B CPW's on probe station after different exposure to different photonic curing conditions.
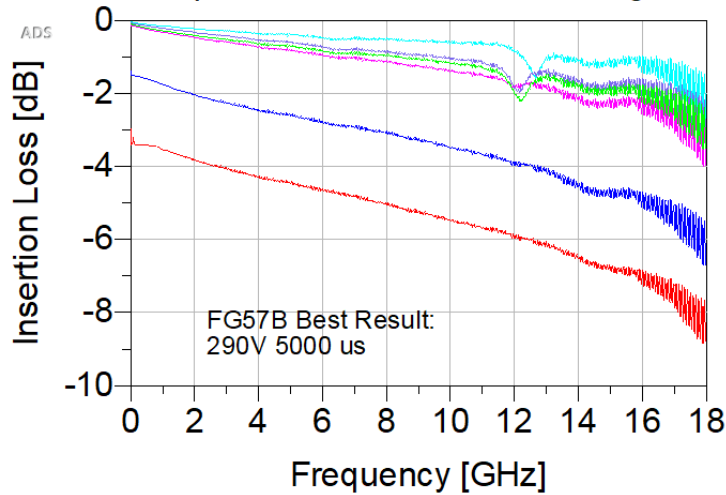
Figure 2.25 – Insertion loss comparison between the various photonic curing conditions on FG57B.
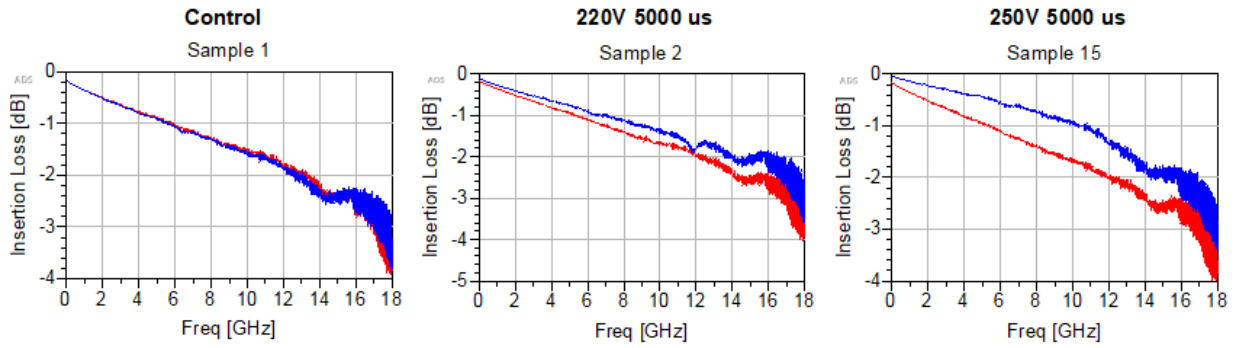
Figure 2.26 – FG77 CPW Insertion Loss results before photonic curing (red) and after photonic curing (blue).
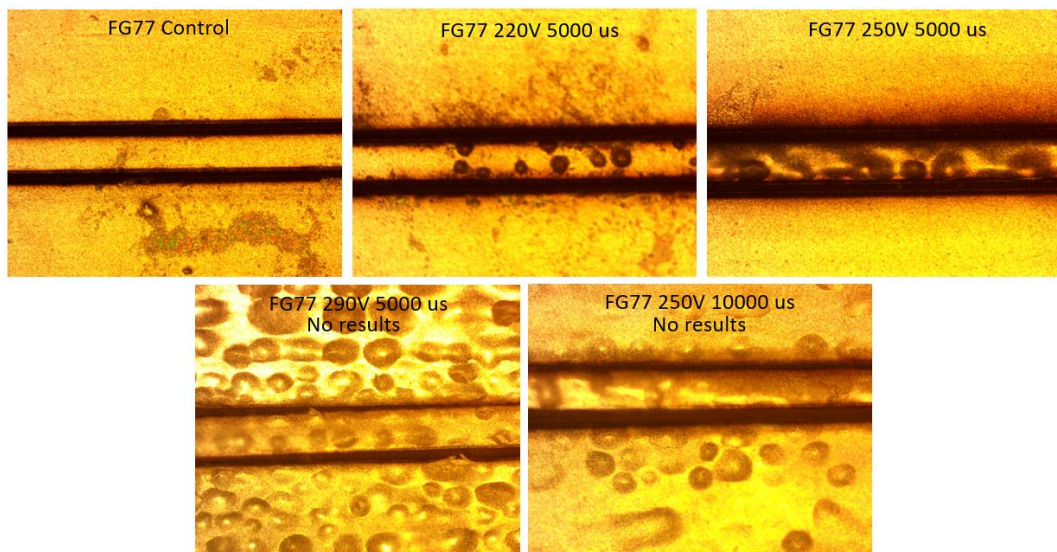
Figure 2.27 – Microscopic images of FG77 CPW's on probe station after different exposure to different photonic curing conditions.
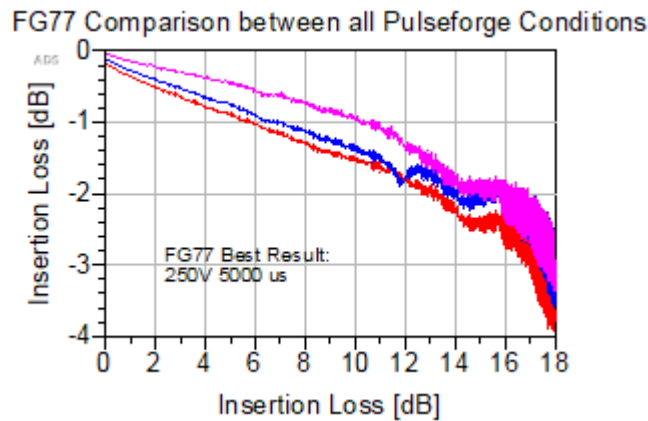
Figure 2.28 – Insertion loss comparison between the various photonic curing conditions on FG77.
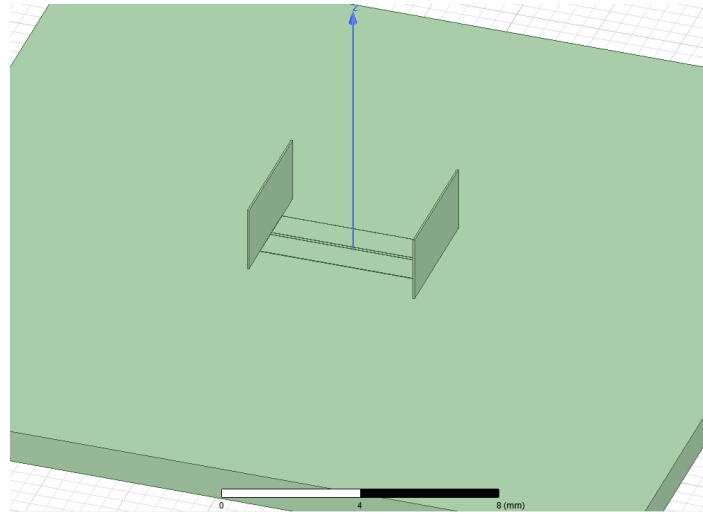
Figure 2.29 – CPW HFSS Simulation to extract RF conductivity.

A test structure within HFSS was simulated in order to extract the improvement in RF conductivity resulting from the photonic curing. Note the measurements were on 5 mm samples.

Table 2.2 – Conductor Properties

Materials	DC Conductivity (S/m)	RF Conductivity	RF Conductivity after photonic curing	RF loss per mm without photonic curing (10 GHz)	RF loss per mm with photonic curing (10 GHz)
CB028	1.45 E6	7.4 E6	17.6 E6	.27 dB/mm	.07 dB/mm
Novacentrix FG77	7.62 E5	3.5 E6	6.3 E6	.32 dB/mm	.2 dB /mm
Novacentrix FG57B	3.3 E5	.137 E6	6.3 E6	1 dB/mm	.25 dB/mm
Copper	5.96 E 7	-	-		
Aluminum	3.77 E 7	-	-		

2.3 Subtractive Manufacturing with Laser Machining and nMill

To develop the cavities for lumped components, fabricate vias, and trim microdispensed lines a picosecond laser was utilized. As mentioned in the introduction, the laser has a third harmonic wavelength of 355 nm which is used to obtain a smaller spot size compared to the fundamental frequency. At the cost of available power at lower voltage levels smaller features can

be cut compared to the larger wavelength options on this laser. For the final device, CPW to microstrip transitions, 0.2 mm and 0.5 mm vias, and 0402 component cavities are fabricated using the laser and further characterized below. The 7 mm square and 3 mm square cavities were also investigated to get finer and more precise features however, problems with the slope of the walls and handling of the chip restricted this method for deep cavities.

The laser power output from the software that is based on a detector measurement during laser operation allowed for the following plot of laser power vs high voltage power setting at a repetition rate of 100 kHz and is recorded below. High voltage power control is with respect to the laser fundamental frequency and because the third harmonic is being utilized for its smaller spot size, a nonlinear power output is expected with change to the power control.
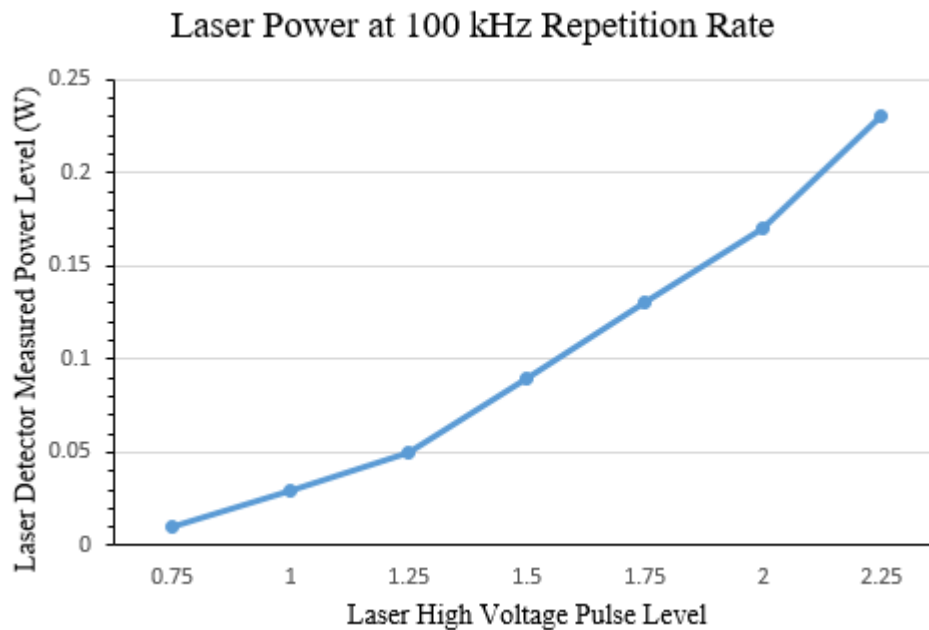
Figure 2.30 – Laser Power at 100 kHz vs High voltage setting read from laser detector in the Rapid software during operation.
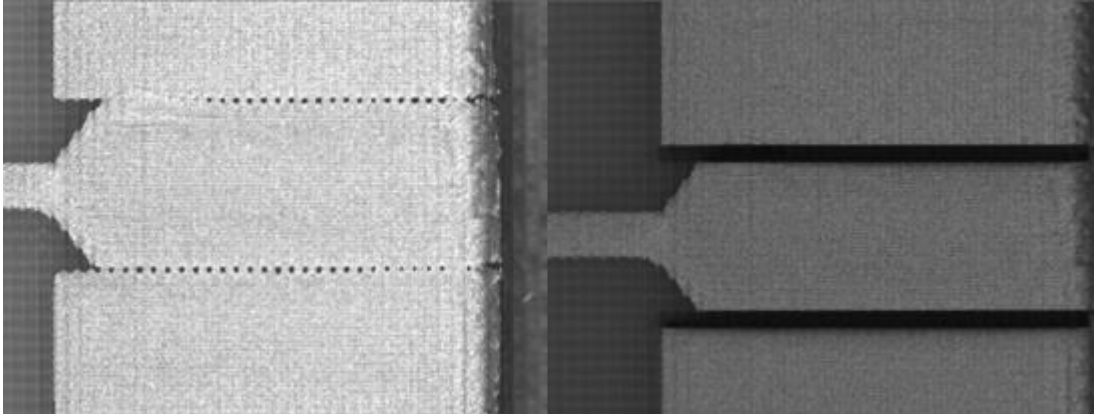
Figure 2.31 – Before and after Lasering of FG57B CPW dispensed on ABS. 3 passes with power of 1 on thin conductor layer.
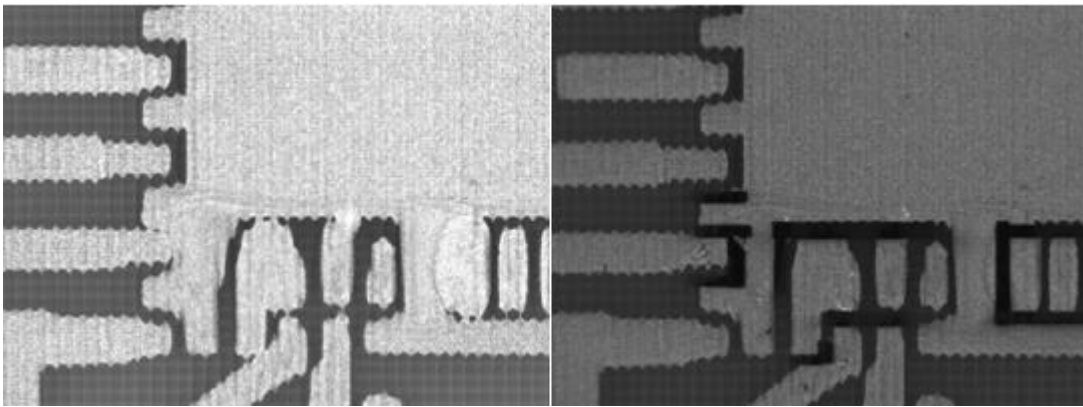
Figure 2.32 – Trimming Conductive Traces to prevent short circuits using the laser.

A via test on 200 µm and 100 µm ABS substrates were then performed to characterize the number of passes to cut though the substrate but not through the bottom conductor with a high voltage level of 1. It is also very important to note that the laser has about a 1 mm range in height where it will cut at all, and ~20 µm range where the laser is highly focused. For this characterization, the height of the laser with respect to the substrate is not changed between passes. This approach was originally investigated but requires a precise knowledge of the depth of cut which changes depending on ABS print quality.
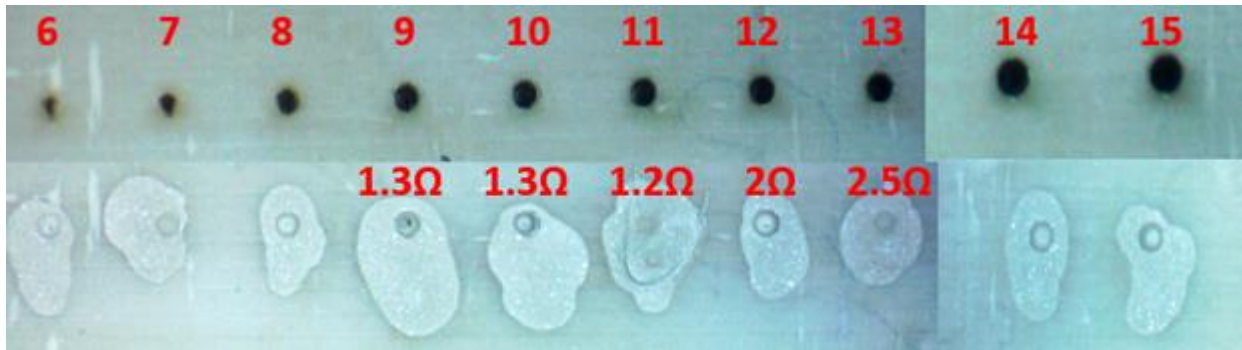
Figure 2.33 – 200 µm diameter via holes on 200 µm ABS substrate with CB028 ground layer underneath and CB028 via filling. The top red number indicates the number of passes and bottom red represent the resistance between the top layer and ground layer 5 mm away from the via. High Voltage level = 1

The preceding pictures show how the vias appear after each cut and demonstrate in the case of CB028 and range of passes that can be utilized to achieve a successful via. A similar test was done on a 100 µm ABS layer on top of a CB028 ground plane. The vias were then probed without filling in smaller cut increments and tested with reference to exposed pads on the ground plane.
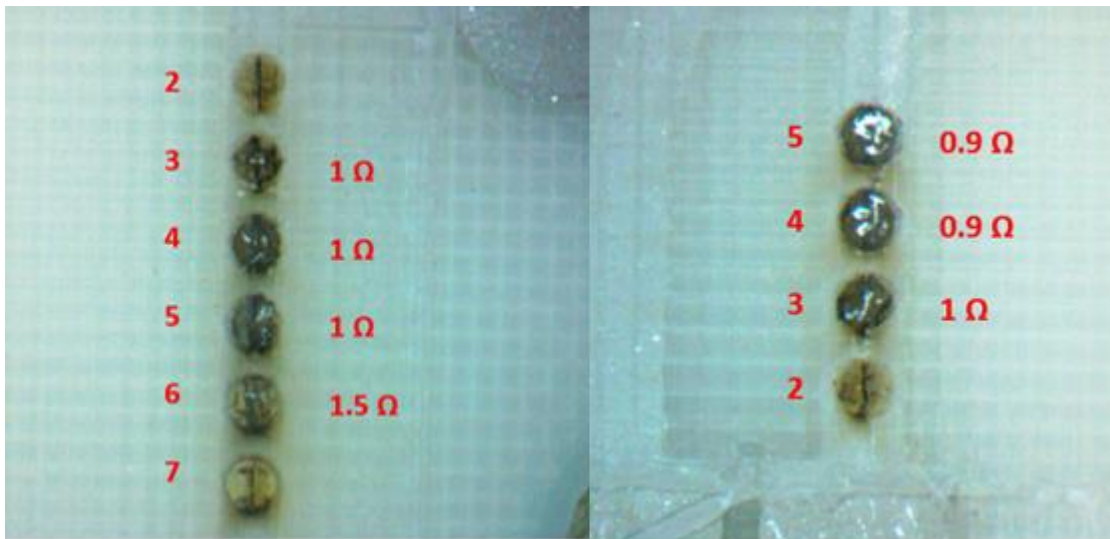
Figure 2.34 – 400 µm diameter via holes on 100 µm ABS substrate with CB028 ground layer underneath and no via filling. The red numbers on the left represent number of passes, and the DC resistance from probing on right. High Voltage level = 1

At this point a good understanding of the number of passes for a 100 µm and 200 µm deep via cut with a reasonably thin ground layer underneath. With the 100 µm a range from 3-5 passes with a focus on the top surface would be expected with a HV level of 1. Similarly, a range between 9 -13 on a 200 µm substrate. It should also be noted that the depth of cut does not vary linearly with number of passes due to the laser focus changing and depth of cut per pass gradually decreasing.

Cavities were then investigated by cutting rectangular cavities with a cut width of about 5 um. In the designs 0402 components with an average height of around 0.5 – 0.6 mm were tested and used for embedding. Due to the deeper cut and the goal to fabricate the entire device in the shortest time possible, the high voltage level was raised to 1.75 to perform the following cuts for the smaller 0402 components, and for a larger square cavity with length of about 7 mm and depth nearing 1 mm, an HV level of 2 was used. The laser was investigated as an alternative to direct print cavities which didn't have the quality needed for small components.
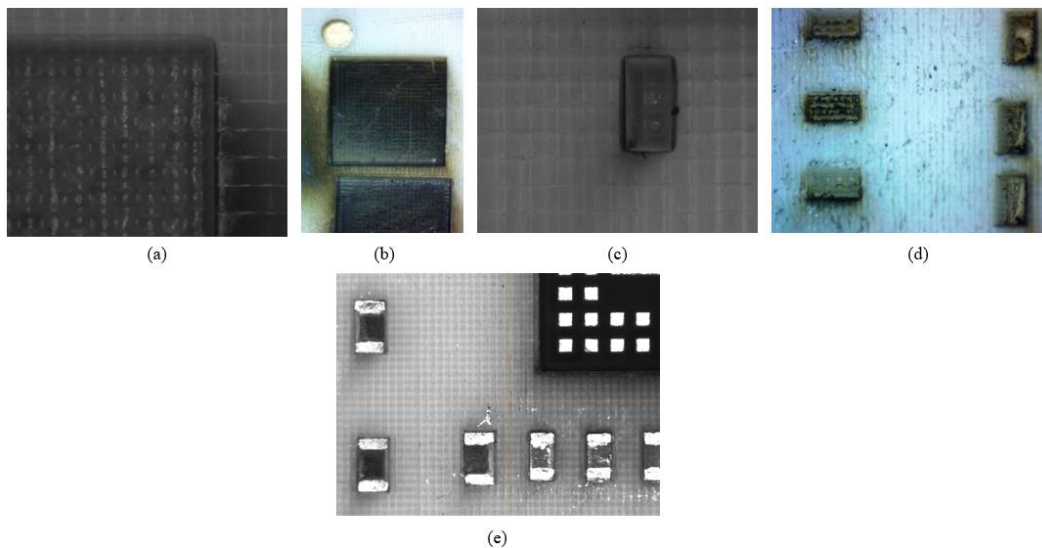
Figure 2.35 – Cavities fabricated using laser. 0402 components with HV power of 1.75 (c)(d)(e) and large 7 mm square chip cavities with HV power of 2 (a)(b). 0402 Depth of 0.6 mm achieved with 13 passes. Depth of .85 mm achieved with 15 passes for the larger 7 mm square IC.

The problem with cavity lasering is the compromise between time and power. Higher power results in a deeper depth of cut but also produces charring of the substrate and a non-uniform bottom surface. With lower powers, very high quality vias with little charring and a controlled depth of cut can be produced at the cost of significant process development.

A print platform with milling capabilities was then obtained and greatly improved the quality of prints and speed of prints. The milling operation allowed for a larger diameter tip to be used for nFD so substrate printing could be achieved much faster. A facing operation was then performed on the over extruded top surface to get a smooth uniform top surface ideal for microdispensing. The milling also allowed for cavities to be printed for ICs as long as holes drilled at each corner were included to fit the chip. Tight tolerances and press fits could then be established to ensure the chip maintained in the proper location through the printing process.

(a)   (b)
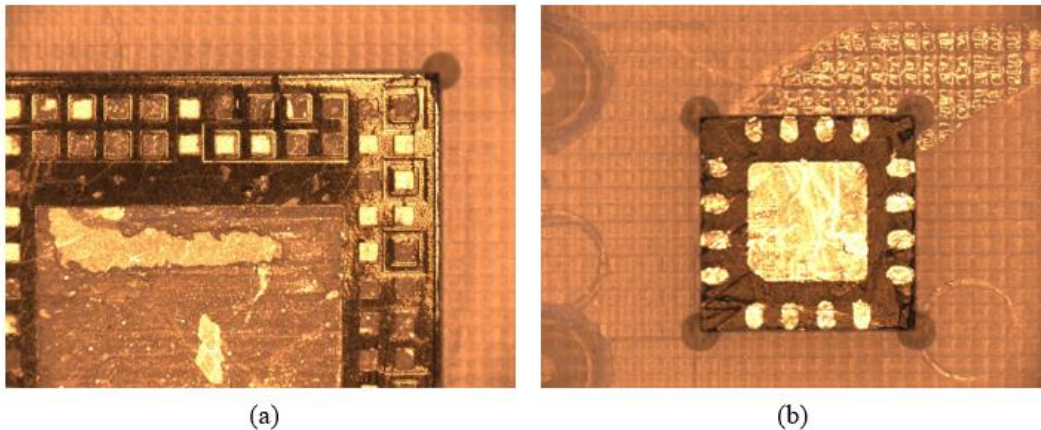
Figure 2.36 – Cavities with nMill for a 7 mm square IC and 3 mm square QFN IC.

The milling tool was also used to compare via fabrication to the laser. The laser benefits from selective etching where the material removal rate of the conducive inks is much slower than that of ABS. This means that many laser passes could be performed to get a via to stop just on the top surface of the conductor without much damage to the traces. The mill benefits from repeatability and speed at the cost of risk of damage to the print of ICs if the improper Z height is

utilized during tool plunges. The laser vias fabricated in this study were used with a HV of 0.5 -1 and results in vias that are difficult to determine if they are the conductive layer but if a lower voltage and more passes are utilized a very high quality via can be fabricated. The mill, on the other hand, is easy to determine if the conductor layer is reached which also makes it more appealing for vias.
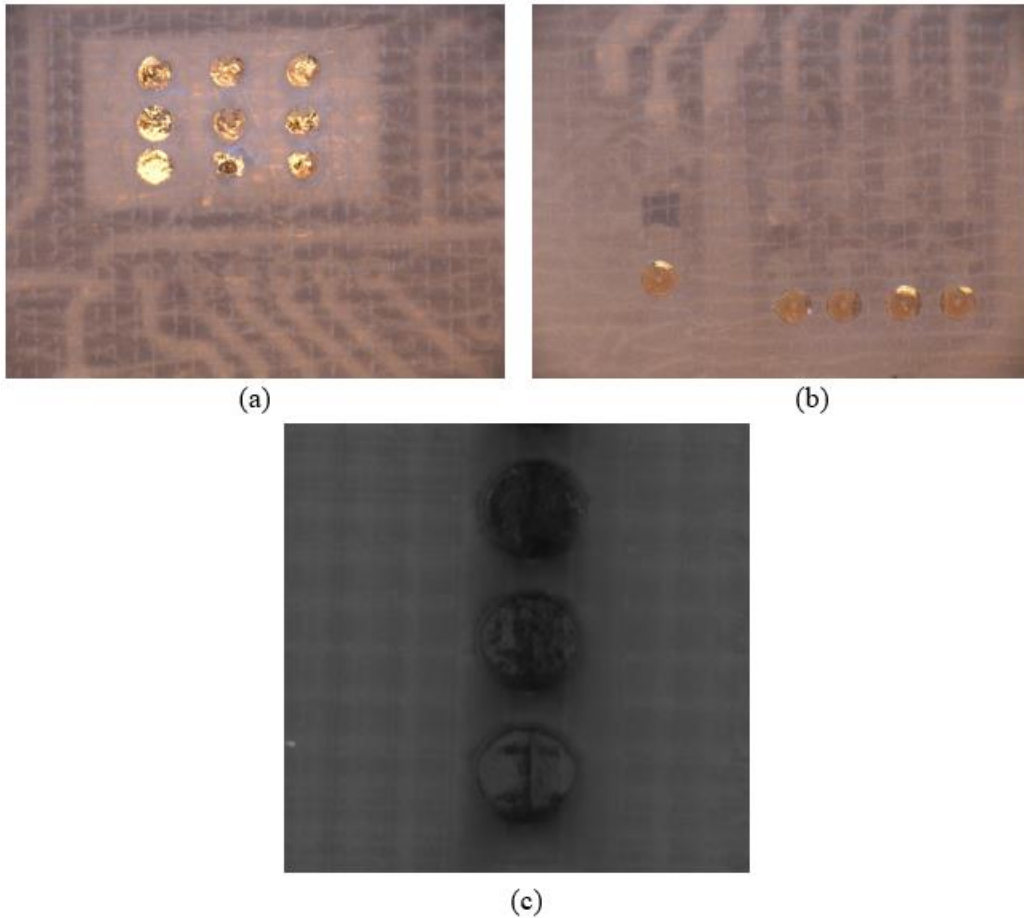
Figure 2.37 - Via Comparison between nMill and Laser.

Chapter 3: Embedding of QFN Packaged High Power Amplifier

In this chapter, a simple embedding process is considered to help evaluate thermal parameters as well as establish familiarity with the printing process beyond material characterization. Specifically, multilayer printing needs to be practiced and potential problems need to be addressed due to the limited amount of IC's that are available later in this project. While multilayer printing seems conceptually simple to perform, nuances in the process appear that want to be avoided or overcame with a developed solution before printing of the final device. Examples of such problems that were experienced include needing to remove sample from bed mid-print in order to allow other users to utilize the printer, reluctance for extruded ABS to stick to a ground layer of CB028 and even the surface of IC's, via hole depth difficult to determine, and micro dispensing inconsistencies all lead to eventual print failures during a printing process. This section serves as a method to get familiar with a small multilayer board and address the thermal concerns that arise when using active devices.

Specifically, a 2.4 GHz high power amplifier was chosen due to its QFN package with dimensions similar to the RF switch used later in this investigation. This allowed for development of the cavity and practice with interconnect printing for this device. The DC power consumption is also similar to the IC used later in its low bias condition which allows for estimation of thermal dissipation and power handling of the ABS substrate.

3.1 Design

The design of the board is not the main purpose of this investigation and for that reason the layout was chosen based on the recommended matching and power distribution network from the IC datasheet to get a device working quickly that could be tested. The below figure represents the final design to be printed without the microstrip or ground layer that will be printed on top to embed the chip.
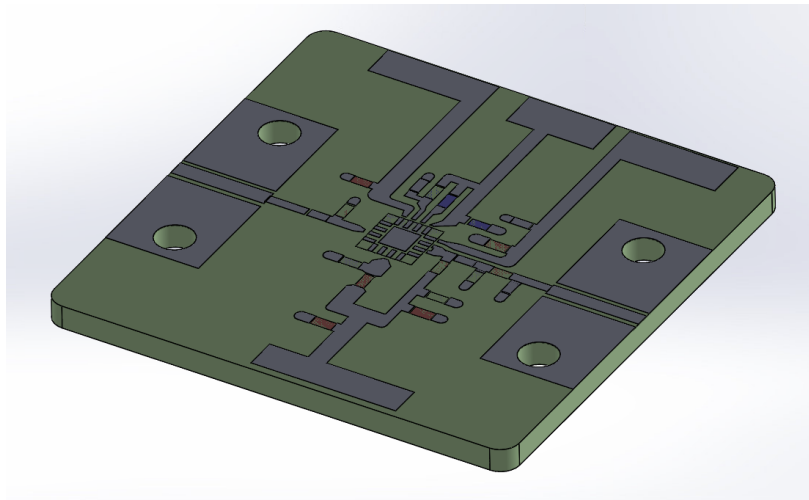
Figure 3.1 – Embedded 4-layer IC layout of QFN PA with lumped components.

The above figure includes 0402 and 0603 to be used for bypass, feed, and matching components. For all devices, we are going to consider a connectorized measurement scheme rather than on-substrate probing. This allows for easier calibration and a more realistic approach for a complete device where connectors are almost always used for connecting modules compared to on-substrate CPW probing which will provide more accurate measurements. Due to the measurement approach a good CPW to microstrip transition needs to be designed.
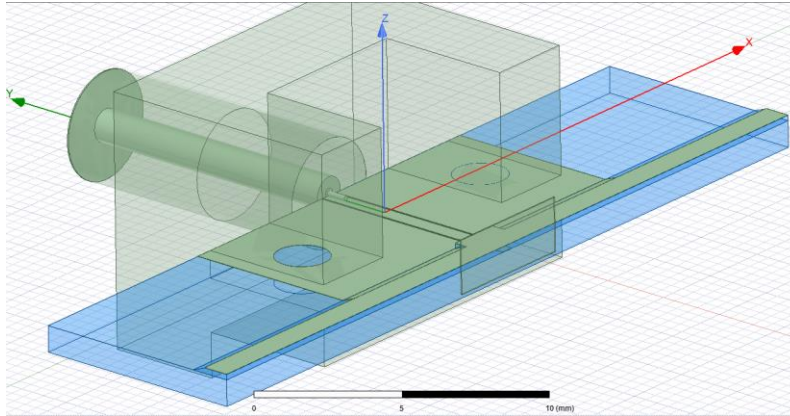
Figure 3.2 – Isometric view of connector to microstrip transition utilizing wave ports at both the microstrip and coax connector ports.
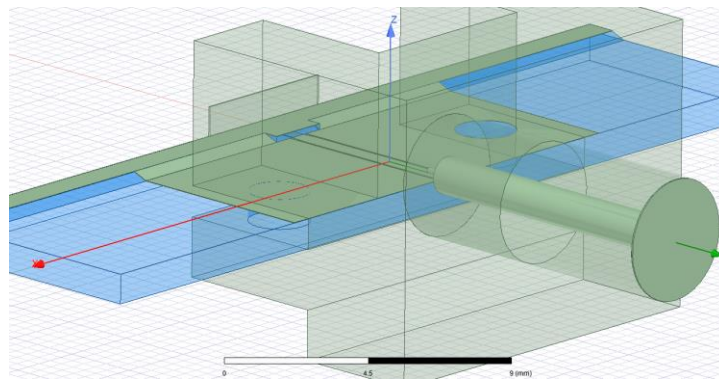
Figure 3.3 – Front view of transition to see the ramp transition needed to elevate the ground from the second to the fourth layer.
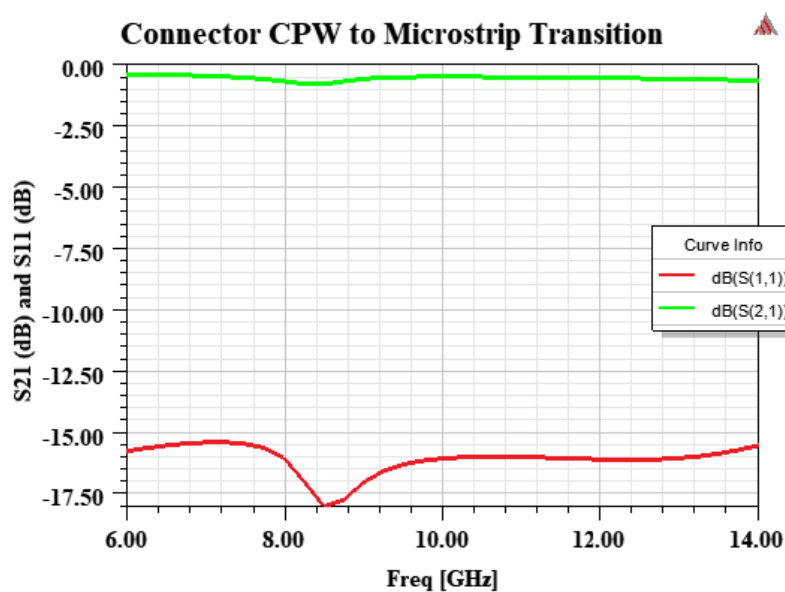
Figure 3.4 – CPW to Microstrip ramp transition. Signal Line width = .622 mm Gap = .066 mm.

The CPW signal line width and gap were optimized to allow for a small transition from the CPW to microstrip width and different connectors were considered to get minimal transition loss and good return loss (around 15 dB) however, a better match good not be developed around 10 GHz without changing the ramp transition geometry. The transition also results in a .541 dB transmission loss at 10 GHz. However, this is considered the ideal design and does not consider how this layer transition is actually manufactured where the ramp is more of a step resulting in a less ideal transition.

3.2 Thermal Considerations

While additive manufacturing lends itself to easily customizable material properties and excelling when a complex design is necessary, it suffers in its thermal management due to material limitations. Due to the inherent nature of the platform used for additive manufacturing within this investigation where a plastic material is melted and extruded through FDM and a semi-viscous paste loaded with conductive flakes is dispensed through a syringe onto a substrate, a disadvantage in the structural and thermal performance is compromised to allow for the mentioned advantages. The platform discussed in this paper decided the range of materials that could be utilized and it was found to be necessary to utilize materials where the capabilities were known to ensure completion within the given time constraint. ABS was used as the substrate which has a low thermal conductivity relative to other commonly used substrates and has a low glass transition temperature (T_g) which may cause device failure due to cavity or substrate deformation and low structural stability when approached. This is the primary reason that thermal considerations need to be investigated when using this substrate with active devices. Aside from the substrate, the conductive paste also leads to a large limitation which involves heat spreading. In conventional circuit boards, copper is typically used as the conductive material and compared to the ink or paste

within this paper, not only has an electrical conductivity around 10-20x the paste/ink but also has a thermal conductivity around 40x greater. This results in a temperature distribution that is primarily vertical in nature through the layer stack up and contains very little horizontal spreading of heat.

Rather than do a simple analysis for a specific geometry, a sensitivity to different thermal parameters was investigated in order to get an idea of what needs to be optimized to provide the best thermal performance. Integration of the device is dependent upon several factors regarding the layer stack up. The alternative to the model shown below is commonly seen with the ground plane printed below the signal traces and around the same height as the IC when showing the improvement to traditional molded packages where dies have printed interconnects and not wire bonds. This was less convenient in the case of my structure due to the fact that later in this investigation the antenna feed and matching was improved by utilizing an aperture coupled stack up where the ground layer is between the signal traces and patch antenna.
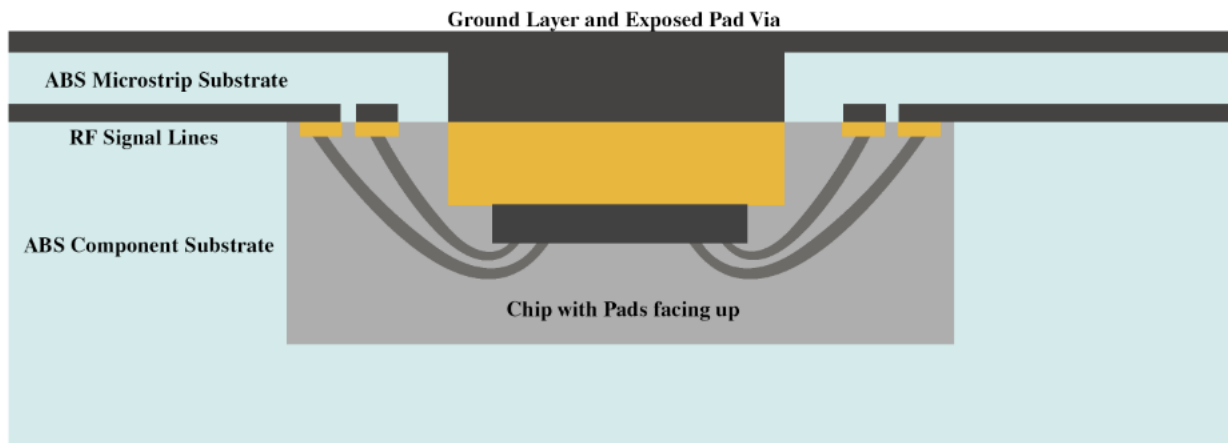
Figure 3.5 – Typical additive manufactured layer stack-up investigated within this study.
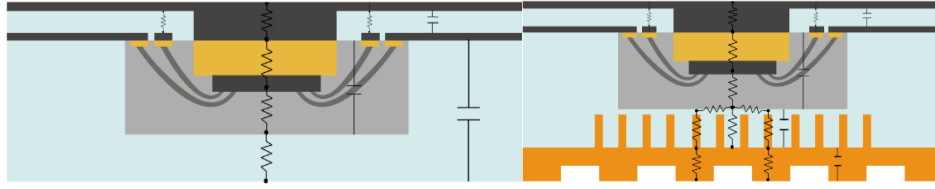
Figure 3.6 –Stack-up with symbols representing thermal resistance and capacitance.

A brief thermal background about the main method heat dissipation is shown to allow better understanding of how some of the mentioned parameters are arrived at. The only way this device is exchanging heat with the surroundings is through convection. Through the concept of energy conservation, heat generated must be dissipated at the same rate to prevent continuous temperature increase. The amount of heat that exchanged is dependent on the surface temperature, the surface area, and the heat transfer coefficient (h). The heat transfer coefficient is a constant that is used in calculating the amount of convection between a surface and a surrounding fluid.

$$Q\ (W) = hA(T_s - T_\infty)$$

Q is the amount of heat transferred, A is the surface area of the surface in contact with the fluid, T_s is the surface temperature, and T_∞ is the surrounding ambient temperature. Considering improving heat dissipation, effective surface area must be increased (area where $T = T_s$, which is limited by heat spreading), the convection coefficient must be increased, or a larger temperature difference (leads to higher h) needs to be developed.

In order to calculate the heat transfer coefficient several other fluid parameters need to be addressed. The Grashof number (Gr) approximates the ratio of the buoyancy to viscous force acting on a fluid and is primarily used in natural convection calculations to take into account the change in density of the fluid.

$$Gr = \frac{g\beta(T_s - T_\infty)L^3}{v^2}$$

In the above equation, g is the gravitational acceleration, β is the coefficient of thermal expansion for the fluid (air), and ν is the kinematic viscosity. The second dimensionless number is the Prandtl number (Pr) and is the ratio of momentum diffusivity to thermal diffusivity and is seen below,

$$\text{Pr} = \frac{\nu}{\alpha} = \frac{c_p \mu}{k}$$

where α is the thermal diffusivity, c_p is the specific heat, k is the thermal conductivity, and μ is the dynamic viscosity. It is important to note that the parameters used in the above equations should be of the surrounding fluid and not of the solid surface.

For free convection the Rayleigh number (Ra) is defined as,

$$Ra = Gr\ Pr$$

Finally, the Nusselt number (Nu), is the ratio of convective to conductive heat transfer across a given length or surface and in the case of free or natural convection the Nusselt number is based on empirical calculation for different flow and structure orientations. The goal is to have conditions where convection due to air movement is larger than conduction through air molecules in close proximity (due to conductivity air being very small).

For a vertical plate [27],

$$Nu = 0.68 + \frac{0.67\ Ra^{\frac{1}{4}}}{\left[1 + \left(\frac{0.492}{Pr}\right)^{\frac{9}{16}}\right]^{\frac{4}{9}}}$$

for a horizontal plate [28],

$$Nu = 0.54 + Ra^{\frac{1}{4}}$$

for a bottom facing plate [29],

$$Nu = \frac{0.619 \, Ra^{\frac{1}{5}}}{\left[1 + \left(\frac{0.520}{Pr}\right)^{\frac{3}{5}}\right]^{\frac{1}{3}}}$$

Then the heat transfer coefficient, h, is found from,

$$h = \frac{Nu \, k}{L}$$

Table 3.1 – Thermal properties of air [30] [31]

Temperature (C)	β, Coefficient of Thermal Expansion (K^-1)	ν, Kinematic Viscosity (m^2/s)	c_p, Specific Heat (Constant Pressure) (J/kg K)	μ, Dynamic Viscosity (kg/m s)	k, Thermal Conductivity (W/ m K)
30	.00332	1.568 E-5	1004.9	1.846 E-5	.02624
80	.00285	2.056 E-5	1008.2	2.075 E-5	.03003
100	.00270	2.317 E-5	1010.6	2.181 E-5	.03186
120	.00251	2.591 E-5	1013.5	2.286 E-5	.03365
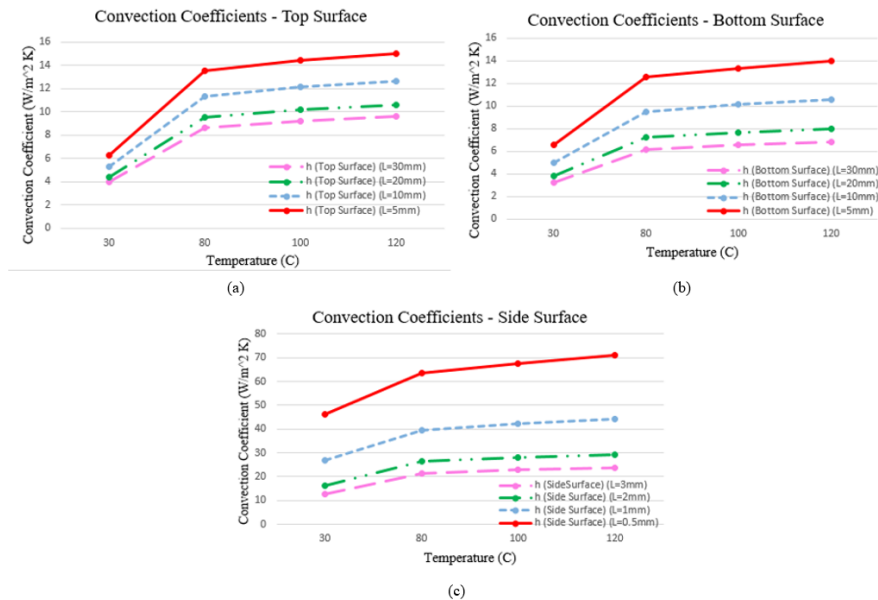
Figure 3.7 – Convection coefficients over various lengths considering the heat is concentrated in a small area and not over the entire device.

The above figure serves to offer a guideline for different convection coefficients at different surface temperatures and different lengths. The length considered changes the Grashof number which contributes to the Nusselt number, and the length in the heat convection coefficient calculation. Clearly from convection coefficient equation, the length changes the coefficient significantly, however, the total heat transfer considers the cross sectional area in contact with the fluid.

The coefficients calculated above are then established as the boundary condition in ANSYS Mechanical steady state thermal simulations. However, before simulation was considered, the parameters that aren't concrete and lend themselves to be changed are addressed. The 4 layer PA device has parameters that need to be assigned to each layer which include: thickness, area, density, thermal conductivity, and specific heat. For ABS the material properties are listed in Table 1.1 and for microdispensing an approximate range based on other data is listed in Table _. The base substrate layer can have a thickness ranging from 1 mm to 1.5 mm depending on the size of the large bypass capacitor, and an area fixed at 25 mm x 25 mm. The second signal layer can be approximated as a conductive layer with thickness between 17 and 34 µm and an area fixed at 25 mm x 25 mm. The microstrip substrate is fixed at 200 µm thickness and area at 18 mm x 15 mm. The final ground layer has a height from 17-34 µm and area around 18 mm x 15 mm. The only material properties that are swept are the conductive ink conductivity and density. Apart from changing these parameters, if the device cannot handle the heat then a heat sink must be considered. One of the easiest ways to determine if a heat sink is needed is to calculate the range in thermal resistances and the power dissipation to determine if even at steady state the device will be safe

$$P_{in} = -7 \, dBm \quad Gain = 29 \, dB \quad P_{out} = 22 \, dBm$$
$$P_{DC} = 240 \, mA * 3.3 \, V = .792 \, W$$
$$P_{Diss} = P_{DC} + P_{in} - P_{out} = .634 \, W$$

$$Maximum\ Device\ Thermal\ Resistance = \frac{(T_j - T_A)}{P_{Diss}}$$

$$Maximum\ Thermal\ Resistance = \frac{(150\ C - 28\ C)}{.634\ W} = 192\ C/W$$

Table 3.2 – Thermal resistance of amplifier test fixture.

	Thickness	Area	Thermal Conductivity (W/m-K)
Layer 1 -Base	1.5 mm	25 mm x 25 mm	.172
Layer 2 – Signal	17 µm -34 µm	20 mm x 20 mm	.5 - .9
Layer 3 – Microstrip Substrate	200 µm	18 mm x 15 mm	.172
Layer 4 - Ground	17 µm – 34 µm	18 mm x 15 mm	.5 - .9

Table 3.3 – Additional thermal properties for simulation

Material	Density (kg/m^3)	Thermal Conductivity (W/m-K)	Specific Heat (J/kg-K)
Aluminum [32]	2700	210	900
Copper [33]	9300	328	1250
FR-4 [34]	1850	0.8	1150
IC Mold	1800	0.7	1400
Ink	1000	0.7	1200

3.3 Fabrication

In this section, the build up to the final design and measurement is discussed. While the initial microdispensing and FDM substrate printing were shown initially, the critical parts are the laser machined cavities, microdispensed interconnects and the vias to connect the signal layer to the ground layer.
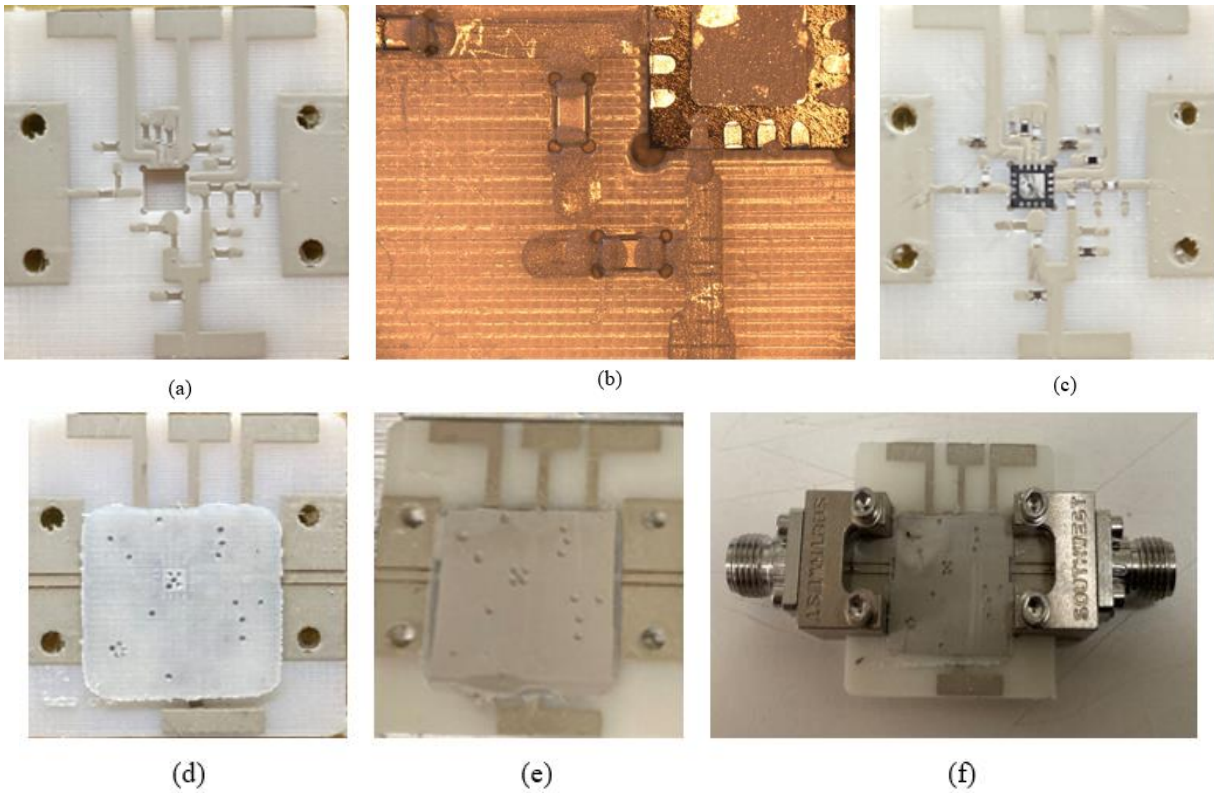
Figure 3.8 – Embedded PA Fabricated Device. (a) Substrate with microdispensing on top followed by milling of the cavities, (b) Placed components and ICs with interconnects on printer camera, (c) Top view of all placed components. The ABS microstrip layer with vias are printed on top to embed the chip (d), ground layer printed on top (e), connectorized device ready for measurement.
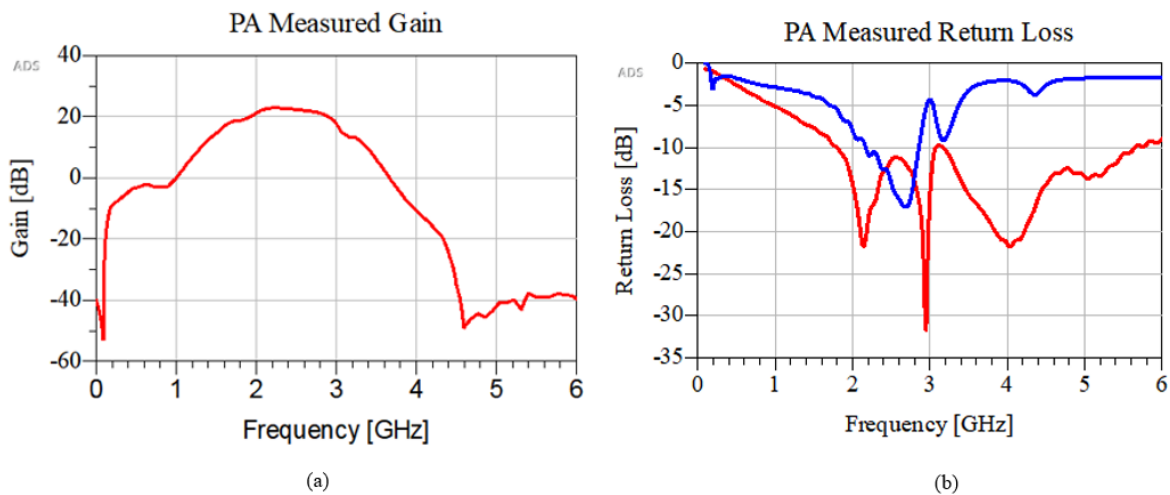
Figure 3.9 – PA Measured Results. (a) Measured small signal gain on ENA, (b) Measured input and output return loss of QFN PA.

The above measured S-parameters represent the small signal characteristics measured on an ENA. When attempting to measure on a different bench with power sweep capabilities, device damage did occur presumably to interconnects and no measurement could be pulled. This is also a concern for the thermal results as the low current draw for low input power did not result in significant temperature rise. Comparing to the PA datasheet and referring to the small signal gain S-parameters, the gain is about 7 dB lower then expected which could be due to conductive losses and resistive interconnects. The layer transition also appears to be a problem for repeatability and could contribute to additional loss by leading to additional signal reflections from the discontinuity. This part of the process commonly requiring manual modifications.

Figure 3.10 – Thermal measurements during small signal gain.

Chapter 4: Packaging of Active Beamforming IC

Patch antennas offer a low-profile design that are typically cheap, small, and easy to fabricate with a variety of different materials. The patches are usually arranged into an array for improved gain performance and the ability to steer the primary beam. Patch antennas usually have a small bandwidth around 5 % which makes them difficult to use over a wide frequency range. Attempts to develop wideband antennas have been explored and wideband results have been shown with an aperture coupled patch antenna [35]. In an aperture coupled patch antenna, the antenna feed line is separated from the radiating patch element by a ground plane with a slot in it. The goal is to optimize the microstrip and antenna substrate thicknesses, aperture width and length, and radiating element dimensions. While previous studies have utilized a phase shifter and shift register to change the phase going to each element, this paper utilizes a beamforming chip from Analog Devices.

4.1 IC Overview and Package Approach

The ADAR1000 was chosen due to its ability to digitally control the phasing and attenuation to each element but also to add gain to the receive and transmit channel paths using an LNA and driver amplifier, respectively. The 4 channel I/O allows for reduction of size and potential RF vias; however, this chip is designed to be implemented into a system with external power amplifiers and LNA's as well as RF switches. This investigation only considers the addition of an RF switch for each channel and based on the frequency range, the ADRF5019 and HMC1118 switches were compared.
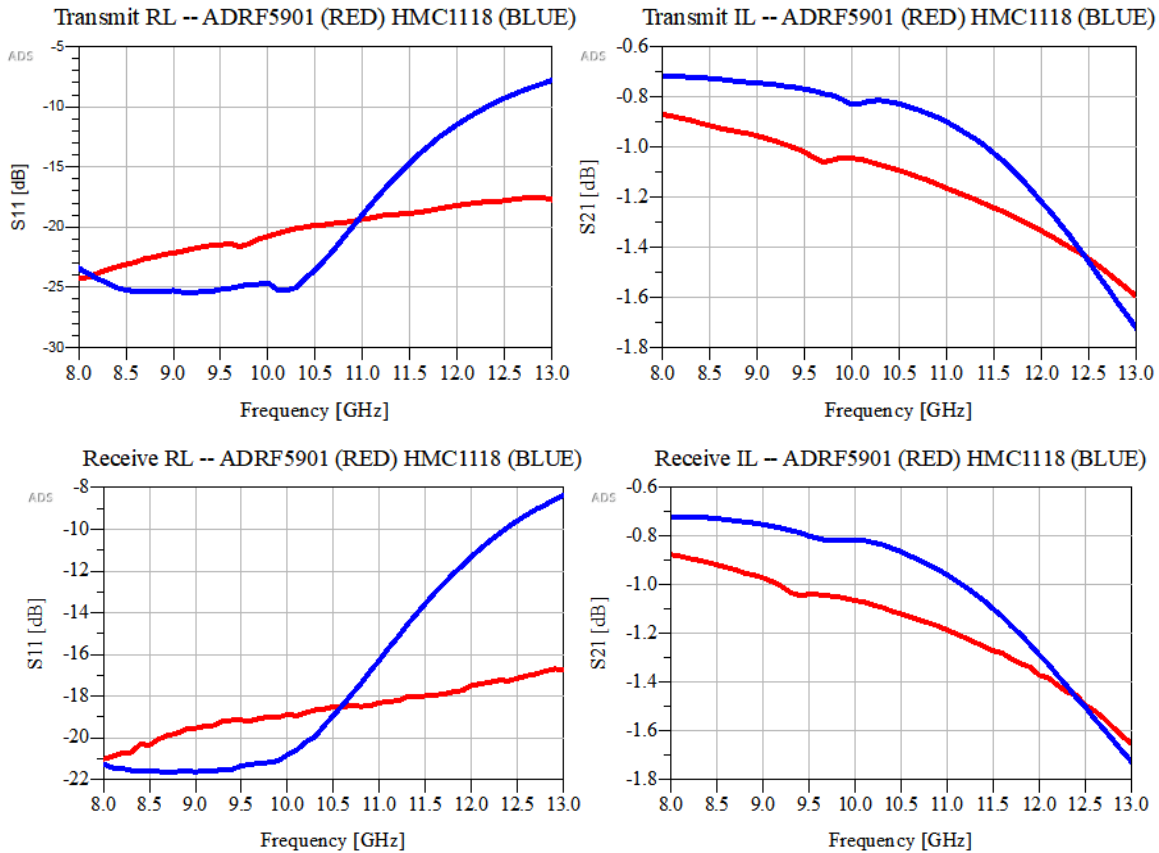
Figure 4.1 – RF Switch comparison between ADRF5019 and HMC1118

It can be seen from the above figures that the ADRF5019 has worse insertion loss by around 0.2 dB but exhibits better wideband return loss. The ability for the switch to have better return loss from 11 GHz and higher is desirable and the main reason for moving forward with that particular RF switch. The following figure is a functional block diagram of the device without the digital control pads and serves to provide a rough RF block diagram for all 4 channels.
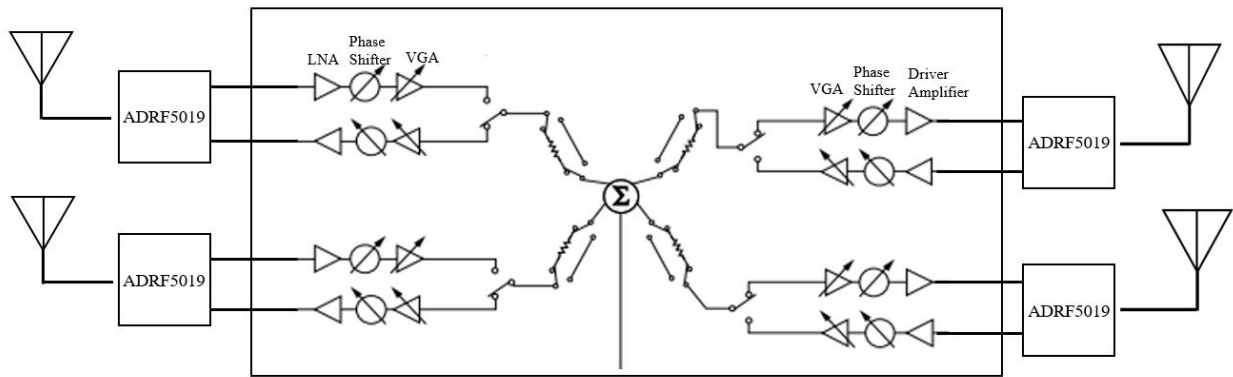
Figure 4.2 – Functional block diagram of the ADAR1000 and RF switches.

As seen in the block diagram, there a single RF input or output that gets fed into a power divider/combiner to separate into 4 different channels. Each split path has its own attenuator, receive path input, and transmit path output making up a total of 4 transmit channels and 4 receive channels. Each receive channel consists of an LNA, a phase shifter, and a variable gain amplifier (VGA) before entering into the combiner and each transmit channel consists of a variable gain amplifier, a phase shifter, and a driver amplifier. The phase shifter, VGA, and attenuator are all utilized and controlled via digital SPI inputs to allow for the IC to be used for beam-steering. The device package is a 7mm x 7mm LGA with 88 terminals. The main concern and difficulty when printing with this chip comes with the 4 wire SPI. The SPI digital control pads are located on the inside ring of pads and the surrounding outer pins are all grounded for this application. While its convenient to simply ground the outer pads, the inner pads need to be brought off the board and the package layout designed in this work requires 4 on chip vias that temporarily transfers the SPI trace to a different layer. This can be seen in Figure 4.4 where an intermediary layer is needed to properly route the SPI traces.
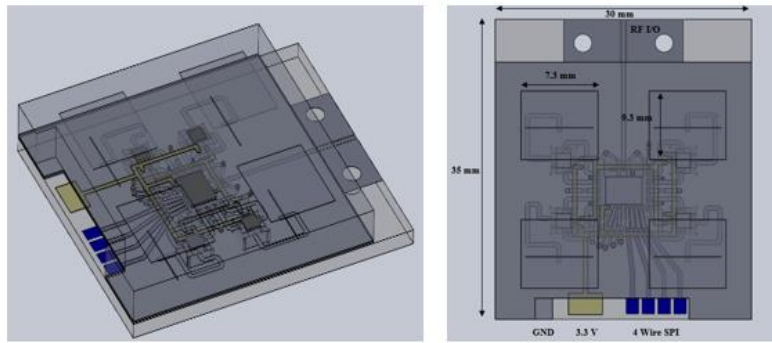
(a)   (b)
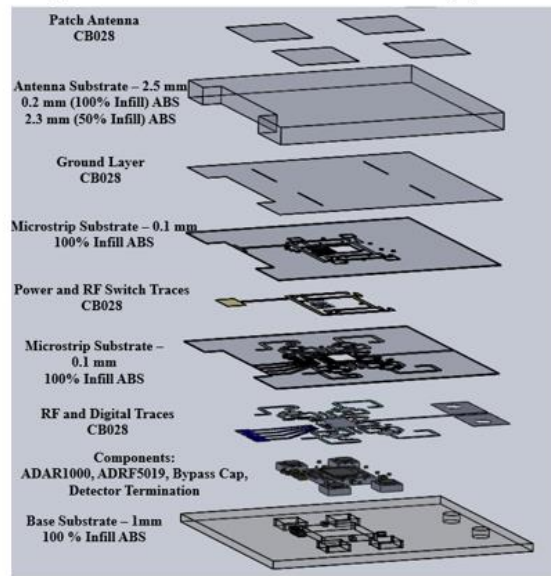
(c)

Figure 4.3 – Initial Design of Embedded ADAR1000 IC.

Figure 4.4 – On-chip via and temporary layer transition for 4-wire SPI. Critical fabrication point where issues were expected to be encountered.

The above figures portray the stack up for the fabrication process of the initial design. The initial design involved embedding the ADAR1000 chip and fabricating vias on an empty part of the IC package to get the SPI traces over the outer pads. Since 0.2 mm vias have been fabricated before, it appeared to be feasible. However, considering the 1st fabrication effort seen later this, had to be readdressed due to reliability and the inability to confirm a connected via.

4.2 Antenna Sub-Array Design

A single element aperture coupled patch antenna was initially developed to understand how the coupling and radiation pattern were affected by the slot position and size. Tuning was primarily done by observing the how different parameters moved the return loss on the smith chart. While a microstrip fed patch antenna would be easier and more reliable to allow for interconnect monitoring, the aperture coupled patch antenna allows for an array to be developed by keeping the elements about a half-wavelength from each other. The single element was simulated to have about 5 dB gain and matched from about 9 – 12 GHz.
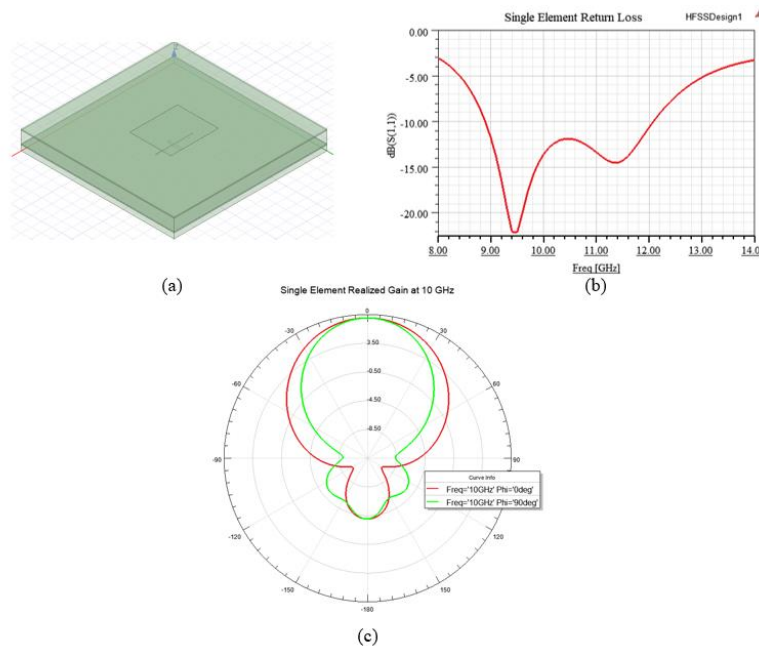
Figure 4.5 –Single element aperture coupled antenna model and performance

While a single element should be initially investigated, in order to become familiar with the printing process for the final device and not risk damage to the limited active devices, a 4-element aperture couple patch antenna array with a 1:4 antenna feed distribution network to provide 50-ohm lines underneath the slots was designed, fabricated, and measured.
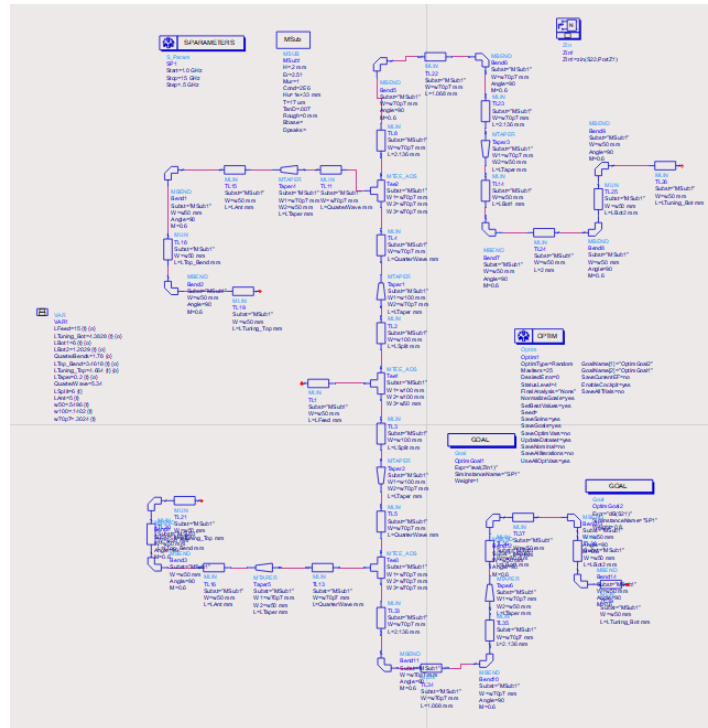
Figure 4.6 – ADS Schematic of 1:4 antenna feed.

(a)   (b)
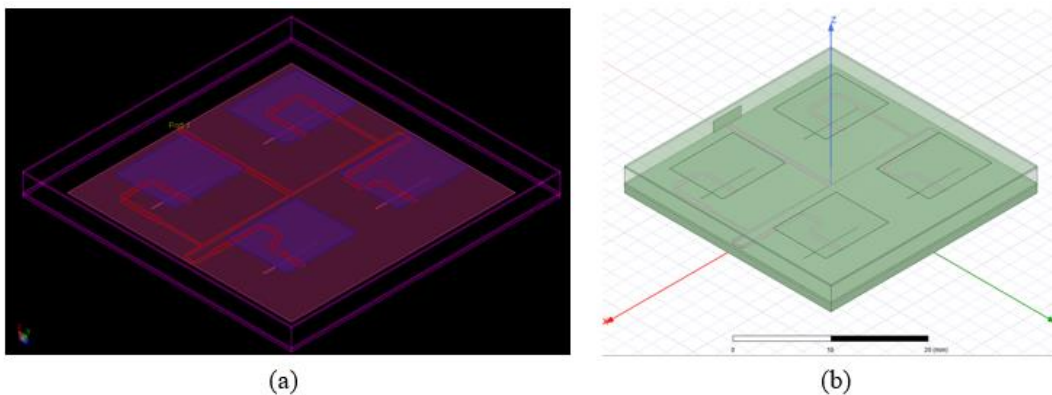
Figure 4.7 – Design of 1:4 antenna feed using Momentum and HFSS.

ADS Aperture Antenna Feed RL

Aperture Antenna 1:4 Feed

m5
freq=8.396GHz
dB(S(1,1))=-10.239

m6
freq=12.11GHz
dB(S(1,1))=-10.280

(a)   (b)
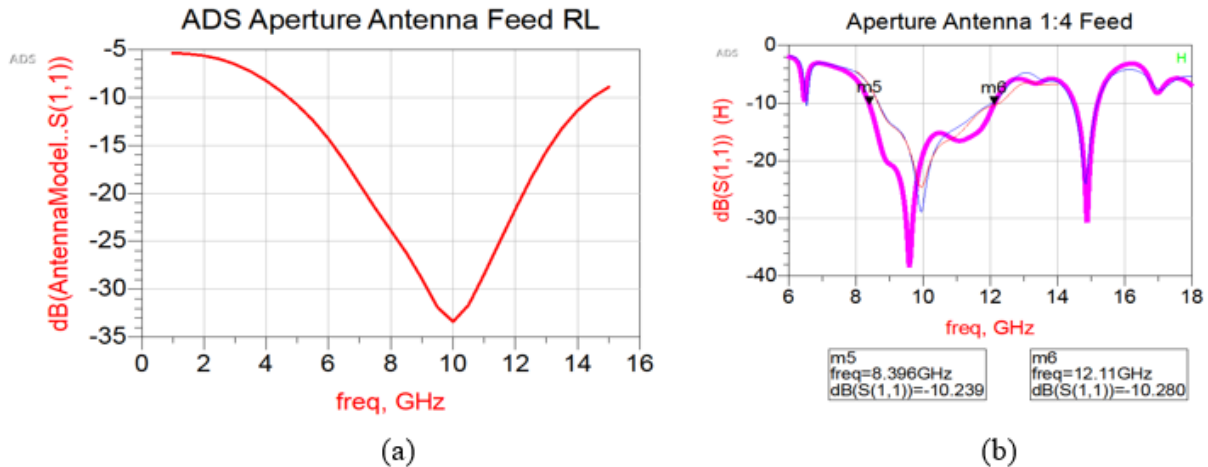
Figure 4.8 – Return loss of 1:4 feed network from Schematic and Momentum.

The above figures represent the simulated performance from HFSS and Momentum which was sufficient for this test print procedure. Fabrication was started to investigate how to print the antenna slots and how the 200 µm 100% infill ABS substrate printed above the 2 mm 50% infill ABS was going to provide a smooth enough top surface for the patch antennas to be printed on. The slots were initially attempted with the laser, but contrary to vias where the reduced etching rate on the conductive paste was beneficial, the number of passes needed to cut the slot resulted in a large heat effected region and an inability to visually verify if the slot had been fabricated. The new printer received throughout the work in this thesis was fitted with an end mill tool that was utilized in both printed arrays due to its accuracy, repeatability, and ability to verify the conductive paste had been removed.

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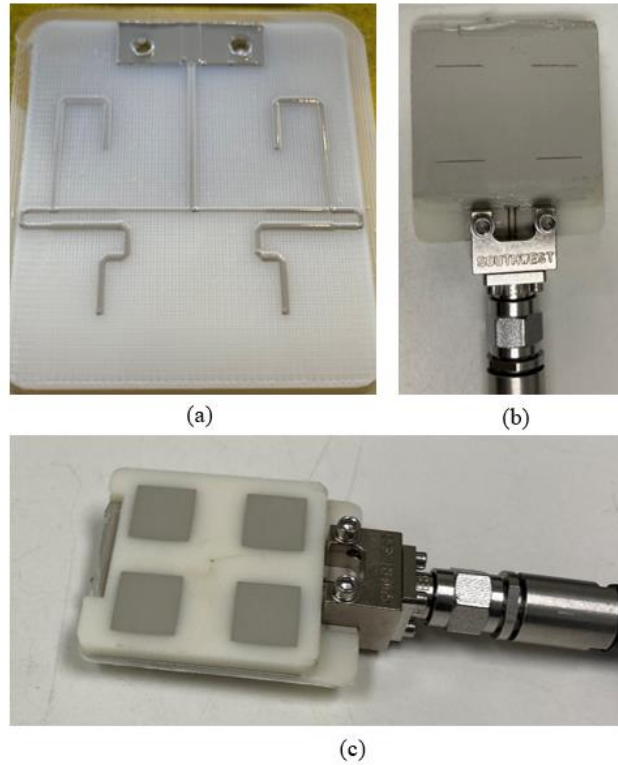
Figure 4.9 –Feed network for antenna printed on ABS with CB028.
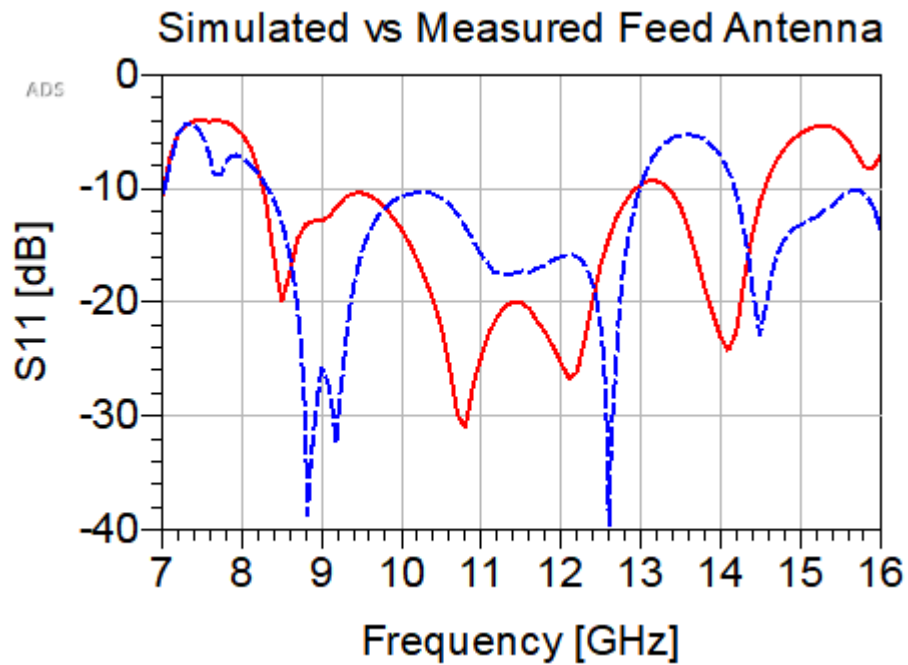
Figure 4.10 – 4 Element, single feed antenna simulated (blue) vs measured results (red).

The match between the simulated and measured wasn't perfect but similar trends were seen in both. The 10 dB return loss bandwidth was similar, however, the lower return loss at 9 and 12.5 GHz could be due to poor coupling efficiency between the slots and antenna due to slight delamination of the printed antenna substrate from bad adhesion during printing.
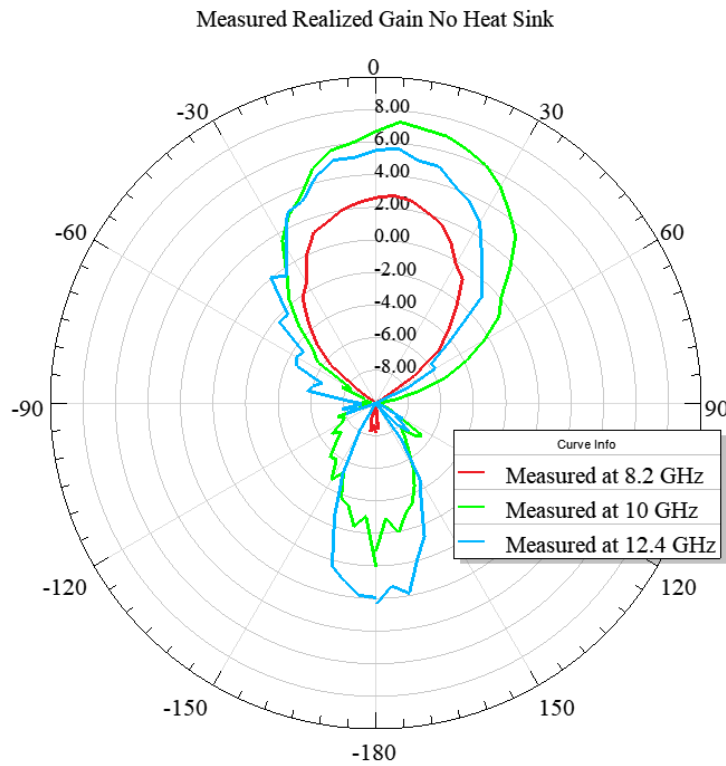
Figure 4.11 – Radiation Pattern measured in anechoic chamber with no heat sink on device.

The anechoic chamber was utilized to take measurements for the antenna as seen in Figure 4.11. The high front to back radiation levels also prove to be a consistent problem and is to be expected because no effort was done to prevent back radiation in order to reduce fabrication complexity.
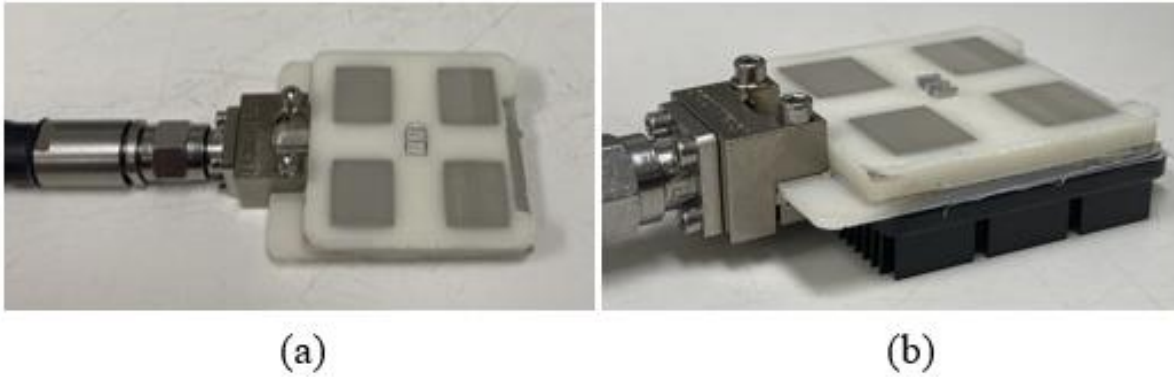
Figure 4.12 – 1:4 Antenna Feed printed with heat sink embedded in top substrate.
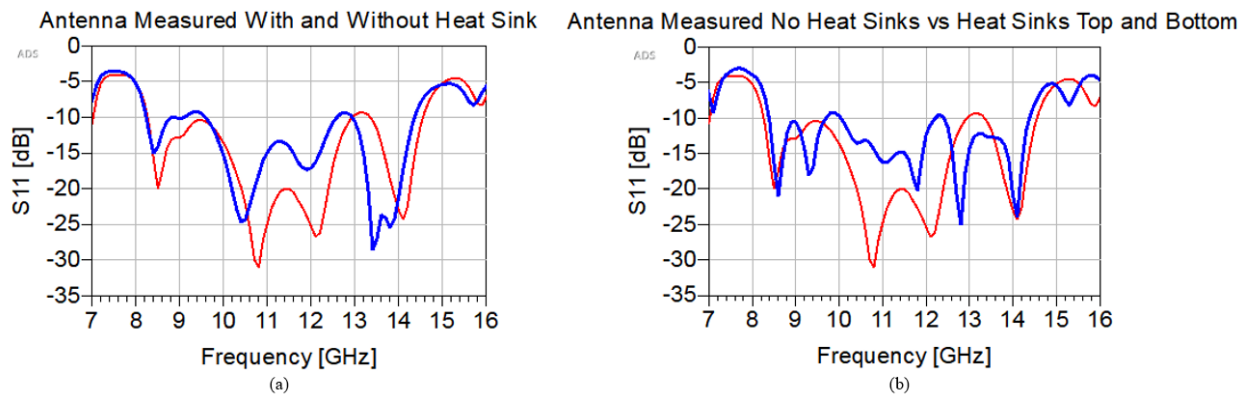
Figure 4.13 – Return Loss of antenna with different heat sink configurations. No heat sink (red).

In Figure 4.12, the addition of the heat sinks was investigated to see how the radiation pattern was affected. Figure 4.13 shows the return loss to be sufficient but the radiation patterns in Figure 4.14 paint a different picture. The addition of the bottom heat sink greatly reduces the 10 GHz antenna gain most likely due to changing of the slot impedance from the large aluminum heat sink, although, the 11 GHz gain was improved due to the same affect.
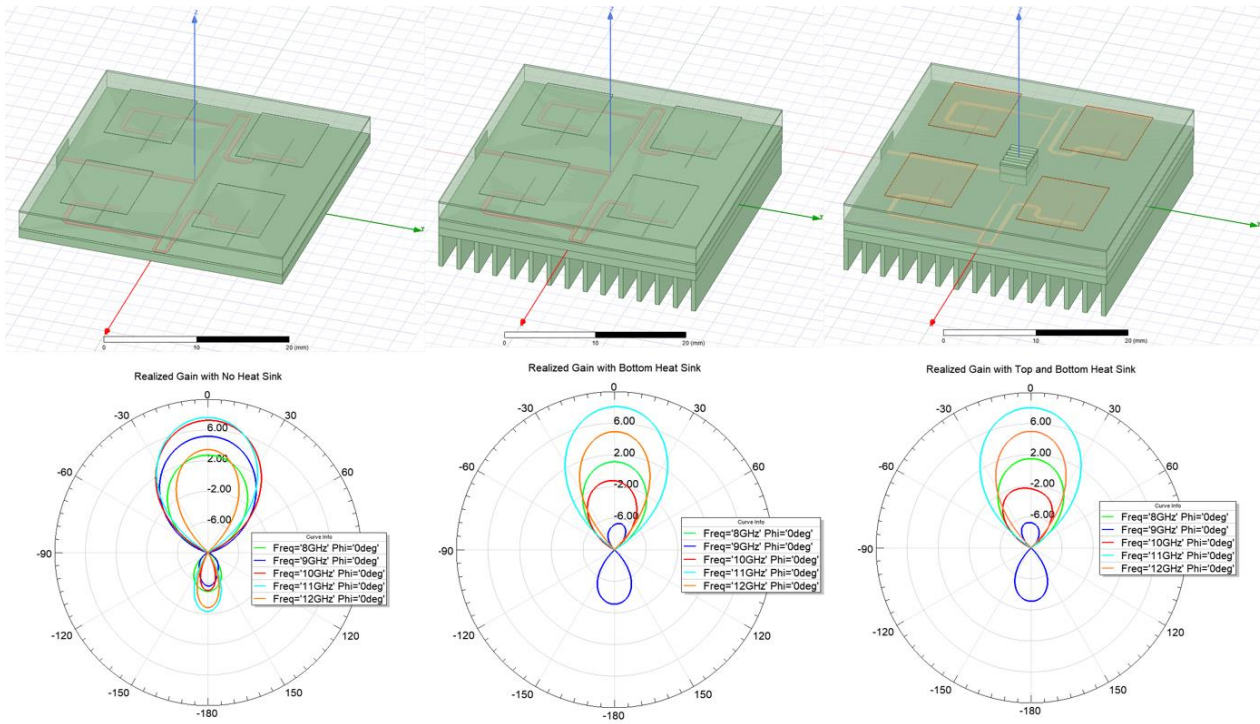
Figure 4.14 – Simulated radiation patterns with different aluminum heat seat configurations

The most important parameters with the above results are the change in impedance and radiation behavior when the heat sinks are added.
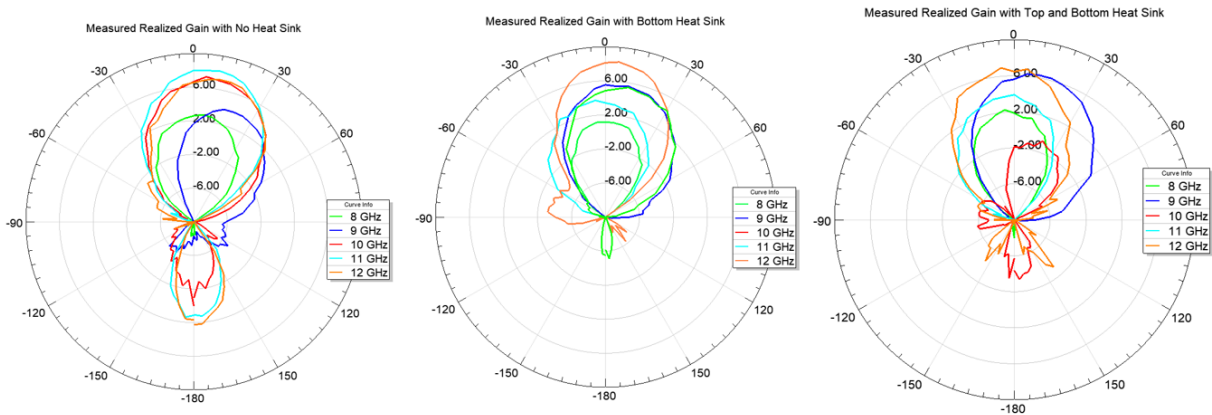
Figure 4.15 – Measured results of the antenna in those respective configurations. Colors correspond to each other across all plots.

The above plots attempt to do a preliminary simulation to measurement comparison of the radiation parameters of an aperture coupled 1:4 feed patch antenna. Moving on from that, the phase

shift needed to direct the beam in the correct dimensions is investigated to determine a phase requirement for the final device.
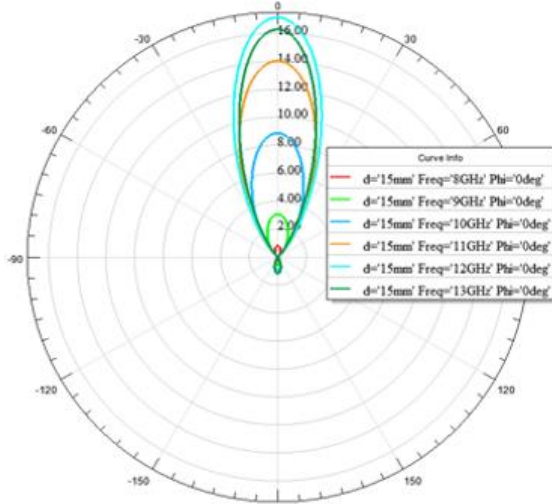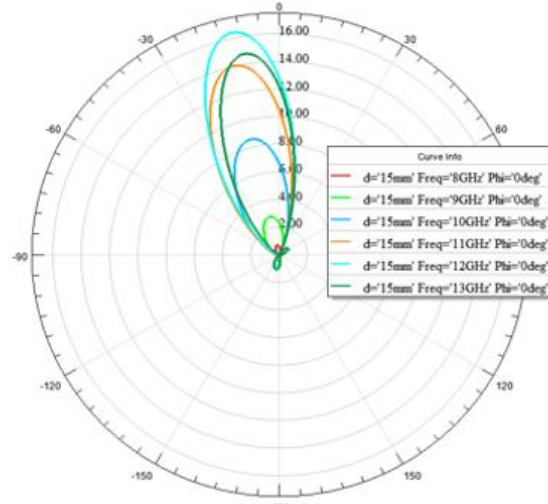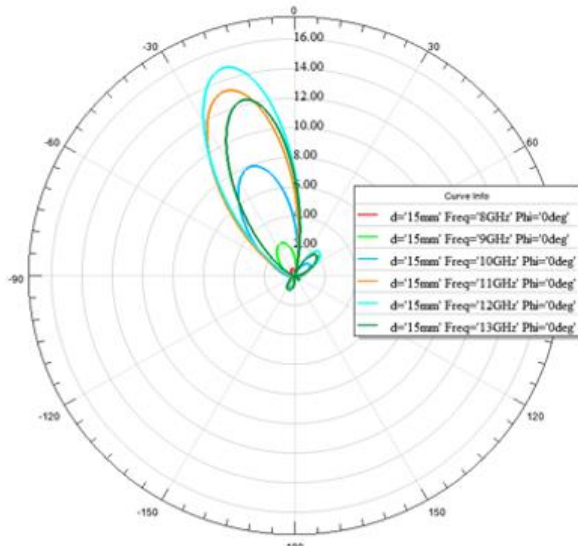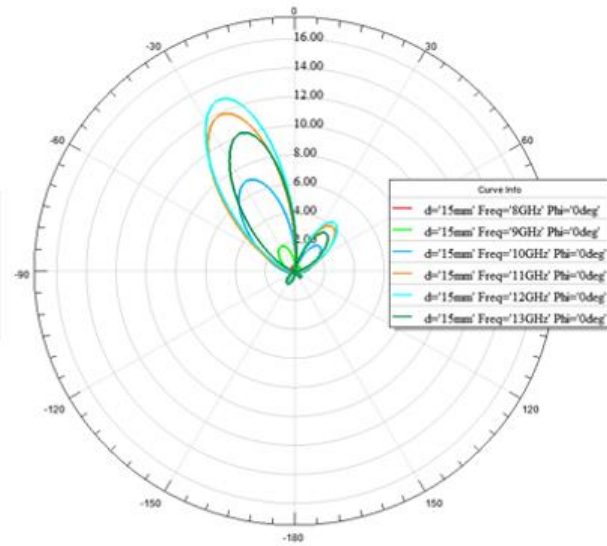
Figure 4.16 – Simulated phase shift and resulting array pattern.

Table 4.1 Element Phasing and Combined Beam Direction

2 Element Relative Phasing	Beam Steering Angle
0	0
60	12
100	20
130	25
160	30

Based on the results from Figure 4.16 and Table 4.1, the targeted phased shift for each element is found for a specified beam position. Side lobes start to get significant with respect to main beam levels as the relative phasing increases. The beam as seen in Figure 4.16, is only able to get to approximately 30 degrees before performance starts to degrade to those levels. This is simulated within HFSS and as seen later the results from the active array differ.
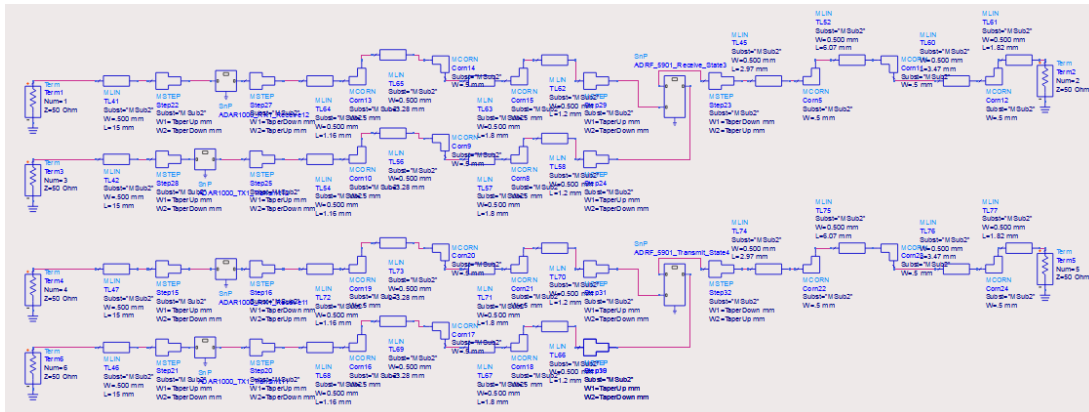
Figure 4.17 – Feedline schematic of RFIO to antenna for transmission line loss estimation.
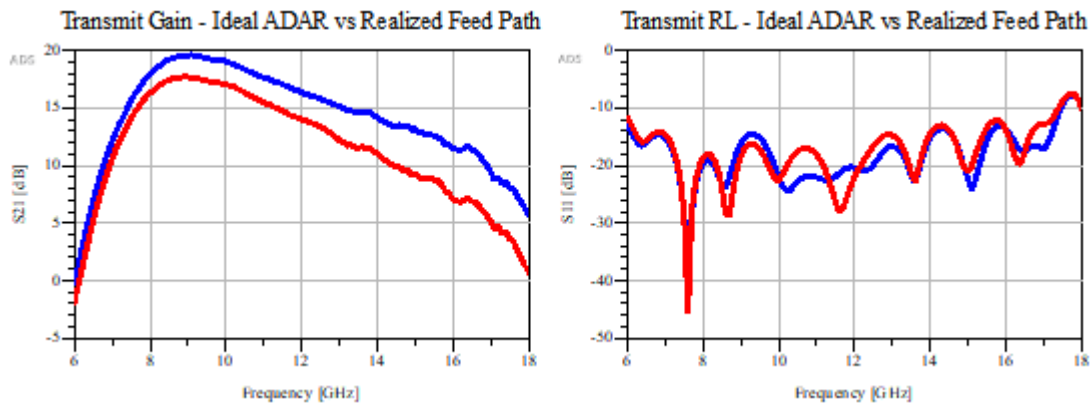
Figure 4.18 – 2 dB drop between the ideal case and realized feed path with most loss being associated with RF switch.

4.3 Thermal Considerations

To begin, we should address the material properties for the materials being used in this device,

Table 4.2 ADAR dissipated power

AVDD3 Supply Voltage	3.3 V	Power Draw
	Current	
Standby Mode	23 mA	.076 W
	Transmit Mode	
Nominal Bias	350 mA	1.155 W
Low Bias	240 mA	0.79 W
	Receive Mode	
Nominal Bias	260 mA	0.86 W
Low Bias	160 mA	0.53 W

Table 4.3 ADAR package thermal properties

	Thermal Resistance
Junction to Ambient (through mold)	18.7 C/W
Junction to Case (through slug)	10.1 C/W

$$P_{DC} + P_{RF_{IN}} - P_{RF_{OUT}} = P_{Diss}$$

Considering nominal receive bias and low VNA input power,

$$860\ mW + \ 0.1\ mW - 3.98\ mW\ = P_{Diss} = 856\ mW$$

$$\frac{T_j - T_a}{P_{Diss_{MAX}}} = \frac{135 - 30}{.856} = Max\ Thermal\ Resistance = 133.6\ (\text{°C} / W)$$

$$Equivalent\ Thermal\ Resistance = \frac{L}{kA}$$

Additional attention should be given to the area component of thermal resistance. In the case of this device and other devices with a lack of heat spreading due to low thermal conductivity metal layers, it is common for the heat effected cross sectional area to be much smaller than the cross-sectional area of the layer thus increasing the thermal resistance. Equivalent circuit simulations are able to match FEM thermal simulations much better when the effective cross-

sectional area has a heat spreading angle that is determined by the thickness and conductivity. In table 4.4 the thermal resistance is calculated to just show the thermal resistance using the entire layer and corresponds to the best-case scenario.

Table 4.4 - Layer Stack-up for printed device.

Layer Number	Layer Description	Thermal Conductivity (W/m-K)	Thickness (mm)	Cross Sectional Area (mm)	Thermal Resistance (°C /W)
8	Patch Antenna Layer	1	0.03	30 x 30	0.03
7	Antenna Substrate	0.172	2.3	30 x 30	14.8
6	Conductive Paste Ground Layer	1	0.03	30 x 30	0.03
5	ABS Microstrip Substrate	0.172	0.2	30 x 30	1.3
4	Signal Layer	1	0.03	35 x 30	0.03
2	FR-4 Board	0.25	0.5	12 x 10	16.7
1	ABS Base Substrate	0.172	1.75	35 x 30	9.7

Due to this being the best-case scenario they should not be considered heavily and including the package properties in Table 4.3 the thermal resistance leading from the junction to the top of the device is about 43 °C/W meaning that the temperature measured from the top of the device is about 43 $°C$ higher than the junction if 1 W is being dissipated by the device.

4.4 Fabrication and Measurement

The addition of the heat sink or any large conductor will usually decrease return loss, reduce the resonant frequency if coupled to the slot and would require tuning the geometry of the aperture coupled feed method in order to get efficient radiation. The first print involved direct printing of the layer interconnect on the IC as seen below in Figure 4.19 in the initial proposed design. This led to difficulties in the fabrication process as shown below where the via fabrication and print errors in high density areas resulted in consistent shorting of the feed lines. An evaluation board was proposed to ensure communication with the chip could be established at the minimum before attempting to print the antenna device.
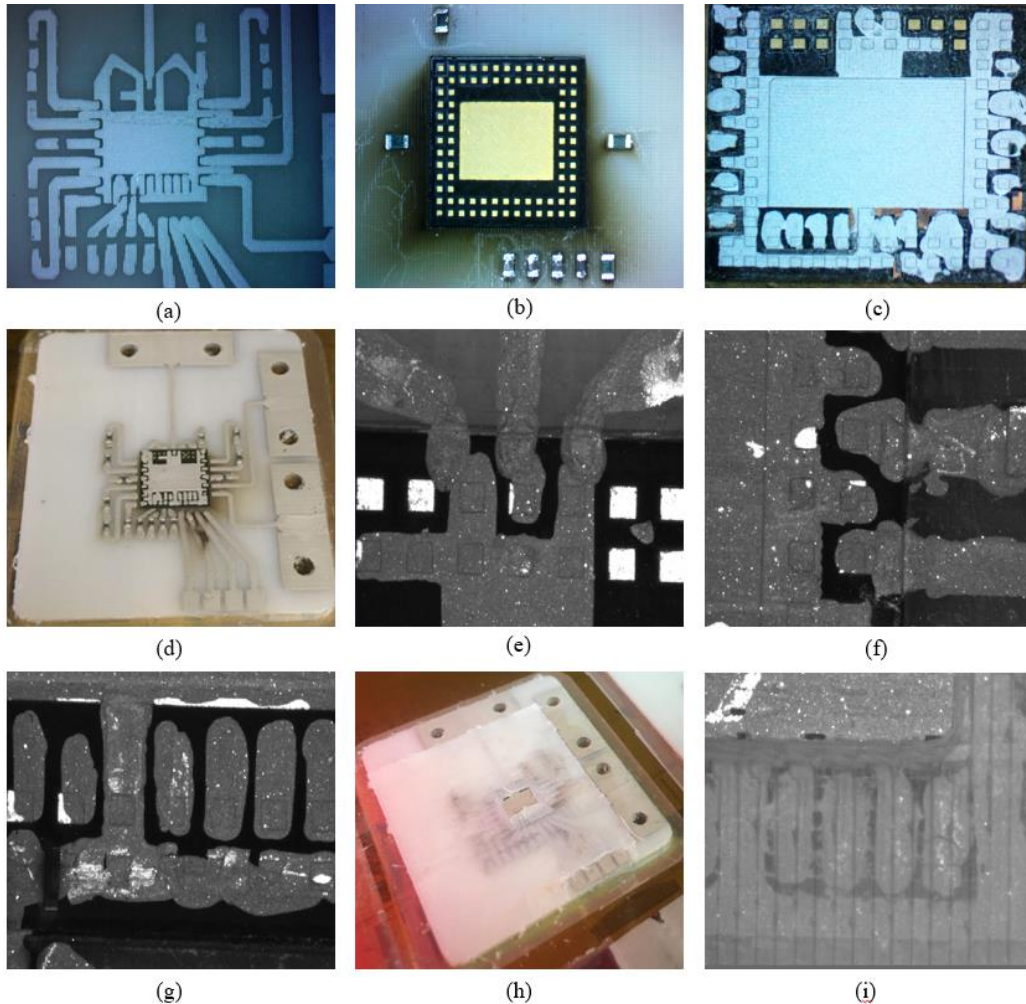
Figure 4.19 – Initial package fabrication images. (a) The initial evaluation board microstrip traces without using any chips in order to test tolerances. (b) Laser processed cavities and placed ADAR1000, LDO capacitors, and terminating resistors. (c) On chip printing of appropriate pads, slight shorting fixed with laser. (d) Placed IC and microstrip lines traces. (e)(f)(g) Critical Interconnect and on chip printing images. (h) Embedded IC with microstrip ADS substrate printed on top. (i) Problem location where on chip vias are necessary.

In Figure 4.19, an initial attempt to print an evaluation board using the USF tabletop printer and laser module to fabricate the device. Without initial access to a milling gizmo, all cavities were made with the laser and significant fabrication time. The pad pitch was 500 µm and the width of each pad was 250 µm. Although this pad size would not be testing the limitations of the microdispensing gizmo, the density and on-chip printing was a challenge in itself. With

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consideration of the later packaged device and how the design would need to change, the initial design would provide the more accurate measurements while the later device would allow for more fabrication errors and a potential for better reliability. In the bottom right figure of Figure 4.19, the SPI printed traces where the vias would need to be fabricated can be seen, but not shown is the poor adhesion of the CB028 to the device package which caused problems and shorting in other initial test prints.

(a)   (b)   (c)

(d)   (e)
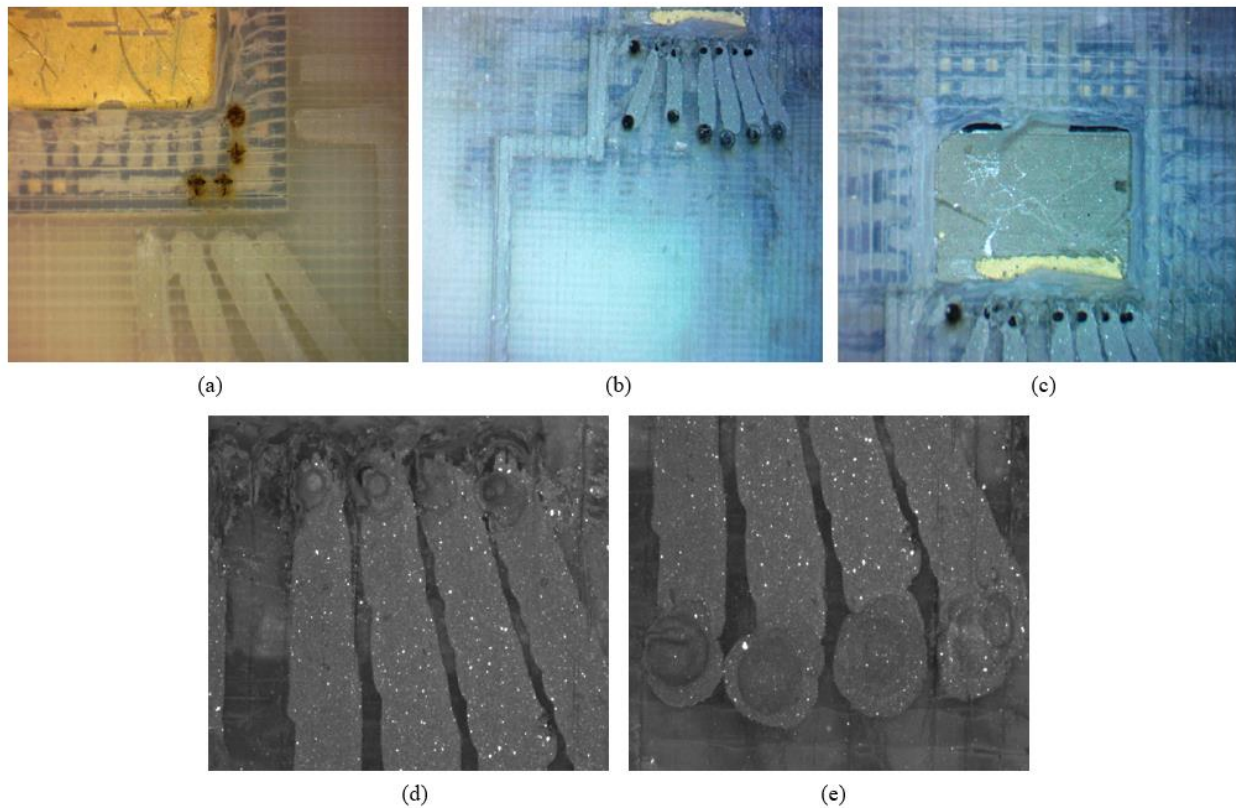
Figure 4.20 – (a) Initial testing of laser cutting thin layer in top of IC. (b)(c) Lasered vias and filled with conductive ink. (d)(e) Close up where short circuit was measured. Determined short was also occurring on IC after via filling.

At this point it seemed like the interconnect vias necessary would be extremely difficult to print and yielded a much higher probability for failure than was felt necessary for continuing. Due to the chip not designed to be implemented onto a board similar to the stack-up proposed in this work. A simpler solution by implementing a breakout board to redistribute all the critical

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internal pads to edge connect pads in order to print the device was proposed and moved forward with.
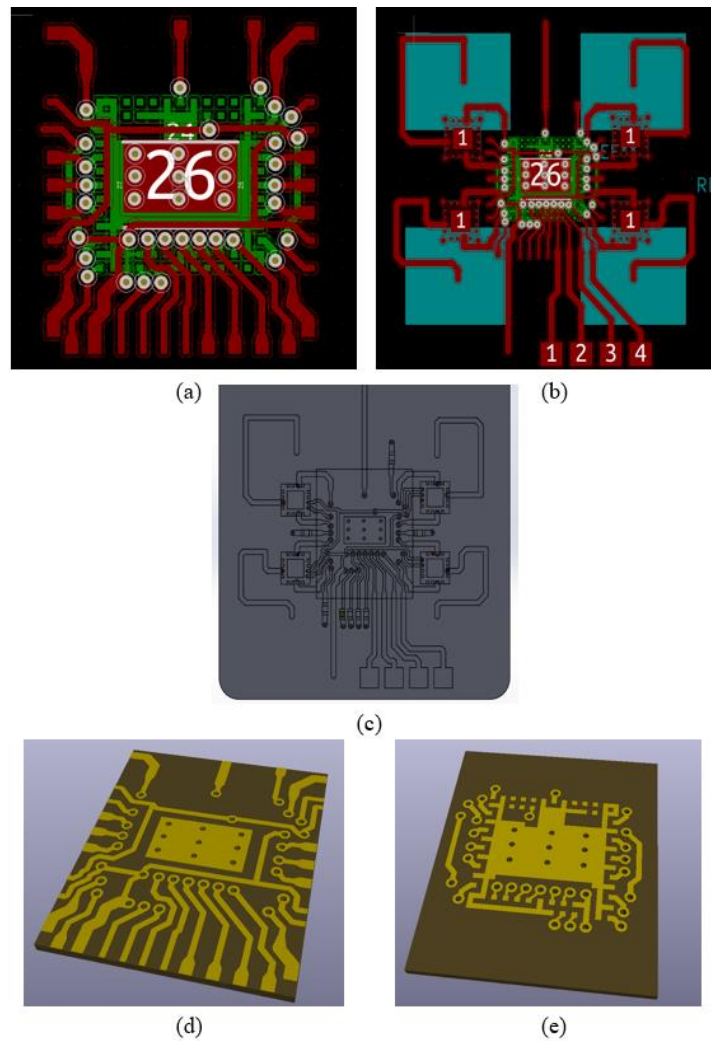
Figure 4.21 – (a)(d) 2D and 3D view of the top of the 2-layer breakout board that is flush with substrate and where interconnects are made. (b)(c) Layout and Full 3D model of the proposed breakout board. (e) Bottom of the 2-layer breakout board that the ADAR1000 gets soldered onto.

In Figure 4.21, the breakout board was made with FR-4 on short notice after significant effort was spent attempting to get the device to be completed entirely with the on-chip printing method. While the rest of the fabrication seemed like it would go smoothly, one problem was replaced with another in that solder reflow to connect the ADAR100 to the breakout board created

a lot of problems. The main design benefit of the breakout board was that it prevented on chip vias for the LDO capacitors, SPI traces, power supply pads, and the output switch control voltage. The breakout board allowed all the mentioned pads to be moved to the perimeter of the board in the vicinity of where they would need to be connected on the printed substrate.
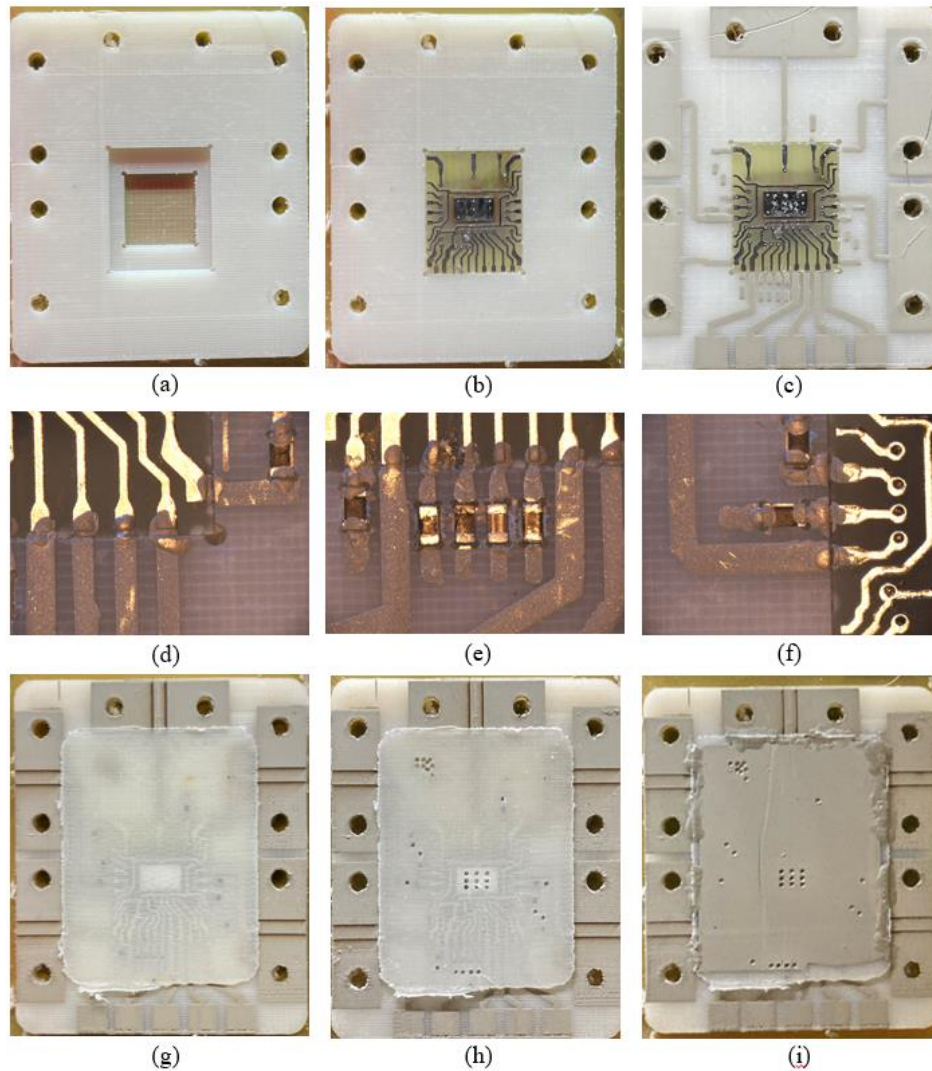
Figure 4.22 – Evaluation board fabrication images.

Figure 4.22 shows the evaluation board fabrication stages from the base substrate printed on the heated bed and cavity produced with the milling bit. Images (d) (e) (f) show the

microdispensed interconnects before additional material was added to prevent cracking or breaking of the interconnects.
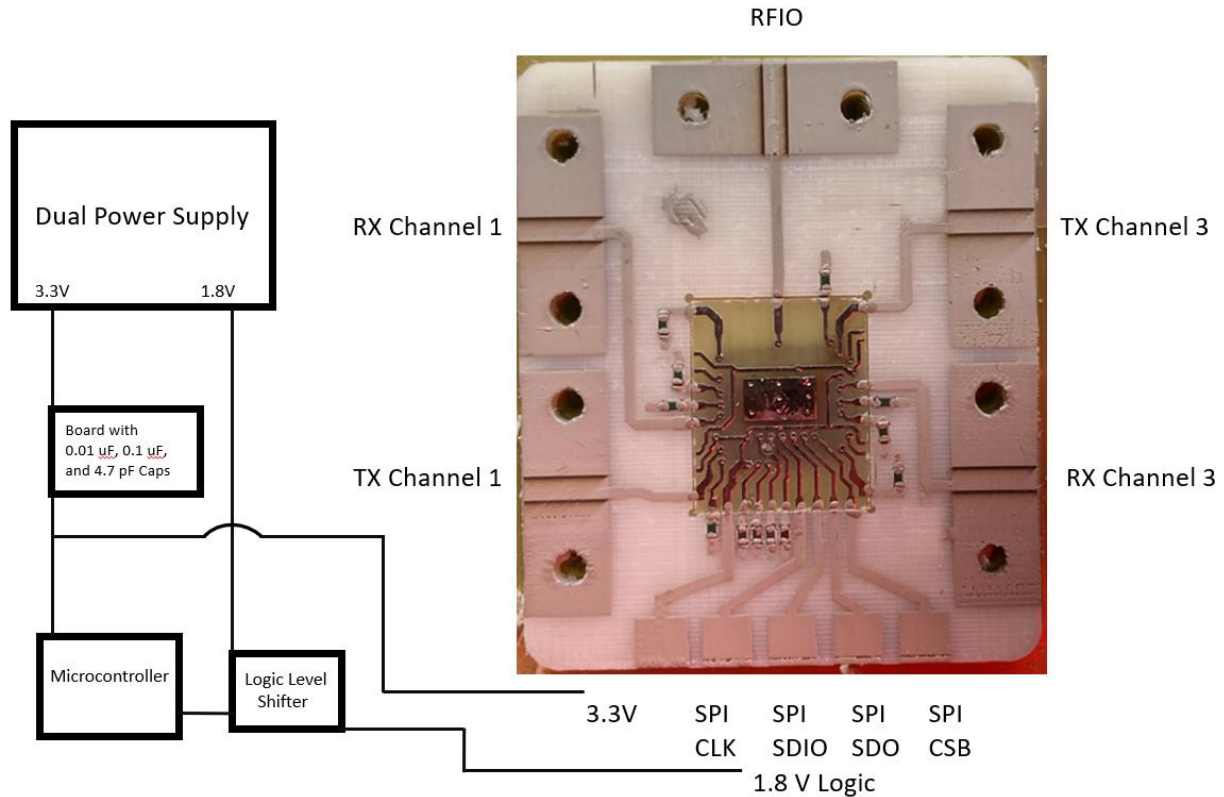
Figure 4.23 – Necessary boards and components for device operation.

The additional boards needed for to properly test the evaluation of the board are shown in a block diagram in Figure 4.23. The power supply provided a voltage to the microcontroller and a 1.8V reference for the logic level shifter. In the figure, a 3.3V supply is shown but a buck converter was used to convert the 5V supply to a 3.3V due to requirements of the microcontroller. An Arduino microcontroller was used and using the SPI libraries to send 24 bits at a time to the ADAR1000 was used and could be another source of error for the different modes chip. Manual reflow of the ADAR1000 on the evaluation board was attempted initially with a hot plate and later attempted with a reflow oven to provide the appropriate reflow profile. T4 solder paste was used and a laser cut stencil was used to get sufficient solder paste onto the evaluation board in the

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appropriate location. Both components were then placed on the bed of the HP-450 3D printer and the pick and place gizmo on the printer placed the ADAR in the correct location on the breakout board with the solder paste. After several reworks and measuring an open on at least one RX pad every time, the evaluation board was reworked and it was determined that placing the component down using the pick and place may have been squeezing out the solder paste from under the pads, no longer creating a good solder joint once reflowed. The parameters were changed to increase the ADAR1000 drop height and a single functional device was fabricated.

Through digital commands, of the 9 channels (1 RFIO, 4 Rx channels, 4 Tx channels), each one can be turned on individually with an assigned gain level and phase. The bias level can also be adjusted between low power and nominal power consumption. The results shown in Figure 4.24 show the result of several attempts to get a measured result from the chip after trying to put in several different modes and bias conditions. Although in most cases, when a new condition was written to the chip and the microcontroller was powered on after connecting to the evaluation board, the current draw would change and reflect what was to be expected based on the datasheet but no measurable results would be observable on the ENA. In transmit modes, because the reflow connection could not be verified through the pad resistance to ensure the breakout board was connected to the ADAR like the RX pads, it was determined that the connection was not made or the solder impedance was too high. The other RX modes were thought to be unsuccessful due to a digital issue where either a clear clock signal or digital out commands saw a decrease in signal integrity due to the connection method or interconnect impedance. As seen in Figure 4.24, the gain is low across the entire functional band likely due to interconnects and the RFIO return loss being low. Other printed devices showed compromised interconnects that had cracked and lost connection during transport to a different building or when attaching the RF connectors to the

device. For this reason, a considerable amount of material was added on the chip to substrate interconnect to prevent device failure at the cost of device performance. In the inks viscous state before drying it has also been seen to drip into the cavity which might also be a source of problems.
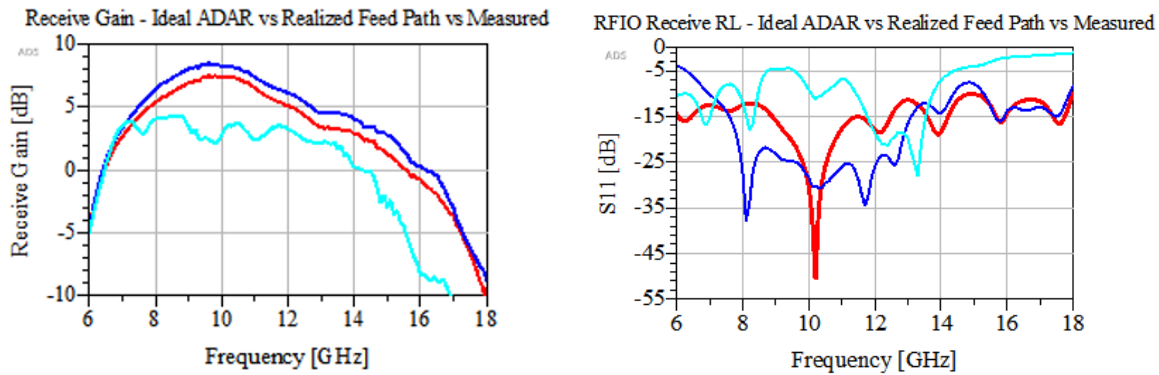
Figure 4.24 – Receive Gain and return loss comparison between simulated ADAR1000 with RF Switch (blue), ADAR1000 and RF Switch with transmission lines (red), ands measured (teal).

Table 4.5 – Evaluation board temperature

Mode	Condition	Current Draw	Temperature*
Transmit	4 Channels Enabled Nominal Bias	375 mA	70.4 °C
Transmit	Single Channel Enabled Nominal Bias	105 mA	40.5 °C
Receive	4 Channels Enabled Nominal Bias	260 mA	53.2 °C
Receive	Single Channel Enabled Nominal Bias	76 mA	34.7 °C

* Maximum surface temperature measured with thermal IR camera

In Table 4.5 recorded temperatures were measured with a thermal IR camera on the evaluation board with it connected to an ENA and power supply. The only condition that lead to a measured result on the ENA was from the single channel enabled nominal bias condition and significant problems were found when attempting to write code to the ADAR chip. The problems are suspected to stem from the digital and power connections from the supporting circuit and Arduino that were connected to the printed device via alligator clips. Initial design lead to questions concerning the stability and reliability of header pins that could be embedded into the structure or epoxied to the top surface and alligator clips were thought to be sufficient for this study but based on experimental results this wasn't the appropriate decision. Improvements were

made based on previous studies on the reliability of the RF connector by choosing a connector and design that would support edge connectors with through bolts that could be used to secure the SMA connector to the device. The same attention should also be put towards any other device connection as a result of the problems faced in this study.
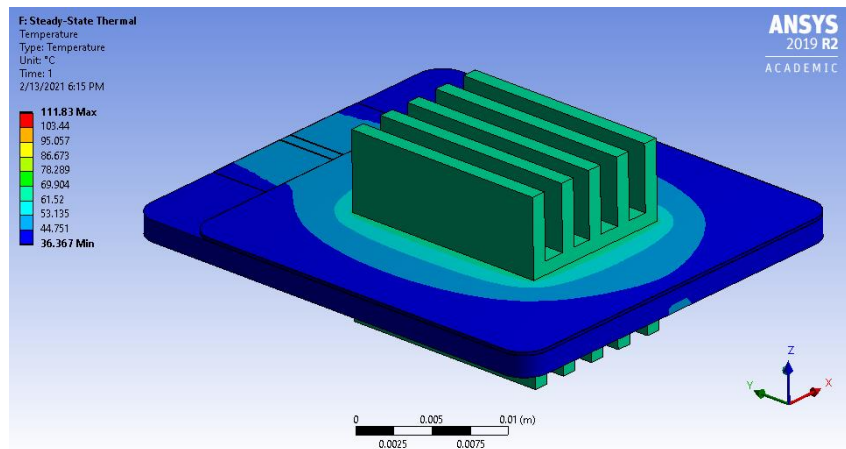
Figure 4.25 – 0.8 W Heat source with 8 w/m-K convection coefficient on top and bottom heat sinks.

Simulation was originally performed with a variety of heat convection coefficients on the top and bottom heat sinks to develop an expected range for temperature measurements. After taking measurements as seen in the following figures, the simulation was revisited and attempted to observe which convection coefficients leads to a result matching the measurement and a single evaluation board result can be seen in Figure 4.25. The original designs based the heat sink sizing on a convection coefficient between 10 – 20 W/m-K, but since this is the driving factor controlling how much heat can be dissipated to the environment a conservative approach must be taken to avoid over estimating and greatly influencing the resulting steady state temperature. Although the steady state condition is considered here because this is how it would need to be measured, actual functionality in its desired environment would be simulated by pulsing of the transmit and receive modes and not keeping them in a constant state.
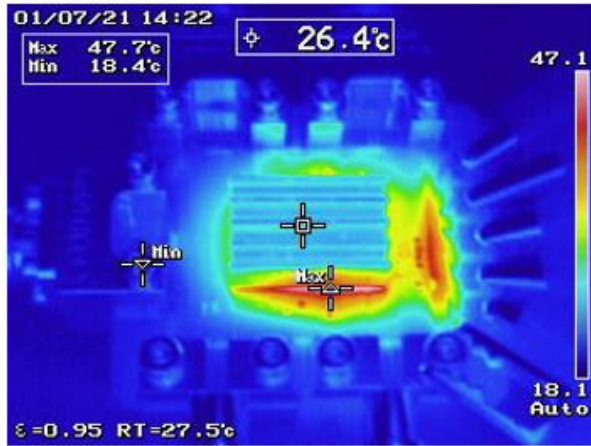
Figure 4.26 – Measured thermal temperatures at various bias conditions.

Figure 4.26 shows the results of evaluation board with a top and bottom heat sink and drawing the appropriate current. Figure (d) is with the device in TX mode and nominal bias, (b) and (c) both in the RX mode and nominal bias, and (a) in TX mode low bias. The other conditions did not deviate significantly from what was expected and the single enabled channels resulted in slight temperature increases up to about 35 °C.

m4	m5	m6
freq=10.00GHz	freq=10.00GHz	freq=10.00GHz
phase(S(5,6))=55.939	phase(S(1,2))=107.668	phase(S(7,8))=144.697

m3	m2	m1
freq=12.00GHz	freq=12.00GHz	freq=12.00GHz
phase(S(5,6))=-13.283	phase(S(1,2))=30.056	phase(S(7,8))=62.154
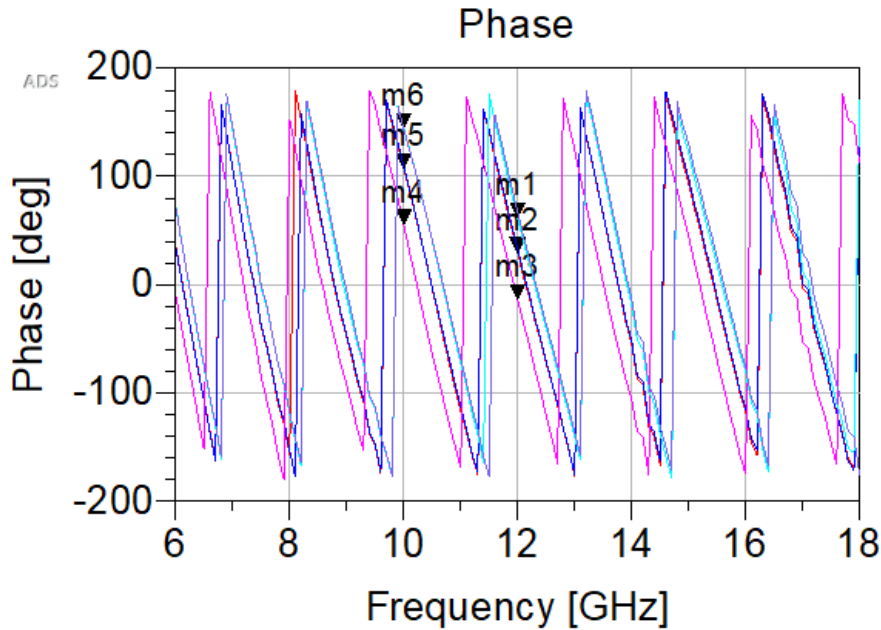
Figure 4.27 – Phase shift output from evaluation board receive mode when set to 45°, 0°, and 90° phase shift.

While measuring the gain on the evaluation board, phase measurements were also taken after quickly powering down the microcontroller, uploading new code, and turning it back on while connected to the test setup. In Table 4.6 it can be seen that at some frequencies and designated phase shifts there can be significant error from the reference phase when a 0° phase shift is wanted from the RX channel.

Table 4.6 Phase shift measurements

SPI Coded Phase Shift	Phase Shift at 8 GHz	Phase Shift at 10 GHz	Phase Shift at 12 GHz
0 Deg	Reference (152°)	Reference (55°)	Reference (-13°)
45 Deg	44°	52°	43°
90 Deg	82°	89°	75°
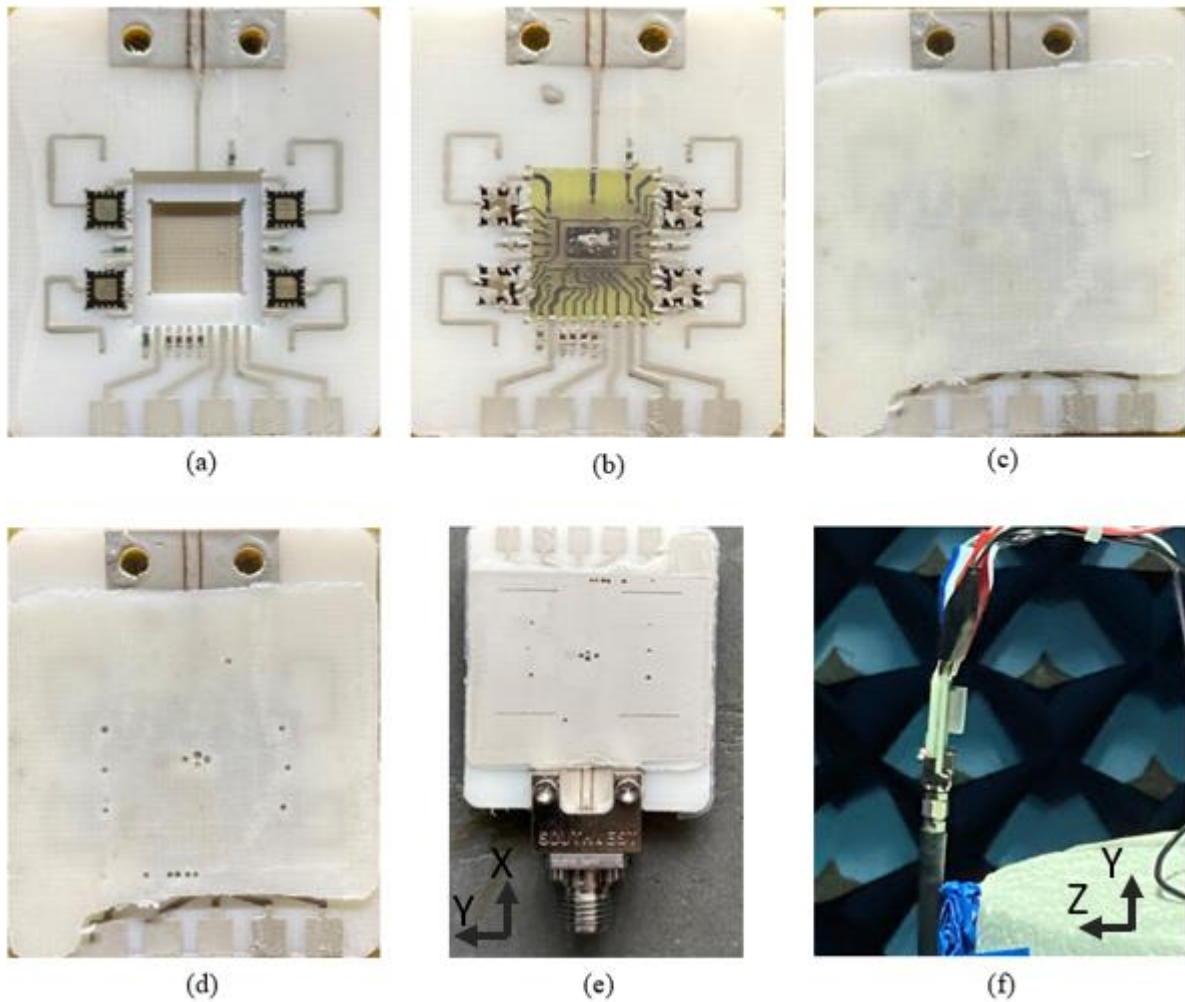
Figure 4.28 – Final Antenna Array Fabrication images.

In Figure 4.28, the method is nearly identical to the evaluation board apart from the aperture slot, antenna substrate and embedded switches. The antenna substrate with the 4 patches was printed separately and bonded afterwards in order to prevent warping which is common due to the

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heating and cooling during different print processes. Figure (b) provides an image of the interconnects after recently dispensing the ink and it should be noted that a generous amount of ink was used for all interconnects to prevent cracks in the ink developed during transport or slight bending when removing the substrate from the printed bed from occurring. Between microdispensing and measurements, consistent problems have plagued the device fabricated at USF and in future studies interconnects need to be addressed for reliability and thicker substrates can also be used to prevent bending and improve mechanical stability. Figure (d) shows the microstrip ABS layer before the ground layer has been printed. Notable for device performance is the lack of ground vias for the RF switch where a single large via is used for each IC. While having several smaller vias would have decreased inductance, fabrication was limited by end mill diameter and the ability to see the exposed pad when using smaller bits. Figure (e) shows the ground layer with the aperture slots that had been fabricated using the end mill. The depth of cut was only about 40 µm so a 0.05 mm diameter end mill could be used to cut the slots. Figure (f) shows the device with a smaller heat sink then what was originally intended in order to show better radiation at 10 GHz from reduced aperture impedance impact. Using a smaller heat sink that doesn't cover the aperture slots and minimally covers RF traces to avoid them behaving more like strip lines resulted in an improved radiation efficiency in the desired frequency range based on HFSS results. The larger the heat sink and the more it covers the aperture slots, the more the radiation improves near 12 GHz and drops at 10 GHz.
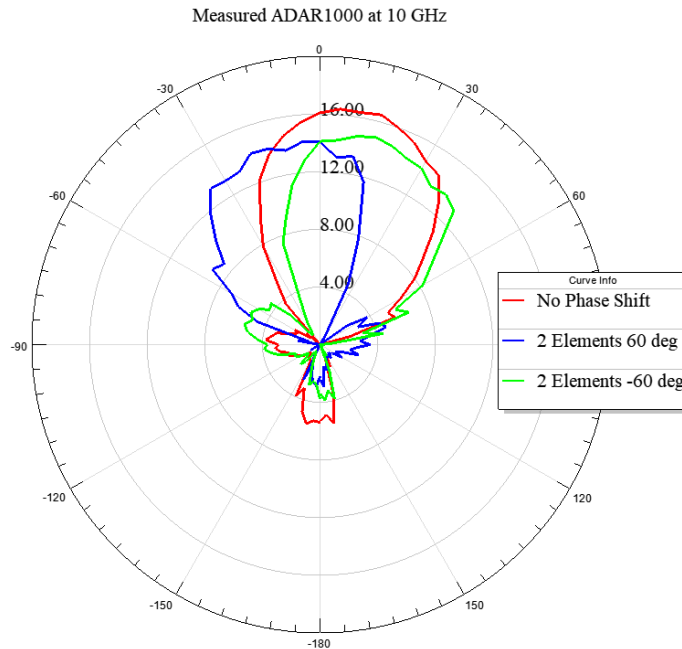
Figure 4.29 – Measured ADAR1000 at 10 GHz in elevation plane with 2 element phase shifts for 3 resulting states.

The above measurement was taken with the small top heat sink seen in Figure 4.12 (a) and a medium back heat sink as shown in Figure 4.28 (f). The maximum channel gain from all 4 driven channels on the device is around 15 dB, the antenna array gain is expected to be about 6 dB, thus, making the loss around 6 dB. This is expected to be largely from an impedance mismatch and coupling of the antenna and heat sink. The measured results were taken in the anechoic antenna chamber at limited frequencies to reduce radiation measurement time in and increase the likelihood of a successful measurement in the case of a problem. After the initial broadside measurement with 0-degree phase shift on all elements which is shown in red was taken, it was determined that there may be a slight difference in the feed line length or aperture slot alignment on top of the angle misalignment relative to the calibration antenna. With respect to the other two measurements it should be noted that the ADAR1000 doesn't allow for a discrete 60-degree phase shift so instead the I and Q registers were coded for 59 degrees and there was expected to be slight phase errors between all elements as well. While other angles had been coded and attempted to be radiated like

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what had been measured on the evaluation board such as 45 degrees and 90 degrees, several microcontroller restarts and code uploads were needed to get the two additional angles measured to radiate and no radiation occurred in other states. Although current draw may be correct, radiation could only be detected after . While measuring on the evaluation test bench similar problems were seen where there was an inconsistent ability to put the ADAR1000 in different phase and gain states most likely due to the digital connections and the lack of quality and care taken to ensure a good digital signal was delivered to the IC. The 7-8 dB realized gain from the antenna array and a total of 15 dB from all 4 driven channels on the ADAR1000 chip leads to about 6 dB of unaccounted for loss that could be largely due to impedance mismatches where fabrication greatly compromised the performance of the device. The single element gain is higher than what is measured in the evaluation board as expected due to lower losses from microstrip to CPW transition but the switch insertion loss must still be accounted for. The lower gain from the phase shifted elements could be due to non-coherent combining of signal due to phase error.

A beamforming IC has been embedded in a 3D printed substrate and measurable results have been obtained. To improve the design, functionality, and most importantly the reliability of printed devices, studies should work to improve interconnects such that they have a much smaller chance to crack or become disconnected under movement and twisting of the device. Interconnects were the main cause of failure for several printed devices in this study and lead to a substantial increase in fabrication time. While more time should have been dedicated to improving the design and more attention should have set for the digital design and integration, most of the thesis time was spent strictly fabricating and determining the best method to print each stage of the device within the printing ability of the platform.

Chapter 5: Conclusion and Future Work

The thesis documents the process development and measurement of an RF beamforming IC with active components that has been integrated with antennas into a single 3D printed package. This has been the first work to embed an active beamforming IC on a single printed platform and represents an important progression in the development of 3D printing technology and the feasibility to be used in a wide array of practical applications. While the technology still has a long way to go, the possibility has been explored and what needs to be further addressed will be mentioned below.

The lessons learned and challenges that had had to be overcome have been addressed within this work but it is critical to emphasize what research is needed to make future printed devices more reliable and repeatable. The interconnects of the device are the primary failure point after embedding and if it was possible to print more rigid substrates or interconnects that had better adhesion or flexibility then that could reduce errors. The fabrication of high-density routing or vias was also shown to be a problem, optimization and platform improvements can be made to remove the human element and improve the ability to confirm the fabrication of a successful via. The digital signaling and control needs to be carefully considered similar to the RF routing especially if the clock signal is operating at a high frequency. Initial consideration of how this device is going to be measured, specifically within the anechoic chamber would also improve performance.

This study builds off previous 3D printed antenna structures to embed an active beamforming device in order to help pave the way for future studies to improve this technology.

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