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Systems and methods for forming contact definitions

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(54) **SYSTEMS AND METHODS FOR FORMING CONTACT DEFINITIONS**

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(22) Filed: **Oct. 18, 2013**

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H01L 29/40 (2006.01)
G03F 1/42 (2012.01)
H01L 21/283 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 29/408*** (2013.01); ***G03F 1/42*** (2013.01); ***H01L 21/283*** (2013.01)

(58) **Field of Classification Search**
CPC H01L 2924/00; H01L 2924/00014; H01L 2224/48091; H01L 2224/45015; H01L 2224/32225; H01L 2924/00012; H01L 2224/48227; H01L 2224/73265; H01L 2224/45014; H01L 2224/45144; H01L 2924/15311
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,370,203	A	2/1968	Kravitz et al.	
3,988,824	A	11/1976	Bodway	
4,437,235	A	3/1984	McIver	
4,843,453	A	6/1989	Hooper et al.	
5,275,165	A	1/1994	Ettinger et al.	
5,358,886	A	10/1994	Yee et al.	
5,693,540	A	12/1997	Turner et al.	
7,282,440	B2	10/2007	Dennison et al.	
7,719,120	B2	5/2010	Hiatt et al.	
7,863,091	B2	1/2011	Coteus	
7,951,702	B2	5/2011	Wood et al.	
2002/0153828	A1 *	10/2002	Yamanobe et al.	313/495
2004/0104655	A1 *	6/2004	Kodera et al.	313/292
2004/0121589	A1	6/2004	Pividori	
2007/0038100	A1	2/2007	Nita	
2010/0207168	A1 *	8/2010	Sills et al.	257/202
2011/0204312	A1 *	8/2011	Phatak	257/4
2013/0345599	A1	12/2013	Lin et al.	

OTHER PUBLICATIONS

International Search Report for PCT/US2014/036625, dated Sep. 5, 2014.

* cited by examiner

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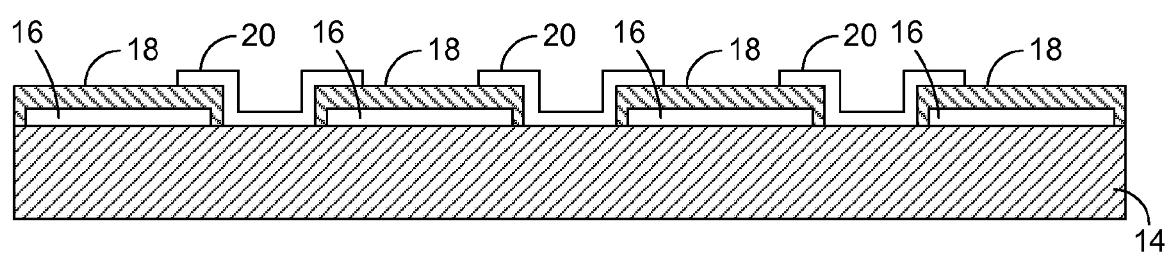
(57) **ABSTRACT**

In one embodiment, an electrical circuit formed on a substrate includes a first multi-layer stack and a second multi-layer stack that share a top layer that comprises a continuous piece of conductive material.

21 Claims, 5 Drawing Sheets



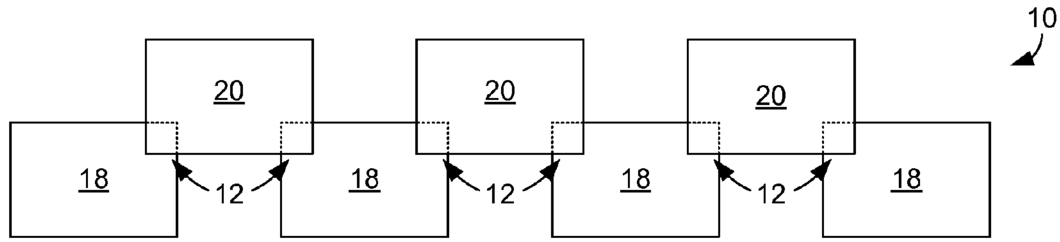


FIG. 1

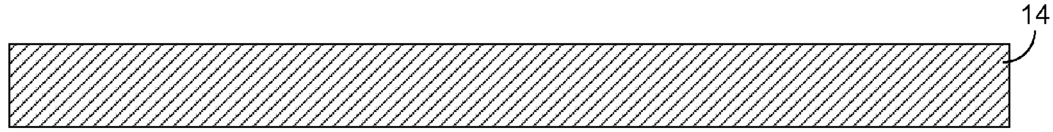


FIG. 2A

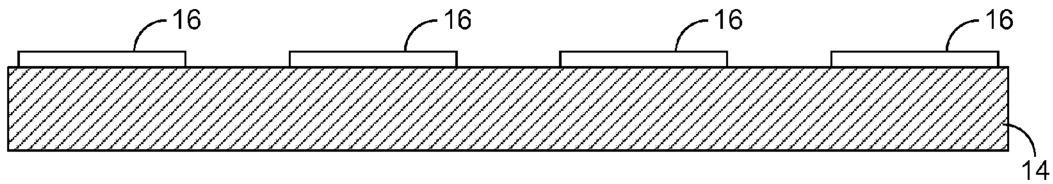


FIG. 2B

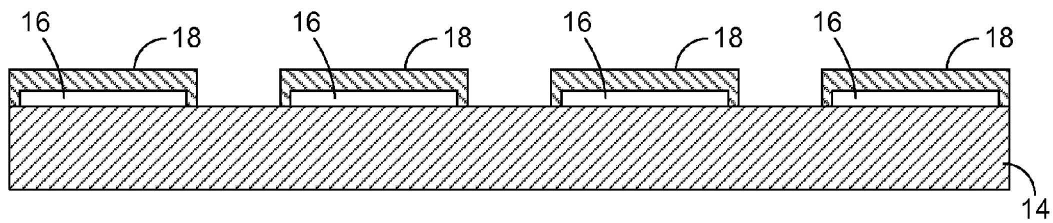


FIG. 2C

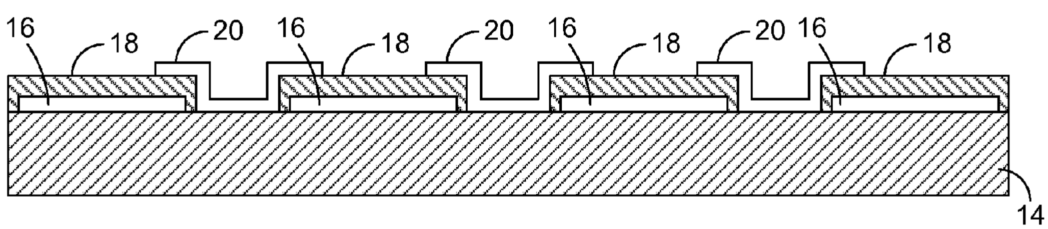


FIG. 2D

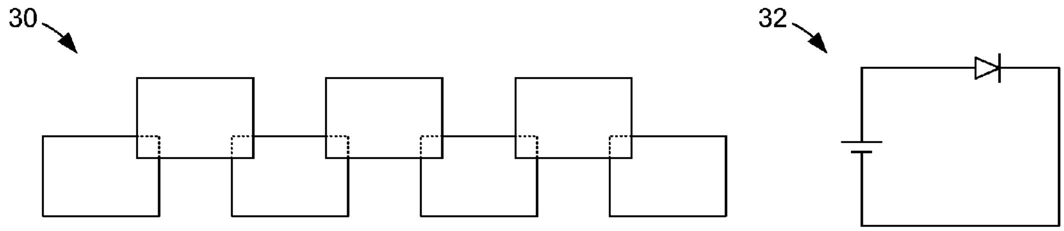


FIG. 3A

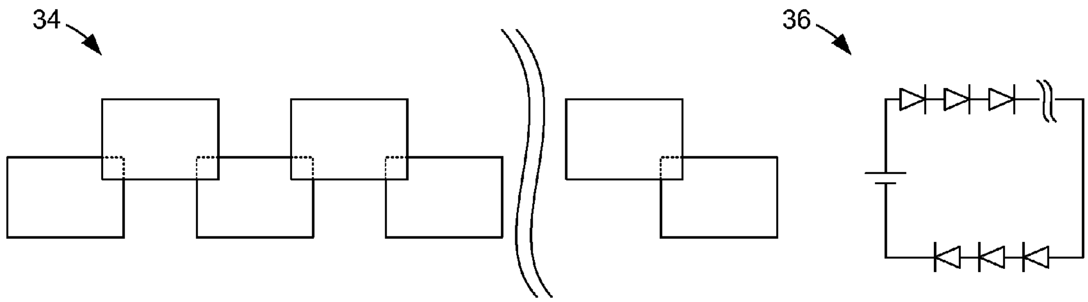


FIG. 3B

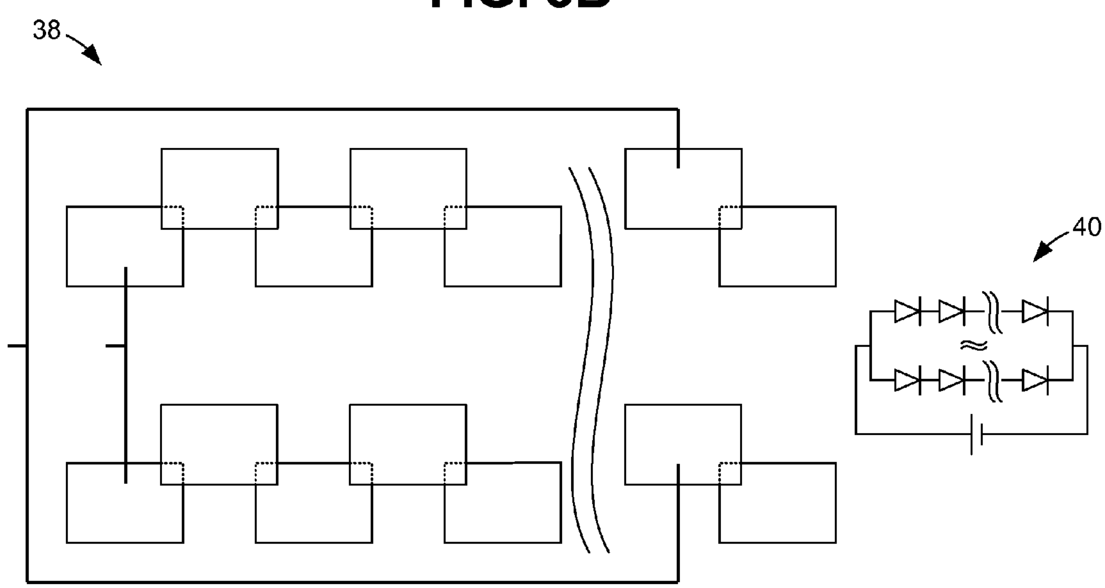


FIG. 3C

FIG. 4

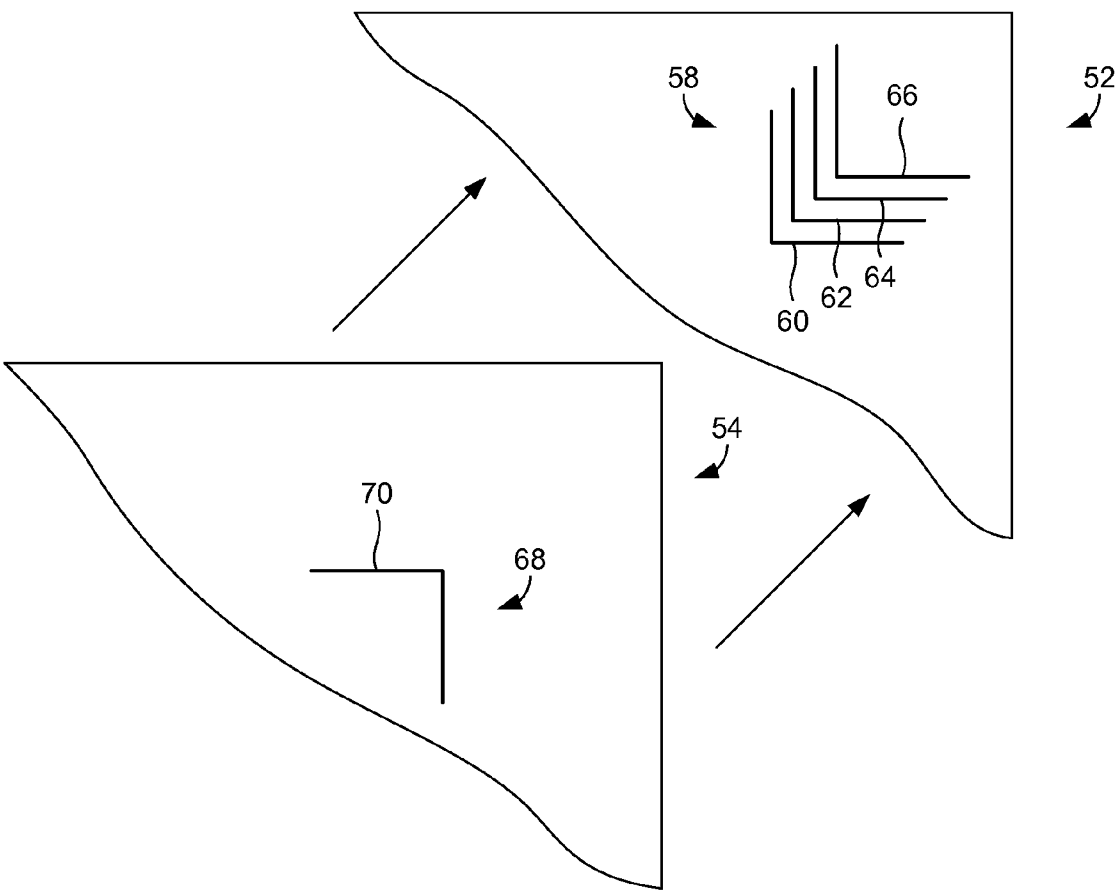


FIG. 5

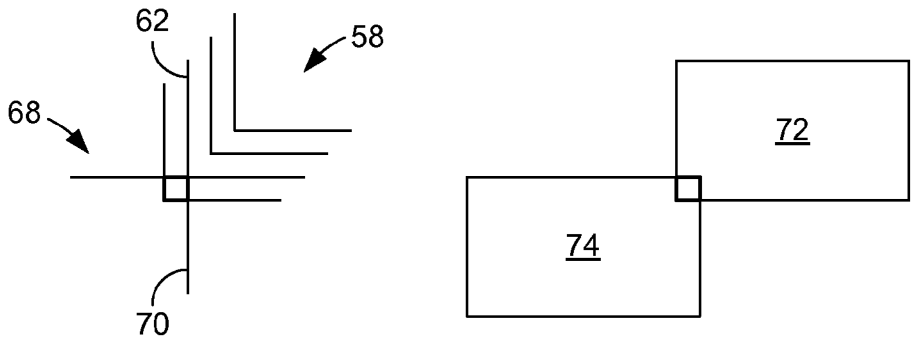


FIG. 6A

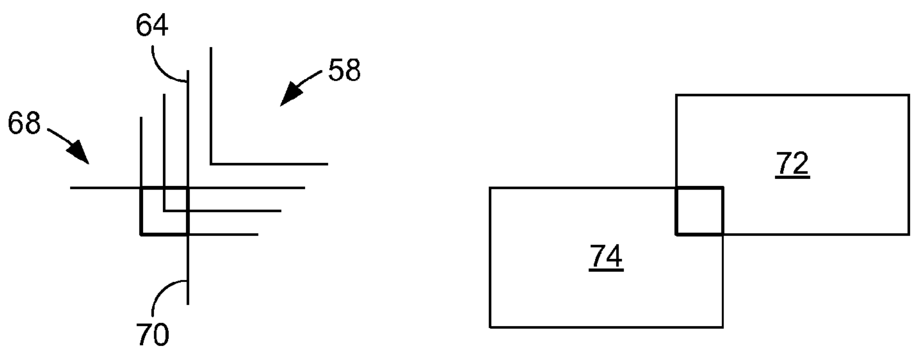


FIG. 6B

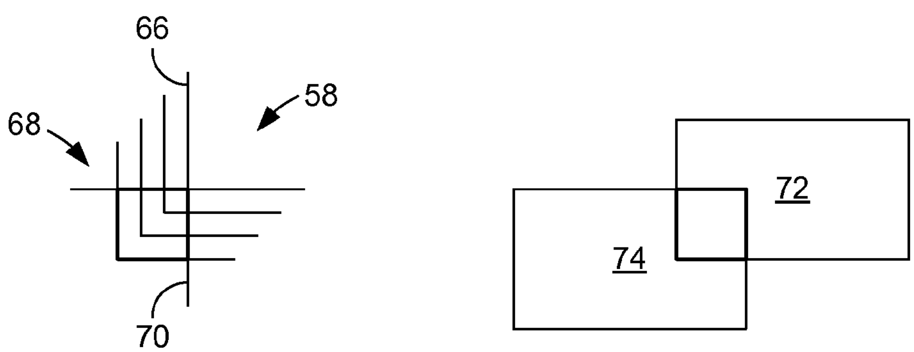


FIG. 6C

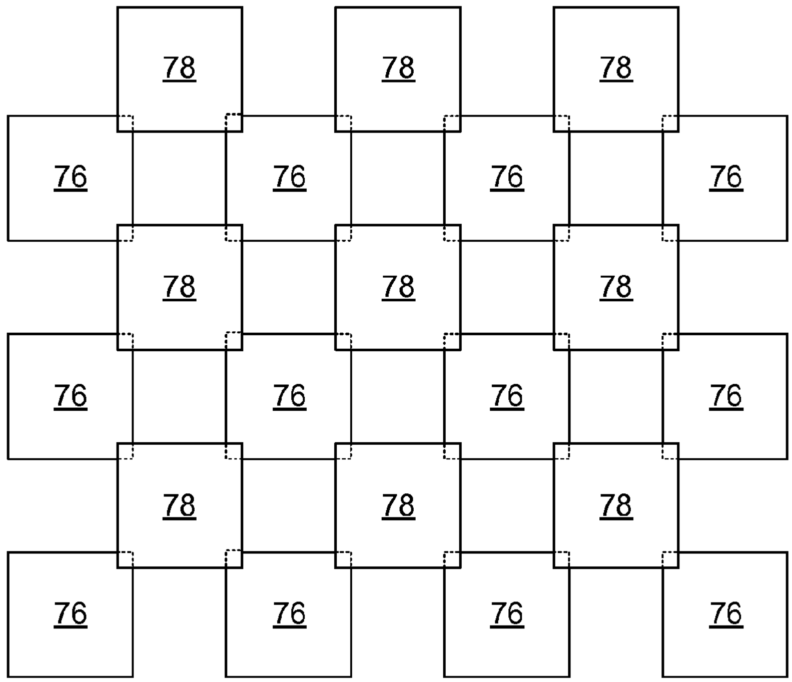

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FIG. 7

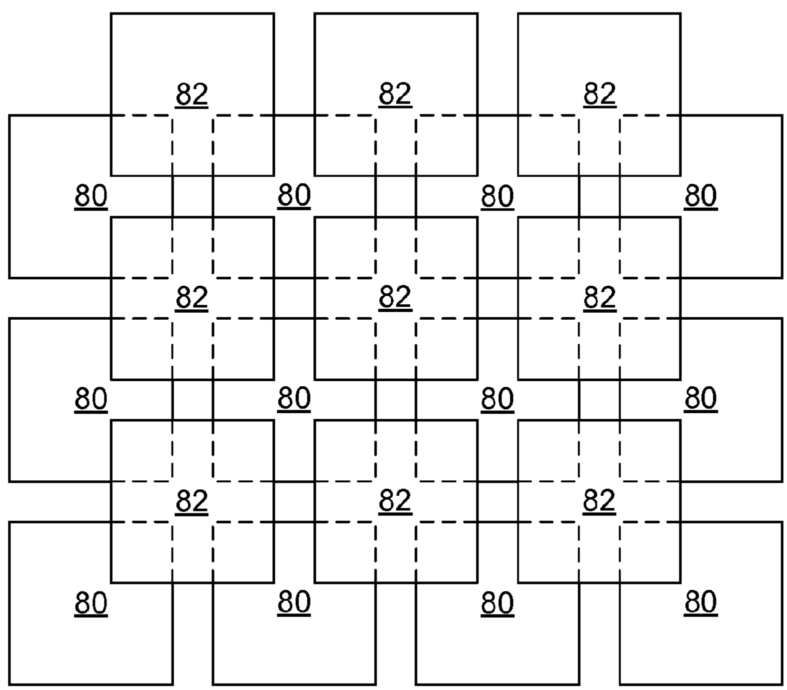
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FIG. 8

SYSTEMS AND METHODS FOR FORMING CONTACT DEFINITIONS

CROSS-REFERENCE TO RELATED APPLICATION(S)

This application claims priority to U.S. Provisional Application Ser. No. 61/715,430, filed Oct. 18, 2012, which is hereby incorporated by reference herein in its entirety.

BACKGROUND

One of the most important aspects of chip fabrication, such as complementary metal-oxide-semiconductor (CMOS) fabrication, entails the contact definitions. In a highly complex chip design, there are many contacts to interconnect a multitude of devices within the chip. Devices such as transistors and diodes specific to a particular circuit have contacts dedicated to that circuit. Parallel and series circuits are generally made by fabricating devices specific to that circuit, and a circuit requiring the connections of the devices in a particular way is separately fabricated. If a different circuit comprising the same device types but requiring a different circuit connection is needed, a new set of devices with the required connections would have to be fabricated separately. Such a process reduces real estate in a chip and gives rise to other complications, such as reliability issues during fabrication, reliability issues during operation, and increased heat buildup in the chip.

It can therefore be appreciated that it would be desirable to have an alternative system and method for forming contact definitions.

BRIEF DESCRIPTION OF THE DRAWINGS

The present disclosure may be better understood with reference to the following figures. Matching reference numerals designate corresponding parts throughout the figures, which are not necessarily drawn to scale.

FIG. **1** is a schematic diagram of an embodiment of a circuit comprising multiple metal-insulator-metal devices.

FIGS. **2**A-**2**D are cross-sectional views that illustrate steps in an embodiment of fabricating the circuit of FIG. **1**.

FIGS. **3**A-**3**C are schematic diagrams of alternative circuit embodiments comprising multiple metal-insulator-metal devices.

FIG. **4** is a partial side view of a mask set that can be used to fabricate a circuit.

FIG. **5** is a top view of two of the masks of the mask set of FIG. **4**, illustrating alignment marks provided on the masks.

FIGS. **6**A-**6**C are illustrations of different alignments between the masks of FIG. **5** and show the results of the alignments.

FIG. **7** is a first example circuit that can be formed using the masks of FIG. **5**.

FIG. **8** is a second example circuit that can be formed using the masks of FIG. **5**.

DETAILED DESCRIPTION

As described above, current methods for forming contact definitions for devices on a chip can be disadvantageous because circuits for connecting the devices must be specifically fabricated for the desired circuit. Therefore, if a different circuit comprising the same device types is desired, a new set of devices with a new set of connections would need to be separately fabricated. As described herein, such disadvantages can be avoided. In some embodiments, a circuit comprising multiple metal-insulator-metal (MIM) devices can be formed by depositing layers of metal that both form the top electrodes of the MIM devices and provide interconnection of the MIM devices. In some embodiments, the extent to which the layers of metal overlap, and therefore the size of the active area, can be controlled to change one or both of the current density and the frequency range of the devices.

In the following disclosure, various embodiments are described. It is to be understood that those embodiments are example implementations of the disclosed inventions and that alternative embodiments are possible. All such embodiments are intended to fall within the scope of this disclosure.

The methods disclosed herein enable multiple MIM tunnel devices to be connected either serially or in parallel to form an electrical circuit. Moreover, the contact areas between devices can be altered by simply moving a photomask used to form the top electrodes of the devices by incremental distances. This enables the current densities of the devices to be altered without having to redesign the devices. In some embodiments, a plurality of MIM devices can be fabricated with the point of contact being defined in such a way that the devices can be used in series or in parallel with multiple variations, as desired for the test setup or circuit. Moreover, by varying the dielectric properties and/or thicknesses of the insulators, the devices can be altered to be used as a resistors, capacitors, or diodes.

Thin-film devices are now increasingly used in the fabrication of passive elements such as resistors and capacitors, and active devices such as diodes including transistors. MIM devices are widely-used thin-film devices. MIM devices typically are formed as quadrilateral structures that include a bottom electrode, an insulator, and a top electrode. The fabrication methods described below enable multiple MIM devices to be connected either serially or in parallel to complete an electrical circuit. Moreover, the contact areas between devices can be altered by simply moving the photomask used to form the top electrode. This enables the current densities of the devices to be altered without having to redesign the devices. Assuming a quadrilateral configuration, one, two, three, or four devices can be connected at any single circuit connection. Therefore a base of one, two, three, or four connection combinations can be achieved. By connecting the devices in such a manner, bottom electrodes and insulator stacks can be independently fabricated and the circuit can later be completed by forming top electrodes that connect two or more electrode/insulator stacks. Also, by including a switching element, single or multiple devices can be called into operation as needed without having to constantly pass power through the same devices.

FIG. **1** illustrates an example circuit **10** that can be formed using the techniques described above and FIG. **2** illustrates steps of an example fabrication method. In the example of FIG. **1**, six MIM devices **12** are formed. As is shown in FIG. **2**A, the circuit **10** can be formed on a substrate **14**, such as a silicon substrate. With reference to FIG. **2**B, bottom electrodes **16** of the devices **12** can be formed on the substrate **14** in a spaced configuration. In some embodiments, the electrodes **16** are made of a metal material, such as nickel, aluminum, gold, or platinum, and are deposited using a conventional microfabrication process, such as photolithography and material deposition (e.g., sputtering). In some embodiments, the electrodes **16** can be approximately 0.5 to 3 μm thick.

With reference next to FIG. **2**C, each of the bottom electrodes **16** is encapsulated in a layer or film **18** of insulating material. In some embodiments the insulating material can

comprise one or more of a metal oxide (e.g., nickel oxide or aluminum oxide) or a polymer (organic or inorganic) and can also be formed using a conventional microfabrication process. In some embodiments, the insulating films **18** can be approximately 0.001 to 1 μm thick. The insulating films **18** act as insulators in the MIM devices **12**.

Once the bottom electrodes **16** and insulating films **18** have been formed, a photomask can be used to define windows for the top electrodes of the MIM devices **12**. As with the bottom electrodes, the top electrodes can be made of a metal material, such as nickel, aluminum, gold, or platinum, and can also be formed by using a conventional microfabrication process. As shown in FIG. **2**D, layers of metal **20** can be deposited on top of the insulating films **18** to form the MIM devices **12** shown in FIG. **1**. In some embodiments, the metal layers **20** can be approximately 0.5 to 3 μm thick.

As indicated FIG. **2**D, each metal layer **20** covers portions of the insulating films **18**, and therefore overlaps bottom electrodes **16**, of multiple devices **12** (two devices in this example) so that the top electrodes of multiple MIM devices are formed by the same metal layer. In other words, the deposited metal layers **20** extend across multiple MIM devices so as to both form the top electrodes of and electrically connect the MIM devices over which they extend. As is shown in FIG. **2**D, the metal layers **20** also cover portions of the sides of the insulating films **18** as well as the surface of the substrate **14**. In the illustrated embodiment, four metal/insulator stacks are covered by three metal layers **20** to form six MIM devices **12** that are electrically connected to each other. Therefore, multiple MIM devices can be simultaneously fabricated and interconnected in a single lithography step.

The method described above can be used to form devices that are serially connected or connected in parallel. FIGS. **3**A-**3**C illustrate example circuit layouts **30**, **34**, and **38** (left) and their equivalent circuit diagrams **32**, **36**, and **40** (right). In the circuits, each of the devices can be MIM devices, which can be configured as resistors, capacitors, or diodes, depending upon the nature of the insulation films (e.g., dielectric properties, thickness) that is used in their construction. As can be appreciated from the layouts and circuit diagrams, a plurality of MIM devices can be connected either serially (FIGS. **3**A and **3**B) or in parallel (FIG. **3**C) and the connections between the devices can be altered depending on the desired result.

As expressed above, the circuits can be formed using conventional microfabrication processes, such as photolithography. In such a process, photomasks are used to define the patterns of the features (e.g., electrodes) that are to be formed on a substrate. In the typical case, a mask set comprising one photomask for each layer of the devices to be formed is provided. FIG. **4** shows an example mask set **50** that comprises three photomasks, **52**, **54**, and **56**, which can, for example, be used to form the bottom electrodes, insulating layer, and top electrodes, respectively of multiple MIM devices. Each photomask **52-56** can comprise a thin transparent (e.g., glass) plate that includes a layer of opaque material (e.g., chrome) that forms a pattern that enables ultraviolet light to pass through the plate in some areas (e.g., where an electrode is to be formed) but prevents the light from passing through the plate in other areas.

The photomasks of a mask set are typically aligned with each other using alignment marks that are provided on the photomasks. Such alignment ensures that the various features that are formed on the substrate are laterally aligned with each other in the desired manner. Such alignment marks can be used to control the amount of overlap between two layers of material. Therefore, alignment marks can be used to control the amount of overlap between bottom and top electrodes of an MIM device and, therefore, control the size of the MIM device's active area.

FIG. **5** shows examples of alignment marks provided on two photomasks **52**, **54** of the mask set **50** of FIG. **4**. As shown in FIG. **5**, the first photomask **52** comprises an alignment mark **58** in the form of a series of corner markers **60-66**. Each corner marker **60-66** comprises a first line (x-direction line) that extends from a point and a second line (y-direction line) that extends from the same point in a direction 90° out of phase of the first line so as to define a 90° corner. In the illustrated example, there are four such corner markers **60-66**, each equally spaced from its neighbor(s) along a 45° diagonal direction.

The second photomask **54** also comprises an alignment mark **68** that comprises a corner marker **70**. Like the corner markers **60-66**, the corner marker **70** comprises a first line that extends from a point and a second line that extends from the same point in a direction 90° out of phase of the first line so as to define a 90° corner. If the corner markers **60-66** are said to have lines that extend in the x direction and the y direction, the corner marker **70** can be said to have lines that extend in the −x direction and the −y direction so as to be rotated 180° relative to the corner markers **60-66**.

The alignment marks **58** and **68** can be used to control the overlap between different layers of a device. FIGS. **6**A-**6**C show an example of this. As indicated in FIG. **6**A, the first and second masks have been aligned so that the corner marker **70** of the alignment mark **68** aligns with the second corner marker **62** of the alignment mark **58**. With this configuration, a relatively small amount of overlap between two layers **72** and **74** will be formed.

Referring to next FIG. **6**B, the masks have been aligned so that the corner marker **70** of the alignment mark **68** aligns with the third corner marker **64** of the alignment mark **58**. With this configuration, a larger amount of overlap between two layers **72** and **74** results.

Finally, with reference to FIG. **6**C, the masks have been aligned so that the corner marker **70** of the alignment mark **68** aligns with the fourth corner marker **66** of the alignment mark **58**. With this configuration, a still larger amount of overlap between two layers **72** and **74** results.

In some embodiments, the alignment between two or more photomasks can be changed for different wafers to form devices having different current densities from wafer to wafer. In other embodiments, the alignment can be changed for different dies on the same wafer to form devices having different current densities on the same wafer.

FIGS. **7** and **8** show example arrays of devices (e.g., MIM devices) that can be formed using the above-described alignment method. In FIG. **7**, an array of first layers **76** is formed on a substrate using a first photomask and an array of second layers **78** is formed over the first array using a second photomask. As indicated in the figure, the second layers **78** overlap the first layers **76** to a relatively small degree. In FIG. **8**, an array of first layers **80** is formed on a substrate using a first photomask and an array of second layers **82** are formed over the first layers using a second photomask. In this example, however, the second layers overlap the first layers to a much larger degree. In some embodiments, such arrays can be used as sensors. For example, the devices can be immersed in a fluid (gas or liquid) and the electrical properties of the device, such as resistance or capacitance, can be observed to determine the effect of the fluid on the properties as a means of detecting the presence or concentration of a substance. In

such an application, different current densities resulting from different degrees of overlap can be used to adjust the sensing frequency.

Although the above discussion has focused on MIM devices, the disclosed methods can be used in conjunction with other devices, such as metal-insulator-semiconductor devices.

The invention claimed is:

1. An electrical circuit comprising:

a first multi-layer stack including a first bottom electrode and a first insulating layer;

a second multi-layer stack including a second bottom electrode and a second insulating layer; and

a continuous top layer that comprises a continuous piece of conductive material that is directly deposited on each insulating layer but not contacting the bottom electrodes, wherein the bottom electrodes, insulating layers, and continuous top layer together form two thin film tunnel devices in which the continuous top layer forms the top electrode for each tunnel device and electrically connects the tunnel devices.

2. The circuit of claim **1**, wherein the top layer is a continuous metal layer.

3. The circuit of claim **1**, wherein the bottom electrodes are made of metal and the insulating layers are made of a dielectric material.

4. The circuit of claim **1**, further comprising one or more further multi-layer stacks each comprising a bottom electrode and an insulating layer, wherein the continuous top layer is deposited on each multi-layer stack so as to form more than two tunnel devices in which the continuous top layer forms the top electrode for each tunnel device and electrically connects the tunnel devices.

5. The circuit of claim **1**, wherein the insulating layer of each multi-layer stack encapsulates its associated bottom electrode so as to cover the sides of the electrode.

6. The circuit of claim **1**, further comprising a substrate on which the circuit is formed.

7. The circuit of claim **6**, wherein the bottom electrodes are metal and deposited on the substrate, the insulating layers are deposited on the bottom electrodes, and the continuous top layer is metal and deposited on the insulating layers so as to form metal-insulator metal (MIM) tunnel devices.

8. The circuit of claim **7**, wherein the continuous top layer is also deposited on the substrate.

9. The circuit of claim **5**, wherein the continuous top layer is also deposited on the substrate.

10. The circuit of claim **4**, wherein the thin film tunnel devices are electrically connected in series.

11. The circuit of claim **4**, wherein the thin film tunnel devices are electrically connected in parallel.

12. An electrical circuit comprising:

a substrate;

a first multi-layer stack formed on the substrate, the first multi-layer stack comprising a first bottom electrode and a first insulating layer;

a second multi-layer stack formed on the substrate, the second multi-layer stack comprising a second bottom electrode and a second insulating layer; and

a continuous top layer of conductive material that is directly deposited on each insulating layer and the substrate but not contacting the bottom electrodes, wherein the bottom electrodes, insulating layers, and continuous top layer together form two thin film tunnel devices in which the continuous top layer forms the top electrode for each tunnel device and electrically connects the tunnel devices.

13. The circuit of claim **12**, wherein the bottom electrodes and the continuous top layer are both made of metal.

14. The circuit of claim **12**, wherein the insulating layers are made of metal oxide.

15. The circuit of claim **12**, further comprising one or more further multi-layer stacks each comprising a bottom electrode and an insulating layer, wherein the continuous top layer is directly deposited on each insulating layer so as to form more than two thin film tunnel devices in which the continuous top layer forms the top electrode for each tunnel device and electrically connects the tunnel devices.

16. The circuit of claim **15**, wherein the thin film tunnel devices are electrically connected in series.

17. The circuit of claim **15**, wherein the thin film tunnel devices are electrically connected in parallel.

18. The circuit of claim **12**, wherein the insulating layer of each multi-layer stack encapsulates its associated bottom electrode so as to cover the sides of the electrode.

19. The circuit of claim **12**, wherein the bottom electrodes are metal and deposited on the substrate, the insulating layers are deposited on and encapsulate the bottom electrodes, and the continuous top layer is metal and deposited on the insulating layers so as to form metal-insulator metal (MIM) tunnel devices.

20. The circuit of claim **1**, wherein the continuous layer overlaps only a portion of the bottom electrodes such that the thin film tunnel devices are smaller in area than the area of the bottom electrodes.

21. The circuit of claim **12**, wherein the continuous top layer overlaps only a portion of the bottom electrodes such that the thin film tunnel devices are smaller in area than the area of the bottom electrodes.

* * * * *